All-SiC 99.4%-efficient three-phase T-type inverter with DC-side common-mode filter

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This letter presents a hardware demonstrator of an all-SiC three-level T-type (3LTT) inverter with the common-mode (CM) EMI filter stages placed on the DC input instead of the AC output side, targeting, for example, high-efficiency PV applications. The extensive experimental characterization shows that state-of-the-art SiC transistors and a DC-side CM filter enable an unprecedented peak/full-load efficiency of 99.4% (calorimetric measurement) at 12.5 kW and a power density of 2.4 kW/dm^3 (39 W/in^3). The demonstrator fulfills CISPR 11 Class A EMI regulations as well as upcoming EMI standards for the frequency range of 9–150 kHz. Compared to other high-efficiency converters, which often employ bridge legs with more output voltage levels, the described 3LTT concept thus offers a very favorable trade-off between complexity and performance.

Introduction: Over the past decade, the global photovoltaics (PV) market has rapidly grown with a compound annual growth rate (CAGR) of 34% [1], with PV contributing by far the largest share of added renewables per year [2]. Thus, a worldwide PV generation capacity of about 940 GW has been reached at the end of 2021 [3]. In this context, there is a clear demand for the power electronics, especially the inverters that interface PV installations to the mains, to achieve ever higher conversion efficiencies with limited complexity and hence cost [4–6].

Targeting high-efficiency inverter systems, multilevel topologies are promising candidates [7–9], as power semiconductors with lower blocking voltage ratings and hence favorable conduction and switching characteristics can be employed. For example, a recently presented 10 kW active-neutral-point-clamped (ANPC) three-phase inverter employing a hybrid Si/GaN semiconductor configuration achieves a peak efficiency of 99.3% (at 5 kW), features a power density of 2.4 kW/dm^3, and fulfills the CISPR 11 Class A EMI regulations [10]. Similarly, some of the authors have investigated a 12.5 kW all-Si seven-level hybrid ANPC (7LHANPC) inverter in [11], which achieves a peak efficiency of 99.35% (at 10 kW), features a power density of 3.4 kW/dm^3, and also complies with CISPR 11 Class A.

However, the 7LHANPC approach is relatively complex due to the high transistor count (30 transistors in a three-phase inverter). It is therefore an interesting question whether similar performance can be achieved with reduced complexity. Three-level topologies have been found to offer interesting trade-offs between efficiency and power density [12, 13]. In particular, the three-level T-type (3LTT) topology originally proposed in the 1970s for thyristor-based circuits [14–16] is of high interest, because a three-phase AC-DC converter system can be realized with only 12 transistors. Even though half of the transistors must block the full DC-link voltage, we demonstrate in this letter that with state-of-the-art SiC transistors and an advantageous arrangement of the common-mode (CM) filter on the DC side [17, p. 36], [6, 12, 18], very high efficiencies can be achieved. Specifically, the designed 12.5 kW demonstrator features an unprecedented peak efficiency of 99.4% (calorimetrically measured at full load), a power density of 2.4 kW/dm^3, and fulfills the CISPR 11 Class A standard as well as upcoming EMI limits for the frequency range of 9–150 kHz.

In the following, we thus discuss first the advantages of a (fully passive; in contrast to the active DC-side CM filter discussed in [6]) DC-side CM filter for grid-connected converters, briefly summarize key hardware design aspects, present the complete experimental characterization of the 3LTT demonstrator, and compare the results with those of the mentioned 7LHANPC system [11].

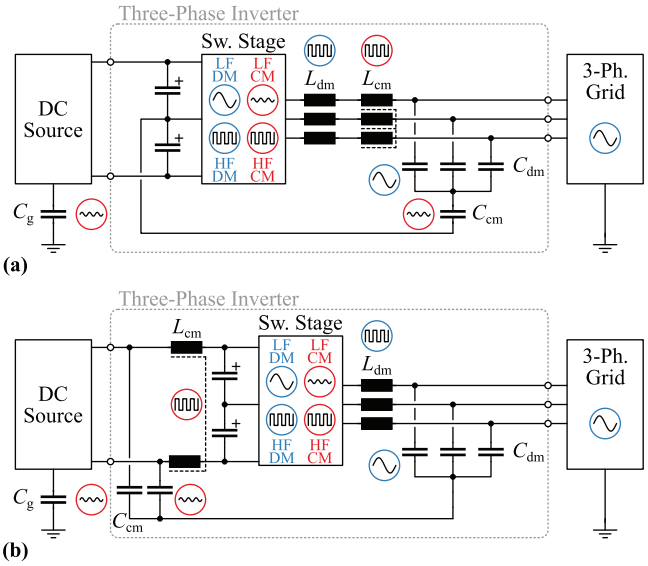

Fig. 1 *Conceptual EMI filter arrangements (one filter stage shown only) for three-phase inverters for, for example, PV applications. The PWM switching stage inherently generates LF DM, HF DM, and HF CM voltages, and LF CM voltages result if third-harmonic injection is employed; these voltage components appear across the filter components and the parasitic ground capacitance C_g as indicated. (a) DM and CM filter on the AC side. (b) Proposed DC-side CM filter concept and AC-side DM filter, which saves about 60% of the CM inductor's winding losses.*

DC-side common-mode EMI filter: Figure 1a shows a typical realization of a three-phase EMI filter with the differential-mode (DM) and CM filter elements on the AC side. Note that the DC-link midpoint is capacitively (via C_{cm}) connected to the star point formed by the three DM filter capacitors. This internal CM filtering approach has been proposed in the 1990s [19–21] for various topologies. Advantageously, relatively large values for C_{cm} can be selected, as the resulting CM current remains inside the converter and does not flow to earth, that is, the value of C_{cm} is not restricted by touch current limits. Further, note that if the modulation employs third-harmonic injection (which advantageously can prevent a 150 Hz current flowing into the DC-link midpoint and hence facilitates a reduction of the DC-link capacitance [12]), the corresponding low-frequency (LF) CM voltage appears at the DC terminals, that is, across the ground capacitance of the DC-side assembly (e.g. the PV panels). If the parasitic ground capacitances of the DC-side assembly would result in too high LF ground leakage current, which could trip residual current devices (RCDs), no third-harmonic injection should be used; furthermore, the leakage current could even be closed-loop controlled to zero [22].

Whereas in typical grid-connected motor drives an EMI limit applies at the AC input terminals, there are also multi-drive applications where the individual inverters operate from a distributed DC bus. Then, in certain applications, the EMI limits must be fulfilled at the inverter's DC input terminals but not at its AC output terminals; hence, a DC-side placement of CM filters is needed [23]. However, as initially proposed in [17, p. 36] and shown in Figure 1b, the CM inductor can be moved to the DC side also for grid-connected converters (for which the EMI limits apply on the AC side) without changing the system's behavior with respect to the DC and AC terminals. With the modulation index defined as $M = \sqrt{2}V_{ac}/(V_{dc}/2)$, the AC- and DC-side power balance yields

$$I_{dc} = \frac{3M}{2\sqrt{2}} I_{ac}, \tag{1}$$

where V_{ac} and I_{ac} are the rms phase voltage and current, respectively. The ratio of the winding losses of a DC-side CM inductor to those of an AC-side CM inductor becomes

$$\frac{P_{w,dc}}{P_{w,ac}} = \frac{2I_{dc}^2 R_{w,dc}}{3I_{ac}^2 R_{w,ac}} = \frac{2R_{w,dc}}{3R_{w,ac}} \cdot \frac{M^2}{4}, \tag{2}$$

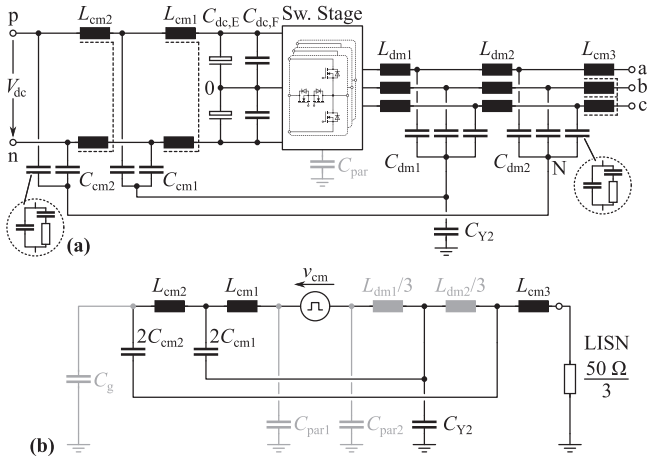

Fig. 2 *(a) Power circuit of the 3LTT prototype with a DC-side CM filter. (b) CM equivalent circuit (C_g represents the ground capacitance of the DC-side circuitry, for example, the PV panels, see Figure 1). Note that the equivalent circuit is simplified considering $C_{cm} \ll C_{dm}$; even though $L_{cm} \gg L_{dm}$ would allow a like simplification, the effective CM inductances of the DM inductors are indicated to facilitate the explanation of a potential resonance of $L_{dm1}/3$ with C_{par1} and C_{Y2}.*

where $R_{w,dc}$ and $R_{w,ac}$ denote the respective winding resistances. Finally, considering the same core and the same total copper usage for both types of CM chokes implies $R_{w,dc}/R_{w,ac} = 2/3$ and

$$\frac{P_{w,dc}}{P_{w,ac}} = \frac{M^2}{2} \approx 0.4 \tag{3}$$

for a typical modulation index of $M \approx 0.9$. This significant reduction of the low-frequency copper losses by about 60% is augmented by the absence of any significant high-frequency (HF) copper losses: except for the very small CM current, no HF currents flow on the DC side, whereas at least the first-stage CM inductor on the AC side would be exposed to the typically high DM HF ripple currents in the boost inductors [12]. On the other hand, also the DC-side of the switching stage is now subject to a high-frequency CM voltage with respect to ground.

Figure 2 shows the full power circuit of the 3LTT demonstrator implementing such a (two-stage) DC-side CM filter and the corresponding CM equivalent circuit. Note that in a practical realization, the presence of parasitic capacitances between the switching stage and ground (C_{par1}, C_{par2}) necessitates the placement of a (small) CM choke L_{cm3} at the grid terminals (i.e. on the AC side) and of a Y-capacitor C_{Y2}, because the internal CM filter arrangement does not provide any attenuation for CM currents through these parasitic capacitances [21]. Furthermore, as discussed in [18] for a single-stage DC-side CM filter without using the internal filtering approach (C_{cm1} and C_{cm2}), the parasitic capacitances from the DC bus to ground, C_{par1}, the Y2 capacitor C_{Y2}, and the effective CM inductance of the three first-stage DM inductors, $L_{dm1}/3$, form a resonant loop (see Figure 2b) that could cause excessive noise emissions at its resonant frequency (in the lower megahertz range with an estimated $C_{par1} \approx 200$ pF). With the selected hardware realization of the DM inductors (see below) using nanocrystalline cores and solid flat-wire windings, however, that resonance is sufficiently damped.

Hardware implementation: A 12.5 kW three-phase 3LTT inverter with the power circuit from Figure 2a has been implemented to demonstrate the high performance that a 3LTT topology with SiC transistors and a DC-side CM filter achieves. The employed design procedure including component modeling has been comprehensively described in [12]. For the sake of conciseness, we do only briefly reiterate key aspects here and Table 1 provides an overview of the components used for the hardware realization.

A relatively moderate switching frequency of 20 kHz is needed to limit the switching losses, whose estimation takes into account the additional capacitive loss contributions found in 3LTT bridge-legs [24]. At these operating frequencies, nanocrystalline core materials (specifically,

Table 1. Main power components of the 3LTT demonstrator shown in Figure 3a.

Component	Value	Part number
Half-bridge transistors	15 mΩ	Infineon IMW120R030M1H (1200 V, 30 mΩ; 2 × parallel per position)
Midpoint transistors	13.5mΩ	Infineon IMW65R027M1H (650 V, 27 mΩ; 2 × parallel per position)
Gate drive		Infineon 1EDI60N12AF
$C_{dc,F}$	75 µF	6 × TDK B32776G4506 (50 µF)
$C_{dc,E}$	200 µF	8 × Nichicon LGU2W101MELY (100 µF)
L_{dm1}	166 µH	2 × 20 turns (parallel), 2 mm × 5 mm wire Core: F3CC0040, 3 distr. airgaps
L_{dm2}	166 µH	2 × 20 turns (parallel), 2 mm × 5 mm wire Core: F3CC0040, 1 airgap
C_{dm1}, C_{dm2}	6.6 µF	2 × TDK B32924D3335K (X2)
L_{cm1}, L_{cm2}	1.6 mH	20 turns (per winding), 2 mm × 5 mm wire Core: F3CC0040, no airgap
C_{cm1}, C_{cm2}	440 nF	2 × KEMET PHE840MB6220
L_{cm3}	140 µH	External realization for EMI meas. with 3 turns (per winding) on VAC W516 core
C_{Y2}	44 nF	2 × TDK B32022B3223 (Y2)

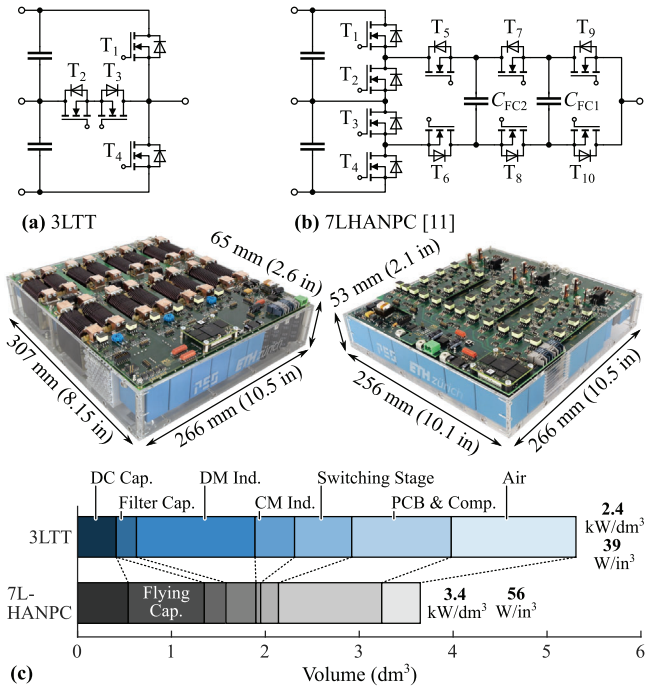

Fig. 3 *12.5 kW three-phase inverter demonstrator systems realized as (a) all-SiC 3LTT inverter with DC-side CM filter (this work) and, for comparison, (b) as all-Si seven-level hybrid active-neutral-point-clamped/flying-capacitor converter (7LHANPC) [11]. (c) Volume breakdown of the two demonstrator systems. The 3LTT demonstrator's power density is 2.4 kW/dm³ (39 W/in³) and the 7LHANPC prototype's is 3.4 kW/dm³ (56 W/in³).*

Hitachi Finemet F3CC) are well suited, and solid rectangular wire (i.e. helical) windings can be used instead of Litz wire windings. However, as known from literature such as [25, 26], estimating core losses of (gapped) nanocrystalline cores is prone to significant errors, for example, caused by misalignments and resulting magnetic field components that are perpendicular to the nanocrystalline laminations. Therefore, we have employed calorimetric pre-characterization measurements of L_{dm1} and L_{cm1} prototype realizations to improve the overall converter loss estimation compared to [12]. As can be seen in Figure 2a, the DC link features a combination of foil capacitors ($C_{dc,F}$) and additional electrolytic capacitors ($C_{dc,E}$), which would facilitate operation without

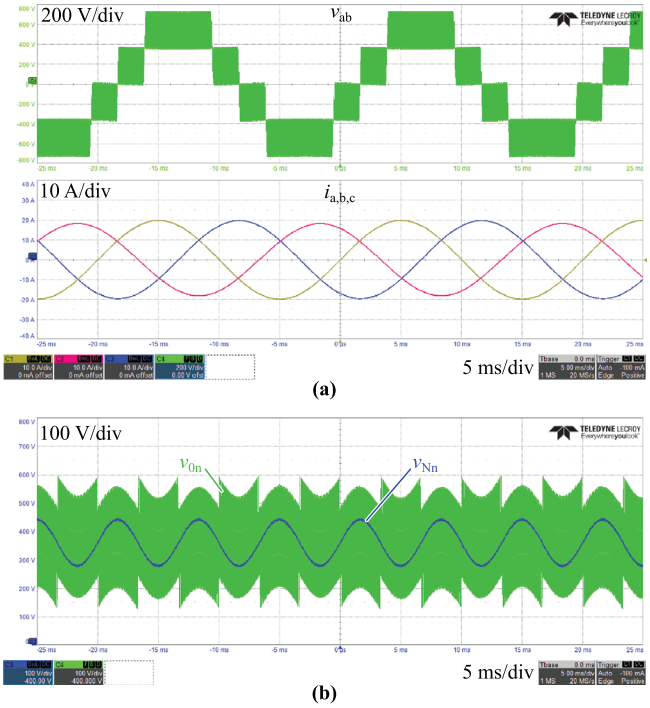

Fig. 4 *Measured key waveforms of the 3LTT demonstrator operating with a 720 V DC supply and a 10 kW three-phase resistive load. (a) Switched line-to-line voltage v_{ab} and the three phase currents $i_{a,b,c}$. (b) HF CM voltage v_{0n} between the DC-link midpoint 0 and the negative DC rail n, and LF CM voltage v_{Nn} measured between the second-stage DM filter star point N and the negative DC rail.*

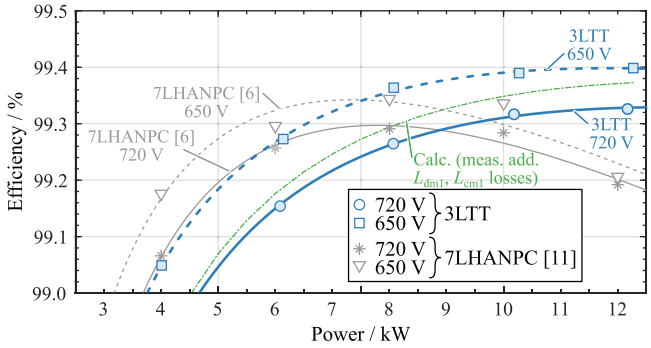

Fig. 5 *Calorimetrically measured efficiencies of the 3LTT demonstrator operating with 720 V and 650 V DC input and resistive load, and calculated curve for 720 V DC (as described in [12], but using the L_{dm1} and L_{cm1} losses obtained from component-level pre-characterization). For reference, the calorimetric measurement results for the 7LHANPC prototype from [11] are shown, too.*

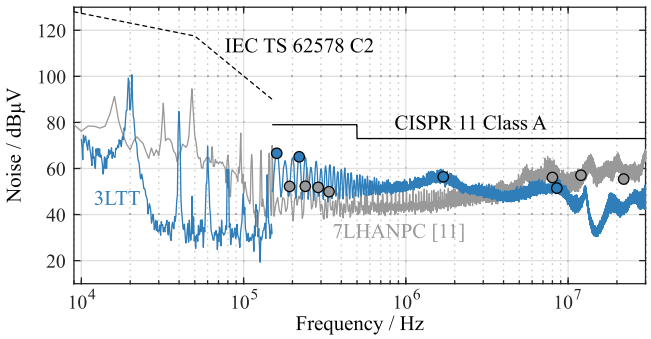

Fig. 6 *Conducted EMI noise emission spectrum of the 3LTT demonstrator operating with 720 V DC. The CISPR 11 peak (PK) detector has been used with a 2 kHz step size, 9 kHz resolution bandwidth, and 10 ms measurement time for frequencies >150 kHz, and with a resolution bandwidth of 200 Hz for frequencies <150 kHz. In addition to the CISPR 11 Class A limit, also a proposed limit (IEC TS 62578 Class 2) for the frequency range of 9–150 kHz is indicated. Selected peaks (see markers) have been measured with the quasi-peak (QP) detector during a 1 s measurement window. For reference, we also show the measurement results for the 7LHANPC demonstrator from [11].*

third-harmonic injection and hence a corresponding 150 Hz current flowing into the DC-link midpoint.

The prototype achieves a volumetric power density of 2.4 kW/dm^3 (39 W/in^3), see Figure 3a.[1] The 7LHANPC prototype described in [11] and shown in Figure 3b is more compact (3.4 kW/dm^3 or 56 W/in^3), mainly because the higher level count facilitates significantly smaller magnetic components. This also explains the lower weight of 4.8 kg (i.e. the gravimetric power density is 2.6 kW/kg) compared to the 3LTT inverter's 11.8 kg (1.1 kW/kg).

Figure 4 shows measured key waveforms of the 3LTT demonstrator operating from a 720 V DC voltage supply and with a 10 kW resistive three-phase load. The expected (see Figure 1b) separation of HF and LF CM voltage components is clearly visible; note that sinusoidal third-harmonic injection with $M_3 = \sqrt{2}V_{ac,(3)}/(V_{dc}/2) = 0.25$ has been used to almost completely mitigate any 150 Hz DC-link midpoint current.

Efficiency measurement: Due to the high expected efficiency levels, the specified accuracy of commercial power analyzers that rely on electrical measurements is at least theoretically not sufficient [11]. Therefore, a high-precision double-wall calorimeter [27] has been used to measure the efficiency characteristics at 720 V DC and 650 V DC shown in Figure 5. At 650 V DC, the 3LTT demonstrator achieves an unprecedented peak/full-load efficiency of 99.4%, and at 720 V DC still 99.3% (at full load). The figure also shows the (calorimetrically) measured efficiency characteristics of the all-Si 7LHANPC demonstrator as given in [11] for comparison purposes. Whereas the peak efficiencies are similar, the 7LHANPC inverter's efficiency curve bends downwards with increasing power, which can be attributed mostly to the comparably high number of semiconductors in the current path (see also Figure 3b) and to the stronger positive temperature coefficient of the Si transistors' on-state resistances, that is, to overall larger ohmic (quadratic) loss components. Interestingly, at 720 V, the 12.5 kW 3LTT inverter achieves a fitted European Weighted Efficiency of 98.8% and a CEC efficiency of 99.1% but the 7LHANPC inverter shows very similar values of 98.9% and 99.1%, respectively, despite the quite different efficiency characteristics.

Conducted EMI pre-compliance tests: Finally, conducted EMI pre-compliance tests have been carried out to assess the 3LTT demonstrator's compliance with CISPR 11 Class A as well as proposed limits for the frequency range of 9–150 kHz (IEC TS 62578 Class 2). The measurement setup consists of a Rhode & Schwarz ESH2-Z5 three-phase LISN and a Rhode & Schwarz ESPI3 EMI test receiver. The converter was placed on an appropriately sized, grounded aluminum plate emulating a housing to which C_{Y2} is connected. The AC-side CM choke L_{cm3} (see Figure 2a) is realized externally with 3 × 3 turns on a VAC Vitroperm 500F W516-03 core, resulting in a measured CM inductance of 142 µH; as mentioned above, a much smaller realization would be possible without significantly affecting the overall converter volume or losses. Figure 6 shows the measurement results and demonstrates compliance with both limits, including a minimum quasi-peak (QP) margin of 12 dBµV at 160 kHz, that is, the 8th harmonic of the switching frequency. Note the minor bump in the emission spectrum at around 1.7 MHz: this can be attributed to the above-mentioned resonance between C_{par1}, C_{Y2}, and $L_{dm1}/3$, which is well damped because of the DM inductors' core and winding losses in this frequency range. Thus, the DC-side CM filter provides the expected attenuation and shows the aforementioned advantages compared to the typical AC-side placement.

[1]Note that the 3LTT prototype does not contain L_{cm3}—it was realized externally during EMI pre-compliance testing—but the overall volume contribution would be negligible (e.g. 3 × 4 turns with a 1 mm^2 wire on a 16/10/06 VAC Vitroperm 500F core, resulting in 4.8 cm^3 boxed volume).

Conclusions: We have demonstrated that a relatively low-complexity three-level T-Type (3LTT) inverter realized with state-of-the-art SiC transistors can achieve an unprecedented peak/full-load efficiency of 99.4% (calorimetric measurement) at 12.5 kW and a power density of 2.4 kW/dm^3 (39 W/in^3). The proposed untypical placement of the common-mode (CM) inductors on the DC side (instead of on the AC side) has been demonstrated to work in hardware without issues (the inverter complies with CISPR 11 Class A and also with upcoming EMI regulations for the frequency range of 9–150 kHz), and clearly contributes to the converter's high efficiency. Overall, the 3LTT inverter's full-load efficiency is higher than that of a recently presented all-Si seven-level hybrid active-neutral-point-clamped (7LHANPC) inverter of equal power rating, which, however, is more compact (3.4 kW/dm^3 (56 W/in^3) instead of 2.4 kW/dm^3 (39 W/in^3) for the 3LTT inverter) but also more complex. Both systems reach almost identical weighted EU and CEC efficiencies. All-SiC 3LTT inverters with DC-side CM filter thus present a very attractive option for realizing future high-efficiency DC-AC inverter (or, for that matter, AC-DC PFC rectifier) systems. Whereas a high efficiency is clearly an important design target, in the course of future research also a system-level life-cycle analysis (LCA) should be performed to fully assess, for example, the trade-off between embodied energy and conversion losses [28], which should thus be in the focus of future power electronics research.

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