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Single-Phase PFC Rectifier With Integrated Flying Capacitor Power Pulsation Buffer

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ABSTRACT Single-phase Power Factor Correction (PFC) rectifiers with sinusoidal grid currents are inherently subject to an input power fluctuating at twice the mains frequency. In order to potentially mitigate bulky, heavy and failure-prone electrolytic dc-link capacitors, active Power Pulsation Buffer (PPB) concepts are proposed in the literature. For converter systems employing Flying Capacitor (FC) multilevel bridge-legs, the FCs can be utilized as a twice-mains frequency energy storage, i.e., as an integrated active PPB without the need for additional power components. Such ac-dc-stage-integrated FC PPBs capable of buffering the complete input power variation are known in literature which, however, require sophisticated control strategies with varying switching frequency and discontinuous conduction mode. This paper presents a novel ac-dc-stage-integrated FC-PPB approach which is compatible with standard PFC control concepts and enables a significant reduction in dc-link voltage variation. First, a control concept cycling the FC voltage in a wide range without interfering with the grid current controller is derived step by step and verified by means of circuit simulations. Design guidelines for the calculation of suitable FC capacitance values are presented and the limits in buffering capability are discussed. The concept is then experimentally verified with a 2.2 kW three-level FC single-phase PFC rectifier employing 600 V GaN power semiconductors where the dc-link voltage variation is reduced by 28% compared to conventional operation. Last, the applicability of the ac-dc-stage-integrated FC-PPB concept to other FC converter topologies is discussed.

INDEX TERMS Active energy buffer, integrated buffer, flying capacitor (FC), multilevel, GaN, single phase, AC-DC, DC-AC.

I. INTRODUCTION

Single-phase Power Factor Correction (PFC) ac-dc converter systems are employed in applications such as solar inverters, or server power supplies. When operating with unity power factor, the system is subject to an input power p_{ac} comprising an inherent twice-grid frequency $2f_{\mathrm{ac}} = \frac{2\omega_{\mathrm{ac}}}{2\pi}$ power pulsation

$$p_{\mathrm{ac}}(t) = \frac{1}{2}\hat{U}_{\mathrm{ac}}\hat{I}_{\mathrm{ac}} - \frac{1}{2}\hat{U}_{\mathrm{ac}}\hat{I}_{\mathrm{ac}}\cos(2\omega_{\mathrm{ac}}t), \qquad (1)$$

where $\hat{U}_{\mathrm{ac}}$ and $\hat{I}_{\mathrm{ac}}$ are the amplitudes of the grid voltage and current, respectively. Hence, the converter system is required to comprise low (twice-fundamental) frequency energy storage elements. In the most simple case, a large electrolytic dc-link capacitor buffers the pulsating input power, where the required capacitance value C_{dc} depends on the admissible low-frequency peak-to-peak capacitor voltage variation ΔU_{dc}. However, as can be seen in [1] the electrolytic dc-link capacitor of a single-phase PFC rectifier system occupies a substantial fraction of the converter volume. Moreover, electrolytic capacitors have limited lifetime, which is further reduced by large dc-link voltage variations ΔU_{dc} [2].

Aiming at ever more compact systems, active Power Pulsation Buffer (PPB) concepts are employed in literature [3], [4]. There, a dedicated circuitry covers the power pulsation, hence allowing for a significantly reduced dc-link capacitor value. Typically, film or ceramic capacitors are employed in an active PPB due to the high resulting voltage (current) swing. The main disadvantage of a conventional active PPB is the

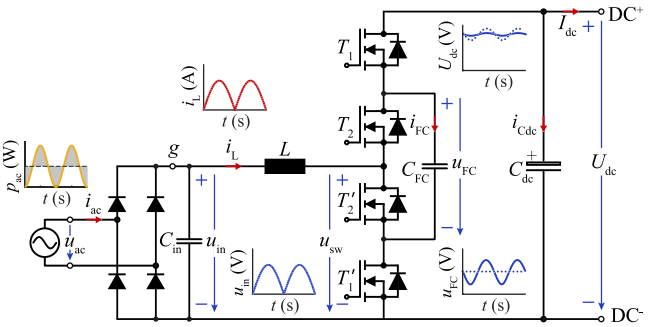

FIGURE 1. Main power circuit of a single-phase Three-Level (3L) Flying Capacitor (FC) Power Factor Correction (PFC) rectifier system with the input power p_{ac} fluctuating with twice the grid frequency. The main converter voltage waveforms are outlined: conventional operation (i.e., $u_{FC} = U_{dc}/2$) is represented by dotted lines, and active FC Power Pulsation Buffer (PPB) operation (i.e., u_{FC} varying over time) resulting in a reduced dc-link voltage U_{dc} variation by solid lines.

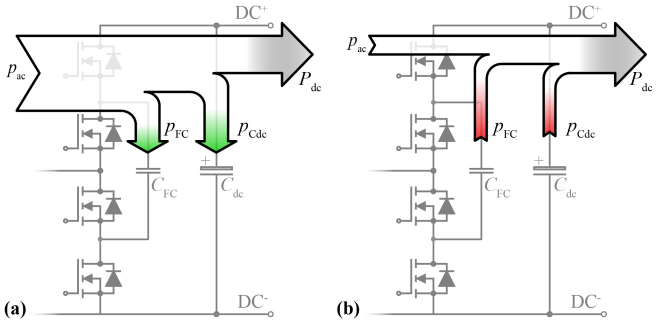

FIGURE 2. Sankey diagram of the main power flow quantities, i.e., grid input power p_{ac}, FC power p_{FC}, dc-link power p_{Cdc} and dc output power P_{dc} of a 3L FC PFC rectifier with active FC PPB operation for (a) $p_{ac} > P_{dc}$ and (b) $p_{ac} < P_{dc}$, where the FC is charged and discharged, respectively in order to decrease the power pulsation of the dc-link capacitor p_{Cdc}.

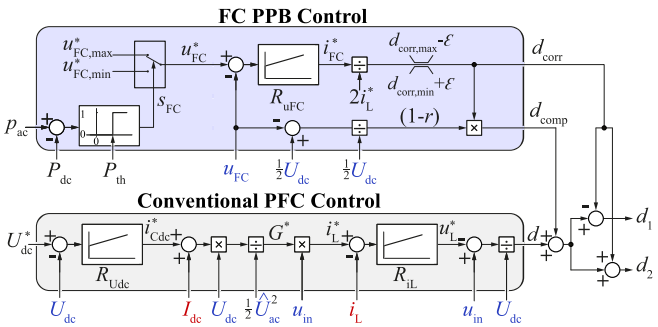

FIGURE 3. Considered 3L FC PFC rectifier control concept enabling active FC PPB operation.

required additional power components, the elevated system complexity, and a reduced overall system efficiency, compared to a passive solution with electrolytic capacitors [4].

Converters employing Flying Capacitor (FC) bridge-legs (see Fig. 1) have additional voltage levels and elevated effective switching frequency and hence enable a more compact and efficient converter realization compared to a standard two-level converter [5], [6]. FCs are typically solely used for creating multi-level voltages, but do not fulfill any low-frequency energy buffering purpose, i.e., the FCs are dimensioned mostly based on the tolerable high-frequency voltage ripple according to the voltage rating of the switches.

However, based on proper dimensioning the FCs actually represent internal energy storage elements, which can be cycled as PPB capacitors. No additional power components are required, hence making the concept very attractive for cost sensitive applications. However, it is important to highlight that (compared to standard FC converter operation), often semiconductors with an elevated voltage rating are required and the switching-frequency f_{sw} voltage harmonics are increased. Such an FC PPB was considered in [7], [8], [9] for a Three-Level (3L) FC dc-dc converter interfacing a solar panel and a (conventional) two-level single-phase inverter. An ac-dc-stage-integrated FC PPB approach is investigated in [10], [11]. There, the complete single-phase grid power pulsation is covered by the FC by means of a rather complex, varying-switching-frequency control strategy utilizing the high-frequency inductor current (up to 32 different control modes occur within one mains period). Further, ac-dc-stage-integrated FC PPB concepts based upon buck- and buck-boost-type single-phase ac-dc converters with full power pulsation compensation capability but relatively high component stresses are investigated in [12], [13], [14].

In this paper, we present an alternative ac-dc-stage-integrated FC PPB where solely the low-frequency inductor current and the redundant FC bridge-leg switching states are utilized to partially buffer the pulsating single-phase power. Hence, the FC PPB concept can be integrated into a conventional PFC rectifier control structure, thereby enabling a simple control circuit realization.

The paper is structured as follows: Section II derives the basic FC PPB power equations and presents the proposed control concept which is verified by means of simulations in Section III. Design guidelines and the selection of suitable FC capacitance and average voltage values are discussed in Section IV. Then, Section V presents experimental verification of the concept and compares the main converter waveforms for conventional operation and active FC PPB operation. Further, Section VI discusses how the concept can be employed in several different FC converter topologies and, last, Section VII summarizes the main findings of the publication and identifies further research questions relevant for integrated active PPB concepts.

II. ACTIVE FC PPB CONCEPT

As already mentioned, the ac-dc-stage-integrated FC PPB requires no hardware changes and this section presents the key control concept enabling the utilization of the FC of a 3L FC single-phase PFC rectifier as an energy buffer as illustrated in Fig. 2.

TABLE 1. 3L Switching States

Design.	T_1	T_2	u_{sw}	i_{FC}	FC
00	0	0	0	0	-
01	0	1	u_{FC}	i_{L}	charge
10	1	0	$U_{\mathrm{dc}} - u_{\mathrm{FC}}$	$-i_{\mathrm{L}}$	discharge
11	1	1	U_{dc}	0	-

The considered control diagram is depicted in Fig. 3 and is based on a conventional PFC rectifier control concept: The outer (slow) dc-link voltage control block R_{Udc} defines a grid current reference i_{L}^{*} (corresponding to a sinusoidal grid current i_{ac} in phase with the voltage u_{ac}) based on the dc-link voltage control error and the output current I_{dc} which is added as a feed-forward term.

The current reference is then tracked by the faster grid current controller R_{iL} defining the Pulse Width Modulation (PWM) duty cycle d resulting in a local average (over a switching period) switch-node voltage $\langle u_{\mathrm{sw}}\rangle = d \cdot U_{\mathrm{dc}}$.

The FC PPB is then realized with an active FC voltage controller R_{uFC} (which is discussed in more detail in the following subsections) adjusting the duty cycle d without impacting the generated local average switch-node voltage.

A. FC VOLTAGE CONTROL

3L FC converters typically operate with two 180° phase-shifted PWM carriers for the half-bridges T_1/T_1' and T_2/T_2' (see Fig. 1) and identical duty cycles $d_1 = d_2 = d$ such that natural FC voltage balancing [15] maintains the FC voltage $u_{\mathrm{FC}} \approx U_{\mathrm{dc}}/2$.

Here, aiming at FC PPB operation, the goal is to increase and decrease the FC voltage with twice the mains frequency (see Fig. 2). This is achieved by active FC voltage control (in contrast to conventional FC operation with natural balancing, an FC voltage measurement is required here) where the redundant FC bridge-leg switching states are used to charge or discharge the FC with the local average inductor current $\langle i_{\mathrm{L}}\rangle$ [7], [16]. Note that the high-frequency inductor current ripple does not have an impact for this type of balancing strategy.

The 3L FC bridge-leg switching states are described in Table 1 and for more details we refer to [5], [6]. A correction duty cycle d_{corr} alters the duty cycles of T_1/T_1' and T_2/T_2' with $d_1 = d - d_{\mathrm{corr}}$ and $d_2 = d + d_{\mathrm{corr}}$, respectively (see Fig. 3). Note that d_{corr} does not impact the duration of the switching states 11 / 00 (see Table 1). In contrast, d_{corr} linearly increases the duration of the charging state 01 and decreases the duration of the discharging state 10 [7], [16], hence yielding a local average FC current

$$\langle i_{\mathrm{FC}}\rangle = 2 \cdot d_{\mathrm{corr}} \langle i_{\mathrm{L}}\rangle, \tag{2}$$

and local average FC power

$$\langle p_{\mathrm{FC}}\rangle = 2 \cdot d_{\mathrm{corr}} \langle i_{\mathrm{L}}\rangle \langle u_{\mathrm{FC}}\rangle, \tag{3}$$

with $\langle i_{\mathrm{L}}\rangle$ and $\langle u_{\mathrm{FC}}\rangle$ representing the local average values of the inductor current and FC voltage, respectively. Hence, the correction-duty-cycle-based FC control block highlighted in Fig. 3 enables the utilization of C_{FC} as an ac-dc-stage-integrated FC PPB in a similar fashion as in [7].

It is important to highlight that if $u_{\mathrm{FC}} \neq U_{\mathrm{dc}}/2$ the "redundant" states 01 and 10 are no longer equivalent with respect to the resulting switch-node voltage u_{sw} (see Table 1) and the local average value $\langle u_{\mathrm{sw}}\rangle$ is defined by

$$\begin{aligned}\langle u_{\mathrm{sw}}\rangle &= d_1(U_{\mathrm{dc}} - u_{\mathrm{FC}}) + d_2 \cdot u_{\mathrm{FC}} \\ &= U_{\mathrm{dc}}\left(d - d_{\mathrm{corr}}\left(1 - \frac{2u_{\mathrm{FC}}}{U_{\mathrm{dc}}}\right)\right) \\ &= U_{\mathrm{dc}}(d - d_{\mathrm{corr}}(1 - r)),\end{aligned} \tag{4}$$

with $r \in [0, 2]$ representing a measure for the relative FC imbalance

$$r = \frac{2u_{\mathrm{FC}}}{U_{\mathrm{dc}}}. \tag{5}$$

Hence, to avoid an undesired interaction of the FC PPB and the current controller a compensation duty cycle

$$d_{\mathrm{comp}} = \left(1 - \frac{2u_{\mathrm{FC}}}{U_{\mathrm{dc}}}\right) \cdot d_{\mathrm{corr}} = (1 - r) \cdot d_{\mathrm{corr}}, \tag{6}$$

is added to d_1 and d_2 in Fig. 3. Note that $r = 1$ corresponds to a balanced FC with $u_{\mathrm{FC}} = U_{\mathrm{dc}}/2$ and $d_{\mathrm{comp}} = 0$. Finally, the duty cycles for the half-bridges T_1/T_1' and T_2/T_2' in Fig. 3 result to

$$\begin{aligned}d_1 &= d + d_{\mathrm{comp}} - d_{\mathrm{corr}} = d - r \cdot d_{\mathrm{corr}} \\ d_2 &= d + d_{\mathrm{comp}} + d_{\mathrm{corr}} = d + (2 - r) d_{\mathrm{corr}},\end{aligned} \tag{7}$$

assuring that the FC voltage control action does not disturb the grid current controller and/or does not influence the generation of the desired local average switch-node voltage $\langle u_{\mathrm{sw}}\rangle$.

B. DUTY CYCLE LIMITATION

Compared to the dc-dc-converter-integrated FC PPB [7], a substantial challenge for the ac-dc-stage-integrated FC PPB is the duty cycle d varying in a wide range within a mains period. It is crucially important to assure valid duty cycles d_1, $d_2 \in [0, 1]$ to avoid the saturation of the PWM signals with $\langle u_{\mathrm{sw}}\rangle \neq d \cdot U_{\mathrm{dc}}$ leading in consequence to a current controller disturbance caused by the FC PPB.

Hence, the correction d_{corr} and compensation d_{comp} duty cycles have to be limited if d is close to zero or unity. The condition of d_1, $d_2 \in [0, 1]$ and (7) can be translated into limit values

$$\begin{aligned}d_{\mathrm{corr,max}} &= \min\left(\frac{1 - d}{2 - r}, \frac{d}{r}\right) \\ d_{\mathrm{corr,min}} &= \max\left(\frac{-d}{2 - r}, \frac{d - 1}{r}\right),\end{aligned} \tag{8}$$

and in Fig. 3 an additional duty cycle margin ϵ of e.g., 5% is considered to assure current controllability.

To avoid undesired high-frequency coupling of the FC PPB and the current controller, the duty cycle d in (8) is substituted by the feed-forward duty cycle $d^* = u_{in}/U_{dc}$ which changes solely with grid frequency and can be further low-pass filtered to avoid any high-frequency noise originating from the feed-forward terms.

C. FC REFERENCE GENERATION

The dc-dc-converter-integrated FC PPB [7] defines the FC voltage reference u^*_{FC} based on the instantaneous difference between the time-varying input $p_{ac}(t) = i_{ac} \cdot u_{ac}$ and the constant output power $P_{dc} = U_{dc} \cdot I_{dc}$.

Here, an additional challenge for the ac-dc-stage-integrated FC PPB is given by the fact that the regulating variable, i.e., the local average of the inductor current $\langle i_L \rangle$ (see (2)) is time varying and during the AC current zero crossing the FC voltage cannot be actively controlled or influenced. Hence, the ac-dc-stage-integrated FC PPB is not capable of fully covering the pulsating input power, but can only perform a dc-link voltage variation *reduction*. It therefore makes sense, to define charging (i.e., the FC consumes excess input power) and discharging intervals (i.e., the FC releases energy towards the dc output) within a mains period, where the instantaneous input-output power discrepancy might even be overcompensated in certain time intervals.

This approach is realized by a simple bang-bang-type FC reference generation block presented in Fig. 3 which sets binary reference values

$$u^*_{FC} = \{u^*_{FC,min}, u^*_{FC,max}\}, \tag{9}$$

based on the instantaneous input-output power imbalance $p_{ac}(t) - P_{dc}$ compared to a charging/discharging threshold power P_{th}. Note that in general $u^*_{FC,min} > 0\,V$ and $u^*_{FC,max} < U_{dc}$, where the range of eligible FC voltages can be further constrained to assure that the power semiconductor voltage rating is not exceeded. By adjusting the threshold power P_{th}, the duration of the charging and discharging intervals can be adjusted, allowing to regulate the global average (over a mains period) $\bar{u}_{FC}$ of the FC voltage which represents a degree of freedom for the modulation of the active FC PPB. In the following, P_{th} is set by a (slow) controller regulating $\bar{u}_{FC}$ to the desired reference value $\bar{u}^*_{FC}$.

III. OPERATING BEHAVIOUR

The aim of this section is to illustrate the concept of the ac-dc-stage-integrated FC PPB depicted in Fig. 1 based on circuit simulation results and to allow for a qualitative understanding of the impact of the FC capacitance value on the energy buffering capability. The considered operating point specifications include a grid voltage U_{ac} =230 V_{rms} and frequency $f_{ac} = 50\,Hz$, a dc-link voltage $U_{dc} = 400\,V$ and power $P_{dc} = 2.2\,kW$. The dc-link capacitor is set to $C_{dc} = 610\,\mu F$ and a boost inductor $L = 140\,\mu H$ is selected.

For comparison, Fig. 4(a) first presents the simulated waveforms within one-half mains period for standard 3L FC PFC rectifier operation. As can be observed in Fig. 4(a.i) the FC voltage is balanced naturally to $u_{FC} = \bar{u}_{FC} = U_{dc}/2$ where a small switching-frequency f_{sw} FC voltage variation can be observed for $C_{FC} = 10\,\mu F$. Fig. 4(a.ii) shows the employed duty cycle $d = d_1 = d_d$ and for completeness the (approximately half-wave symmetric) eligible ranges for the correction duty cycle d_{corr} (which is here hard-coded set to $d_{corr} = d_{comp} = 0$).

Active ac-dc-stage-integrated FC PPB operation is presented in Fig. 4(b) for an identical $C_{FC} = 10\,\mu F$. A large variation of the FC bridge-leg duty cycles can be observed in Fig. 4(b.ii) where the eligible ranges for the correction duty cycle d_{corr} are now asymmetric as a compensation duty cycle d_{comp} (6) needs to be applied to compensate for the instantaneous FC voltage imbalance r (5). Note that the FC voltage in Fig. 4(b.i) quickly follows the reference value $u^*_{FC} = \{10\,V, 390\,V\}$ such that no further energy can be buffered after this short charging (or discharging) interval and in consequence the dc-link voltage variation ΔU_{dc} can be reduced only by 6% compared to standard operation (see Fig. 4(b.iii)). Hence, $C_{FC} = 10\,\mu F$ can be considered as an *undersized* FC value.

Accordingly, Fig. 4(c) presents the main converter waveforms for $C_{FC} = 50\,\mu F$. Here, $u^*_{FC} = \{10\,V, 390\,V\}$ is not immediately tracked, thereby enabling longer buffering intervals and a reduction of ΔU_{dc} by 25% compared to standard operation (see Fig. 4(c)).

Interestingly, a further increase of the FC value to $C_{FC} = 150\,\mu F$ (i.e., an increase by a factor of 3 compared to Fig. 4(c)) presented in Fig. 4(d) results in a reduction of ΔU_{dc} by 27% compared to standard operation, i.e., only a marginal improvement compared to Fig. 4(c). Hence, $C_{FC} = 150\,\mu F$ can be considered as an *oversized* FC value. The culprits for the observed saturation in buffering capability are the correction duty cycle limits which (for a given instantaneous grid current and FC voltage values) limit the instantaneous power intake of the FC PPB and hence the energy buffering capability within one half-mains period.

An alternative approach to further increase the energy buffering capability with $C_{FC} = 50\,\mu F$ is presented in Fig. 4(e) where the average (during one mains period) FC voltage is increased to $\bar{u}_{FC} = 250\,V$. With the elevated FC voltage values, an injected local average FC current corresponds now to a larger instantaneous power intake of the FC PPB (compared to $\bar{u}_{FC} = 200\,V$), thereby improving the energy buffering capability within one half-mains period [11]. Here ΔU_{dc} can be reduced by 33% in Fig. 4 (e.iii) compared to standard operation.

It is important to highlight that the dc-link voltage fluctuation for conventional operation in Fig. 4 (a.iii) is purely sinusoidal (at $2f_{ac}$). In contrast, the reduction in ΔU_{dc} in Fig. 4 (b.iii)–(e.iii) is accompanied by additional low-frequency components at multiples of $2f_{ac}$ which is to be considered in the design of the subsequent converter stage.

The results of Fig. 4(a)–(e) enable a basic understanding of the capabilities and limits of the ac-dc-stage-integrated FC

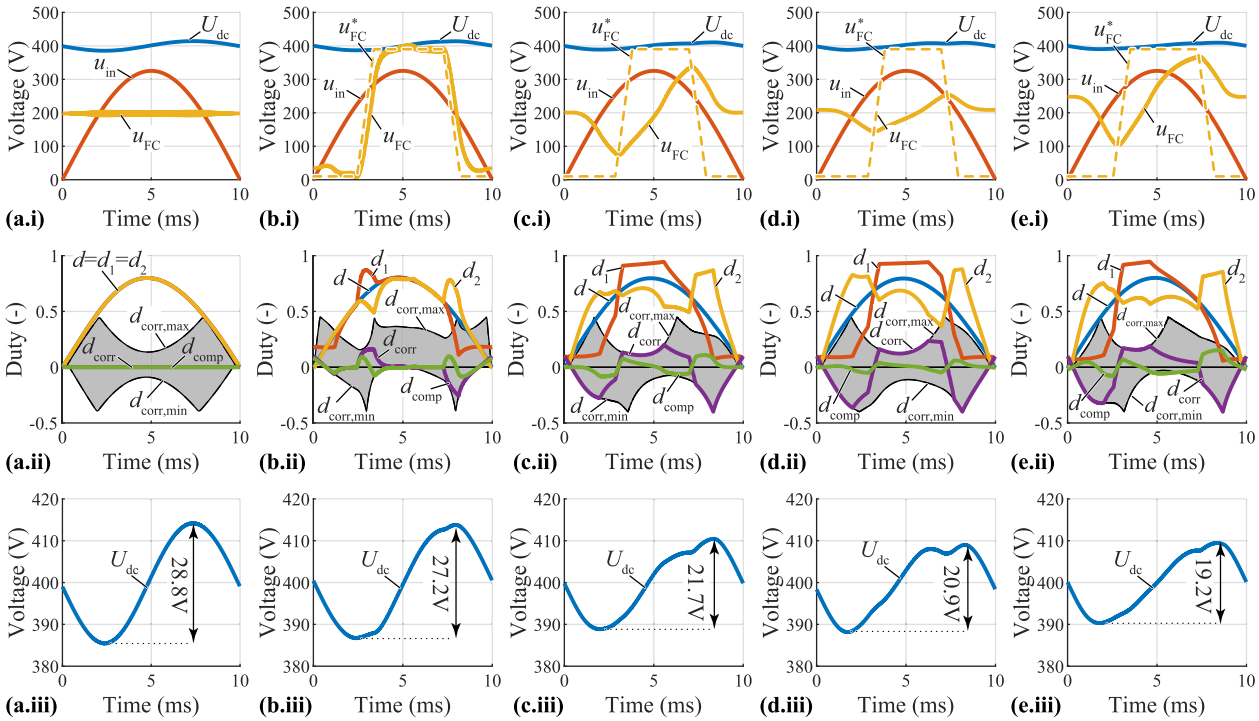

FIGURE 4. Simulated 3L FC PFC rectifier waveforms with a grid voltage U_{ac} =230 V_{rms} and frequency f_{ac} = 50 Hz, a dc-link voltage U_{dc} = 400 V and P_{dc} = 2.2 kW for (a) standard FC operation with C_{FC} = 10 µF and $\bar{u}_{FC}$ = 200 V, and for active ac-dc-stage-integrated FC PPB operation with (b) C_{FC} = 10 µF and $\bar{u}_{FC}$ = 200 V (i.e., an undersized FC, with P_{th} = 155 W), (c) C_{FC} = 50 µF and $\bar{u}_{FC}$ = 200 V (i.e., a reasonably-sized FC, with P_{th} = 736 W), (d) C_{FC} = 150 µF and $\bar{u}_{FC}$ = 200 V (i.e., an oversized FC, with P_{th} = 694 W), (e) C_{FC} = 50 µF and $\bar{u}_{FC}$ = 250 V (i.e., a reasonably-sized FC with elevated average FC voltage and P_{th} = 394 W). For all simulations a dc-link capacitor C_{dc} = 610 µF and a boost inductor L = 140 µH is considered.

PPB and the subsequent section provides a systematic design approach for the selection of the FC parameters.

IV. DESIGN CONSIDERATIONS

The aim of this section is to provide a guideline on how to select suitable FC values for the system with ac-dc-stage integrated FC PPB depicted in Fig. 1. The energy buffered by the dc-link capacitor, ΔE_{Cdc} (see Fig. 2) is defined by

$$\Delta E_{Cdc} = \int p_{Cdc} \mathrm{d}t = \int (p_{ac} - p_{FC} - P_{dc}) \mathrm{d}t. \qquad (10)$$

As discussed in Section III the time-domain waveforms of the correction duty cycle limit values $d_{corr,max}$ and $d_{corr,min}$ depend on the FC imbalance r and vice versa. Hence, no simple analytic expression exists for the impact of the FC capacitance value C_{FC} on the buffered energy of the dc-link capacitor $\Delta E_{Cdc} = f(C_{FC}, \bar{u}_{FC}, \hat{U}_{ac}/U_{dc}, f_{ac}, U_{dc})$. Accordingly, Fig. 5 presents results from an iterative circuit simulation allowing to identify suitable FC values where the considered operating point and component values are identical to Section III.

Fig. 5(a) highlights the energy buffered by the dc-link capacitor ΔE_{Cdc} vs. the FC capacitance value C_{FC} for a set of average FC voltages $\bar{u}_{FC}$ where ΔE_{Cdc} is normalized by the buffered energy resulting for conventional operation ΔE_0 (i.e., without active FC PPB) with a constant output power P_{dc}

$$\Delta E_0 = \frac{\frac{1}{2}\hat{U}_{ac}\hat{I}_{ac}}{2\pi f_{ac}}. \qquad (11)$$

There, it can be observed, that FC values $C_{FC} \approx 50$ µF enable a reduction of ΔE_{Cdc} by up to 40%. Further, high average FC voltages up to $\bar{u}_{FC} = 300$ V can be identified as advantageous, whereas a further increase in $\bar{u}_{FC}$ decreases again the buffering capability. Note that this is a major difference to the concept in [11] where $\bar{u}_{FC} = 350$ V was selected (also with $U_{dc} = 400$ V). As discussed in Section III, a further increase of C_{FC} above 50 µF only allows a marginal reduction in ΔE_{Cdc}, as now the FC power flow is constrained by the available duty cycle limits $d_{corr,max}$ and $d_{corr,min}$ and not the lack of storing capability of C_{FC}.

Fig. 5(b) depicts the overall capacitance $C_{FC} + C_{dc}$ required to maintain a constant peak-to-peak dc-link voltage variation $\Delta U_{dc} = 30$ V (i.e., $U_{dc} \in [385\,\mathrm{V}, 415\,\mathrm{V}]$) normalized by the reference dc-link capacitance required for standard PFC operation

$$C_{dc,0} = \frac{\Delta E_0}{U_{dc} \Delta U_{dc}} = 584\,\mu\mathrm{F}. \qquad (12)$$

As expected from the discussion of Fig. 5(a), the total capacitance can be minimized by up to 30% for $C_{FC} \approx 50$ µF, whereas a further increase in C_{FC} causes an increase in the overall required capacitance $C_{FC} + C_{dc}$.

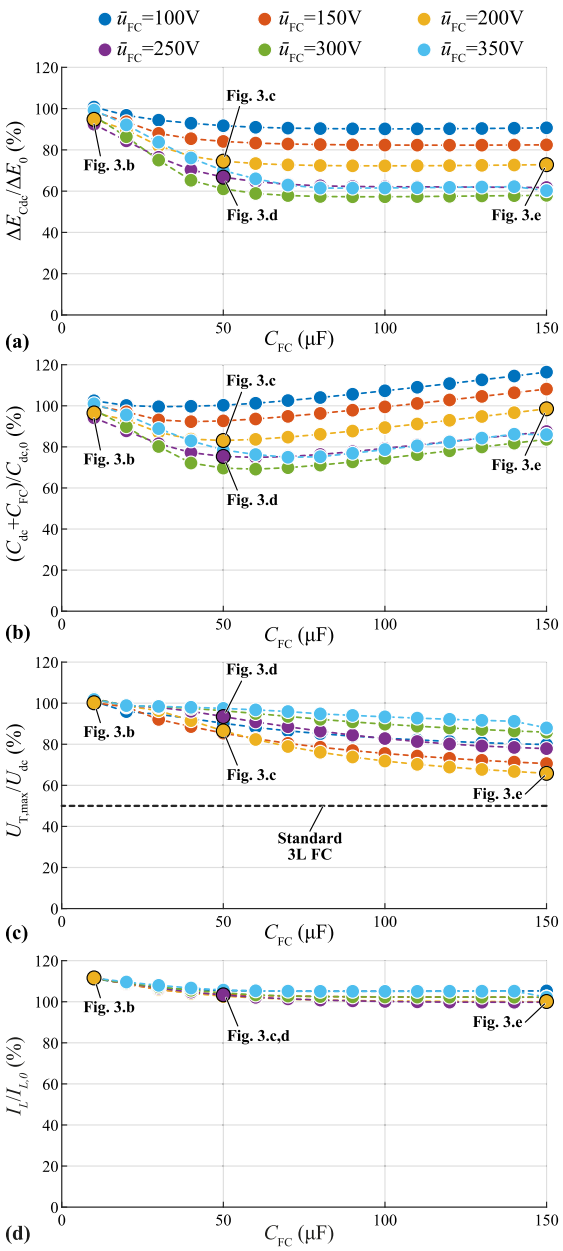

FIGURE 5. Simulated impact of the FC capacitance value C_{FC} for a set of average FC voltages $\bar{u}_{FC}$ for $U_{dc} = 400\,V$, $U_{ac} = 230\,V_{rms}$, $f_{ac} = 50\,Hz$ and $P_{dc} = 2.2\,kW$: (a) energy buffered by the dc-link capacitor ΔE_{Cdc} (normalized by the input power pulsation $\Delta E_0 = 7\,J$), (b) total system capacitance $C_{FC} + C_{dc}$ required to maintain a constant peak-to-peak dc-link voltage variation $\Delta U_{dc} = 30\,V$ (normalized by $C_{dc,0} = 584\,\mu F$), (c) maximum semiconductor blocking voltage $u_{T,max}$ (normalized by the dc-link voltage U_{dc}), (d) RMS inductor current I_L (normalized by the current stress for standard 3 L FC operation $I_{L,0} = 9.4\,A_{rms}$).

Then, Fig. 5(c) presents the maximum semiconductor blocking voltage within one mains period and the selected $u^*_{FC} = \{10\,V, 390\,V\}$ implies that switches with blocking voltage equal to $\approx U_{dc}$ are required for $C_{FC} \leq 50\,\mu F$ (i.e., an increase by a factor of two compared to standard 3L FC operation). It is important to highlight that the increased blocking voltage is accompanied by elevated high-frequency emissions

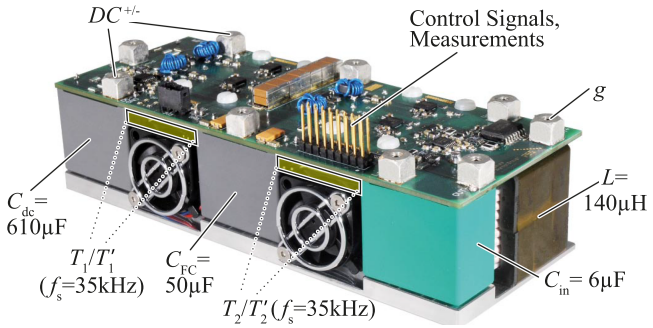

FIGURE 6. Employed 3L FC converter prototype (details on the system design can be found in [17] and component designators refer to Fig. 1). The system is connected to an external full-bridge diode rectifier (not shown).

by up to a factor of two which, however, corresponds to an increased line-side filtering demand of only 6 dB.

Note that the blocking voltage requirement could be eased with $\bar{u}_{FC} = U_{dc}/2 = 200\,V$ and a large C_{FC}, which, however, would diminish the overall capacitance savings (see Fig. 5(b)), such that similar to [11] semiconductors with full dc-link voltage blocking capability are the only reasonable choice.

Last, Fig. 5(d) presents the RMS inductor current stresses I_L normalized to the current stress for standard 3 L FC operation $I_{L,0} = 9.4\,A_{rms}$, which change by less than 15% across the considered ranges of FC capacitance value C_{FC} and the average voltage $\bar{u}_{FC}$. Note that the semiconductor RMS current stresses also change by less than 15% throughout the considered converter specifications and are hence not further detailed here.

It is worth highlighting that for converter specifications with an increased average power P_{dc} (or decreasing mains frequency f_{ac}) the results of Fig. 5 remain valid if the x-axis (i.e., the FC value C_{FC}) is scaled linearly with P_{dc} and/or the inverse of f_{ac}. Further, when aiming at a straight-forward FC PPB component sizing, the global average voltage $\bar{u}_{FC}$ and the binary voltage swing u^*_{FC} are selected as high as tolerable from the employed semiconductors in order to maximize the buffering capability. Then, starting from a low FC capacitance value C_{FC}, the value of C_{FC} is iteratively increased until the decrease in ΔE_{Cdc} (see Fig. 5(a)) begins to saturate.

V. EXPERIMENTAL VERIFICATION

Fig. 6 depicts the 3L FC converter prototype (and the main power component values) from [17] rectifying a grid voltage of $U_{ac} = 230\,V_{rms}$ to a dc-link voltage $U_{dc} = 400\,V$. Employing Gallium Nitride (GaN) semiconductors with a blocking voltage of 600 V (IGOT60R070D1) capable of switching the full dc-link voltage, the FC voltage can be allowed to vary in a range $u_{FC} \in [0, U_{dc}]$.

Fig. 7(a.i), presents the main converter waveforms of the FC rectifier shown in Fig. 6 and $P_{dc} = 2.2\,kW$ in conventional 3L operation with $u_{FC} \approx U_{dc}/2 = 200\,V$, where a peak-to-peak dc-link voltage variation $\Delta U_{dc} = 29.6\,V$ can be observed.

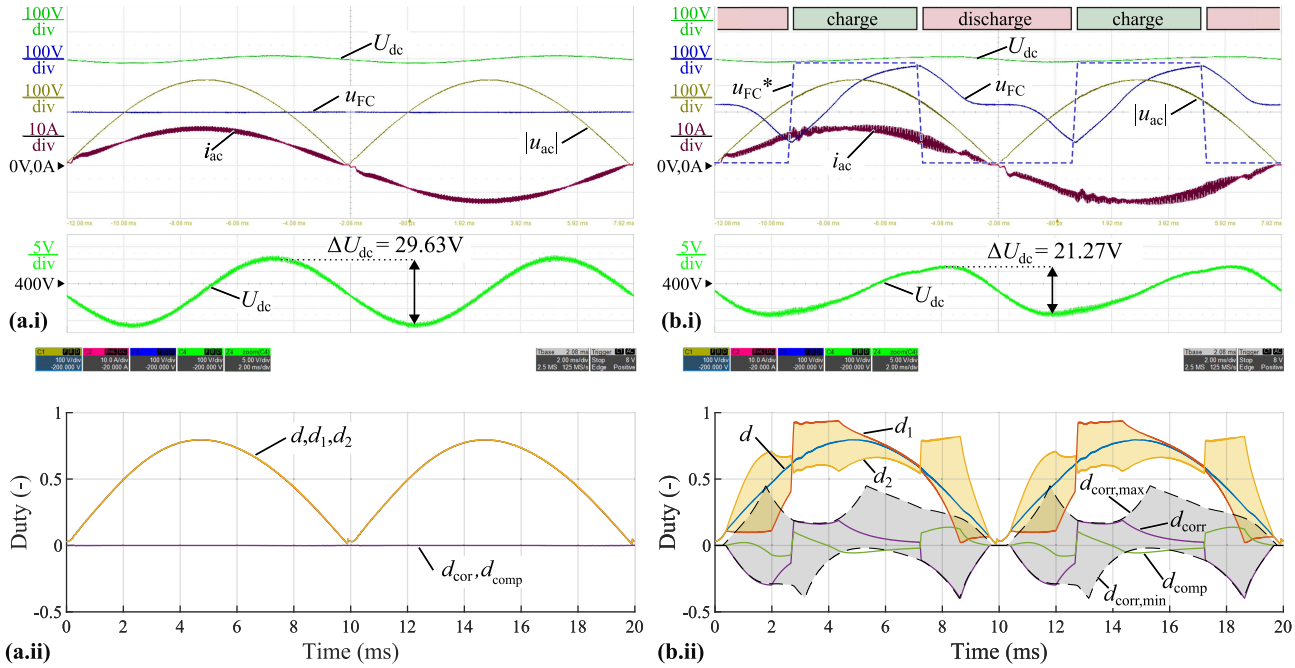

FIGURE 7. Experimental 3L FC PFC rectifier waveforms with a grid voltage U_{ac} =230 V_{rms} and frequency f_{ac} = 50 Hz, a dc-link voltage U_{dc} = 400 V and P_{dc} = 2.2 kW for (a) standard and (b) active ac-dc-stage-integrated FC PPB operation (see Fig. 4(e)): (a.i)/(b.i) are oscilloscope screenshots and (a.ii)/(b.ii) show the experimental duty cycle waveforms exported from the controller. The FC reference voltage u^*_{FC} = {10 V, 390 V} was also exported from the controller and added on top of (b.i) to highlight the FC charging and discharging intervals.

Fig. 7(a.ii) further details the duty cycles exported from the control board, where conventional operation is characterized by $d_{corr} = 0$ and $d_1 = d_2 = d$.

Operation with the proposed integrated FC PPB is outlined in Fig. 7(b.i), where the FC voltage u_{FC} varies in a wide range with twice the mains frequency and at the same time a sinusoidal grid current i_{ac} is maintained. Note that due to the fluctuating FC voltage the switching-frequency f_{sw} component of u_{sw} does no longer cancel out (in contrast to conventional 3L FC operation), such that an increased high-frequency grid current ripple can be observed. Here, the dc-link voltage variation results to $\Delta U_{dc} = 21.3$ V corresponding to a 28% improvement compared to conventional FC operation, which is close to the result of Fig. 4(e). This reduced ΔU_{dc} is especially beneficial as the expected lifetime of an electrolytic capacitor depends both on temperature and current stress [2], i.e., is extended by employing the proposed integrated FC PPB operation. Alternatively, the dc-link capacitor could be decreased while maintaining a constant dc-link voltage fluctuation.

In contrast to Fig. 7(a.ii), the duty cycles d_1 and d_2 in Fig. 7(b.ii) differ substantially. There, the correction d_{corr} and the compensation duty cycle d_{comp} (preventing a current controller disturbance by the active FC PPB), and the correction duty cycle limits $d_{corr,max}$ and $d_{corr,min}$ (aiming at a valid duty cycle range of [0.1,0.95]) are also highlighted.

As expected, the discharging of the FC slows down in the vicinity of the current zero crossing (see Fig. 7(b.i) for $t \approx 10$ ms), which is a result of 1) the low inductor current values and 2) the limited range of admissible correction duty cycle values for d close to zero. Here, a threshold power $P_{th} \approx 400$ W increases the duration of the discharging intervals and assures that a global average FC voltage $\bar{u}_{FC} = 250$ V is maintained.

All in all, it can be stated that a 28% dc-link voltage variation ΔU_{dc} improvement is enabled by the active, ac-dc-stage-integrated FC PPB operation for the topology presented in Fig. 1. Note that this dc-link voltage variation improvement, results in a slight increase of the grid current Total Harmonic Distortion (THD) (considering up to the order 40) from 1.7% in Fig. 7(a.i) to 3.2% in Fig. 7(b.i), which, however, still remains substantially below a typical THD value of 5% of industrial demonstrator systems.

VI. APPLICABILITY OF THE CONCEPT

It is worth highlighting that the ac-dc-stage-integrated FC PPB concept presented here could be also employed to topology variants of the 3L FC converter shown in Fig. 1 and several topology candidates of interest are presented in Fig. 8.

In case bidirectional power flow is required and/or the conduction losses of the front-end diode bridge of the single-phase PFC rectifier circuit of Fig. 1 should be avoided, an unfolder bridge-leg T_N/T'_N can be employed, resulting in the converter topology depicted in Fig. 8(a). Advantageously, the unfolder only operates at mains frequency, such that T_N and T'_N can be realized with low-on-state resistance Silicon (Si) Super Junction (SJ) semiconductors.

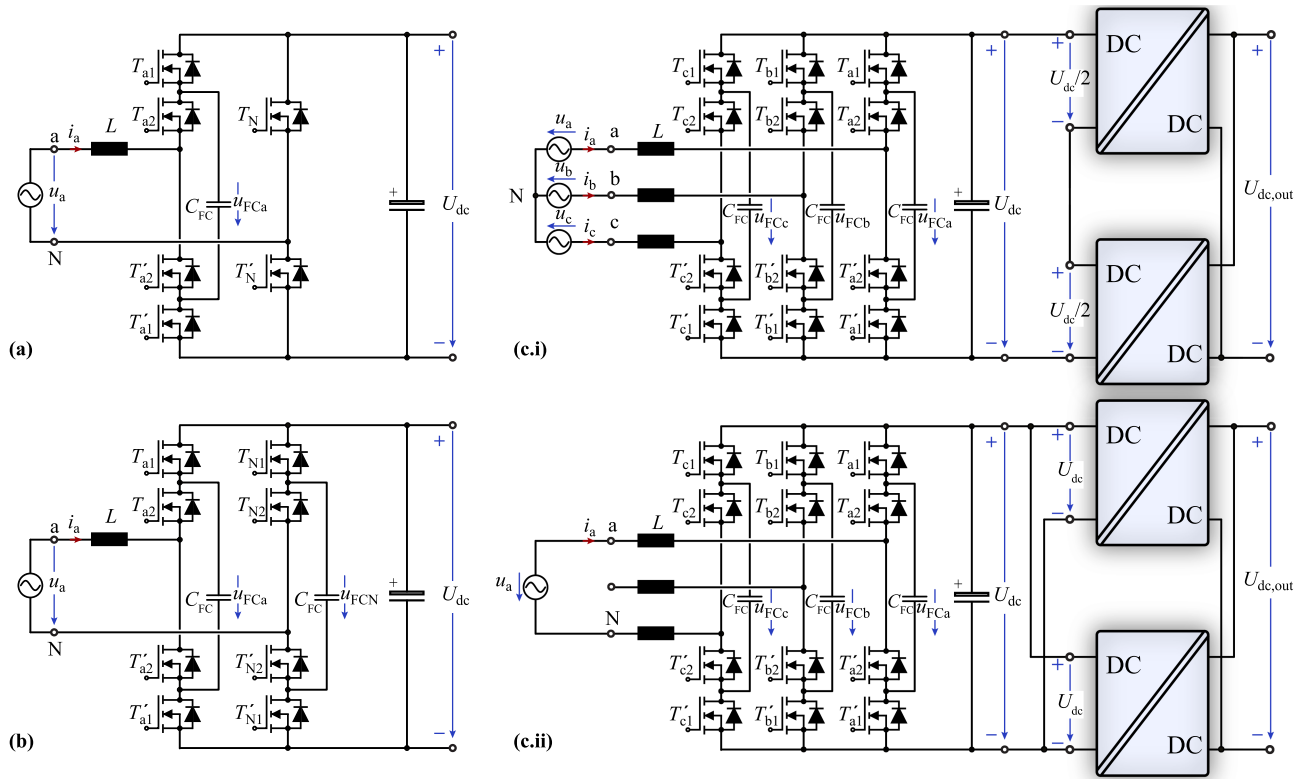

FIGURE 8. Further applications of the 3L FC bridge-leg with integrated PPB introduced for a single-phase PFC rectifier with a front-end diode bridge in Fig. 1: (a) bidirectional realization with a main-frequency-operated unfolder bridge-leg T_N/T'_N, (b) bidirectional H-bridge realization employing two high-frequency-operated FC bridge-legs, (c) converter topology featuring three-phase and single-phase ac-dc power conversion.

Alternatively, Fig. 8(b) presents an H-bridge realization employing two FC bridge-legs which are both high-frequency switched. Here, an even larger reduction of the dc-link voltage variation compared to the system in Fig. 1/Fig. 8(a) is facilitated, as advantageously 1) twice the energy can be buffered due to the second FC and 2) a duty cycle of $d \approx 0.5$ results in the vicinity of the grid current zero crossing enabling large correction duty cycle values and hence charging/discharging intervals of approximately equal length with additional buffering capability.

Another interesting field of application for the ac-dc-stage-integrated FC PPB concept is a PFC rectifier system capable of operating in a single-phase as well as a three-phase AC grid [18], [19] as highlighted in Fig. 8(c). For safety reasons, this system provides galvanic isolation which is realized with two isolated dc-dc converters. In three-phase operation (Fig. 8(c.i)), the grid input power is constant, and hence no PPB is required and the FC voltages remain constant at half the dc-link voltage. For a boost-type system, a large dc-link voltage is required with $U_{dc} > \sqrt{3}\hat{U}_{ac}$, where $U_{dc} = 800\,\text{V}$ is a typical voltage level allowing to utilize 600 V GaN power semiconductors, which can be also employed in the two isolated dc-dc converters connected in an Input-Series-Output-Parallel (ISOP) configuration. In single-phase operation (Fig. 8(c.ii)), the input power p_{ac} is pulsating with twice the mains frequency. Since the minimum dc-link voltage criterion is relaxed to $U_{dc} > \hat{U}_{ac}$, e.g., $U_{dc} = 400\,\text{V}$ can be selected, such that the integrated FC PPB can cycle the FC voltages u_{FCa} and u_{FCc} in a wide range, thereby reducing the minimum required dc-link capacitor value, while the blocking voltage capability of the 600 V GaN semiconductors is respected. Here, the isolated dc-dc converters are advantageously reconfigured to Input-Parallel-Output-Parallel (IPOP), such that the isolated dc output voltage $U_{dc,out}$ remains identical to three-phase operation.

VII. CONCLUSION

Conventional single-phase PFC rectifier systems require large dc-link capacitors to buffer the twice-mains frequency input power pulsation. This paper presents an ac-dc-stage-integrated Flying Capacitor (FC) Power Pulsation Buffer (PPB) for single-phase ac-dc converters employing FC bridge-legs requiring no additional power components. The presented 3L FC control concept is based on the utilization of the redundant switching states and can be integrated into a standard PFC rectifier control structure. The proposed control concept allows to manipulate the FC power flow within certain bounds, thereby enabling a power pulsation and/or a dc-link voltage variation reduction.

Experimental verification with a 2.2 kW prototype presented in this paper revealed a dc-link voltage variation reduction of 28% enabled by the active, ac-dc-stage-integrated FC PPB, which is closely matching the achievable reduction

found by circuit simulations. With the completed verification of the control concept based upon an existing converter system, in a next step a performance assessment with respect to the limits in power density and efficiency by means of an optimized converter prototype (including a grid-side high-frequency filter) employing the FC PPB concept can be conducted. In closing it is important to highlight that the proposed FC PPB concept can be employed in a wide variety of single-phase ac-dc FC converters.

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