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Comparative Evaluation of Three-Phase Three-Level GaN and Seven-Level Si Flying Capacitor Inverters for Integrated Motor Drives Considering Overload Operation

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ABSTRACT Integrated Motor Drives (IMDs) are gaining popularity in industrial Variable Speed Drive (VSD) applications, thanks to their more compact realization and simpler installation. However, mission profiles of, e.g., servo applications, demand overload torques of two to three times the nominal value during several seconds, which is thermally challenging for the power electronics. Accordingly, high efficiency and power density of the inverter are of paramount importance for motor integration. Multi-Level Flying Capacitor inverters (ML-FCis) benefit from a reduced output filter volume and improved switching and on-state performance of low-voltage devices for increasing number of levels N, whereas the PCB overhead and gate drive volume increases. In this paper, the most power dense solution between a seven-level (7L) FCi with Si semiconductors and a three-level (3L) FCi with GaN semiconductors is evaluated. Thereby, a straightforward design procedure allows to dimension both FCis for 99% efficiency at nominal operation, while providing a high short-term overload torque (three times the nominal torque) also for low inverter output frequencies. Due to its slightly higher power density and greatly reduced complexity, a phase module of the 3L GaN FCi is realized as an IMD hardware demonstrator. A transient thermal model is employed to specify the feasible overload operating range, considering the limited heat spreading in the baseplate and parameter variations, e.g., from manufacturing tolerances. The experimental analysis of the demonstrator verifies an efficiency of 98.94% and the practically required overload capability.

INDEX TERMS Integrated motor drive, variable speed drive, multi-level inverter, flying capacitor, overload operation, WBG power semiconductors.

I. INTRODUCTION

VARIABLE Speed Drives (VSD) supplying, e.g., high-performance servomotors, are ubiquitous in today's industrial automated manufacturing processes. They enable accurate control of position, speed and torque while achieving high total system efficiencies, which comply with the current interest of sustainable production and energy saving [1].

Typically, a VSD system is realized as a standalone three-phase inverter combined with an active/passive front-end rectifier stage and is accommodated in a dedicated cabinet. The generated Pulse Width Modulated (PWM) voltages at the inverter output are applied to the motor windings, which requires a shielded cable between cabinet and motor to confine Common Mode (CM) EMI emission. While this system arrangement allows high flexibility in the selection and combination of individual components, the shielded motor cables are expensive [2] and still potentially introduce additional voltage stress on the insulation of the motor windings due to overvoltages resulting from voltage reflections at the motor terminals [3].

1) Integrated Motor Drives (IMDs)

Accordingly, a trend has developed towards drive systems with motor-integrated inverters (so-called *Integrated Motor Drives (IMDs)*), which largely eliminate the requirement of complex shielded wiring and thus allow a simple and compact

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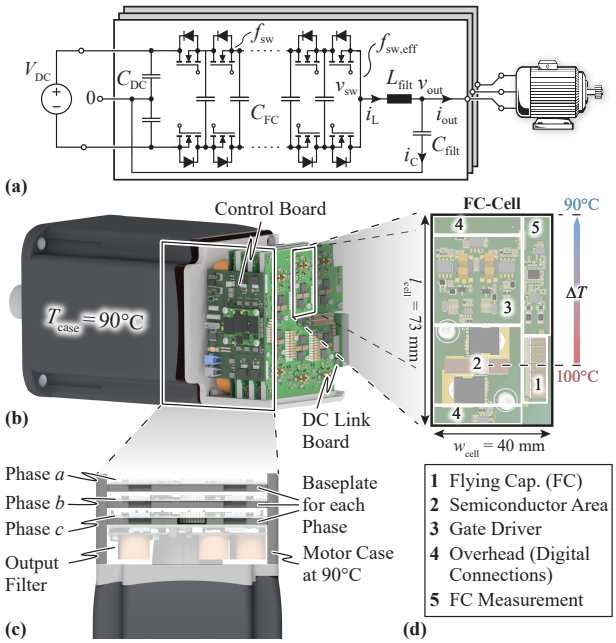

FIGURE 1: **(a)** Schematics of a Multi-Level (ML) Flying Capacitor inverter (FCi) phase module. **(b)** Phase-modular Integrated Motor Drive (IMD) setup. **(c)** Side view without DC link and control board. **(d)** Rendered 3D layout of a FC-cell of a 7L-Flying Capacitor inverter (FCi) prototype with labeled main components whose volumes are considered in the design optimization (Section II). The temperature gradient over the baseplates of the phases to the motor case at $T_{\mathrm{case}} = 90\,^{\circ}\mathrm{C}$ is assumed as maximum $\Delta T = 10\,^{\circ}\mathrm{C}$.

installation of the system [4]. Moreover, advantageous for motor integration, a recent tendency towards local *DC power grids* has emerged in industry, where several independent drives operate on a common DC link bus, which allows a direct energy exchange of accelerating and braking motors. Thereby, the active/passive rectifier front end, which was previously required for each drive separately, is replaced with a central bidirectional Power Factor Corrected (PFC) rectifier unit for connection to the AC mains [5]. The resulting lower number of components of the drive (i.e., only the inverter) strongly facilitates the direct integration into the motor [6]. Several inverter motor integration concepts have been discussed in the literature and were classified into four main arrangements: Radial housing mount, radial stator mount, axial endplate mount and axial stator mount [7].

If the specific frame size (and thus indirectly also the diameter) of a given motor should be maintained despite drive integration (e.g., NEMA frame size [8]) an axially mounted drive is often the only option. In this case, however, the frame size restricts the available mounting area for the inverter. In order to overcome this limitation, one possible approach is to utilize a phase modular assembly such as shown in **Fig. 1 (b)**, where each phase module is mounted on an individual baseplate, which is fixed on two sides to the elongated motor case (cf. **Fig. 1 (c)**). At the remaining two sides, the control board as well as an interconnecting DC link board are attached, providing similar connection distances for all phases.

TABLE 1: Specifications of the analyzed Integrated Motor Drive (IMD).

Parameter		Value
DC-Link Voltage	V_{DC}	800 V
Nominal Output Power (Three-Phase)	P_{nom}	$3 \cdot 2.5\,\mathrm{kW}$
Nominal Output Voltage Amplitude	$v_{\mathrm{out,nom}}$	330 V
Nominal Phase Current Amplitude	$i_{\mathrm{out,nom}}$	15 A
Overload Phase Current Amplitude	$i_{\mathrm{out,OL}}$	45 A
Overload Duration	t_{OL}	3 s
Maximum Inverter Output Frequency	$f_{\mathrm{out,max}}$	300 Hz
Motor Case (Ambient) Temperature	T_{case}	$90\,^{\circ}\mathrm{C}$
Minimum Nominal Inverter Efficiency	$\eta_{\mathrm{nom,min}}$	99 %

The thermal management of an IMD varies with the type of integration and the target requirements. The power electronics can be thermally insulated from the motor, thus allowing a more independent design of motor and/or power electronics, especially with two separate cooling systems (i.e., water cooling, forced or natural convection cooling over the housing/additional cooling fins or heat conduction over the flange), but resulting in a larger total volume. Alternatively, the power electronics can be thermally connected to the motor leading to a more compact integration into a single housing without thermal barriers, but at the cost of potentially higher operating temperatures of the semiconductors in the vicinity of the motor. For example in the case at hand, the inverter stage has to be able to operate at the peak temperature of the naturally cooled motor housing (i.e., $T_{\mathrm{case}} = 90\,^{\circ}\mathrm{C}$ as specified in **Table 1**).

Consequently, the realization of an IMD does not only rely on compact power electronics (i.e., high power density ρ) to minimize the overall system size, but also on high efficiency η to avoid exceeding the maximum allowed operating temperatures of various electronic components due to self-heating; power semiconductors are typically rated for junction temperatures of $150\,^{\circ}\mathrm{C}$ to $175\,^{\circ}\mathrm{C}$, Digital Signal Processors (DSPs) and current sensors up to $125\,^{\circ}\mathrm{C}$, and capacitors in the range of $105\,^{\circ}\mathrm{C}$ to $200\,^{\circ}\mathrm{C}$.

Both, high ρ and high η objectives can advantageously be accomplished with Wide-Bandgap (WBG) unipolar power semiconductors, i.e., SiC and GaN power MOSFETs, which offer an attractive alternative to the established Si IGBTs due to their significantly lower switching and conduction losses. However, the improved performance of WBG devices comes at the cost of a high $\mathrm{d}v/\mathrm{d}t$ ($> 20\,\mathrm{V/ns}$) during switching transients. Said $\mathrm{d}v/\mathrm{d}t$ does not only cause ringing and overvoltages in long motor cables, which advantageously are not present in an IMD, but also result in uneven voltage distribution over the motor windings as well as bearing currents, thus potentially leading to premature insulation aging and/or partial discharge issues [9], [10]. To mitigate these issues, $\mathrm{d}v/\mathrm{d}t$-filters can be placed at the inverter's output terminals [11] to lower the switching speed to the ratings accepted by motor manufacturers.

Alternatively, the installation of a sine-wave *LC* output filter after the inverter stage fully protects the motor from

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any of the aforementioned dv/dt effects. In addition, it prevents any Low-Frequency (LF) CM resonances, which can be excited in the motor independently of the dv/dt [12], and advantageously eliminates any High-Frequency (HF) losses in the motor, which can contribute to an overall higher system efficiency [13]. The *LC* filter cutoff frequency can be selected relatively high for WBG devices—thanks to the high possible switching frequencies—which accordingly enables compact filter designs [14]. Nevertheless, for conventional two-level inverter systems, the filter volume still dominates the overall inverter volume and thus limits the achievable power density [15].

2) Multi-Level (ML) Inverters

This motivates the use of *Multi-Level (ML)* inverter concepts to further reduce the output filter volume since they offer advantages such as:

- multiple voltage levels at the switch node of ML bridge legs, which helps to more closely approximate the desired sinusoidal output voltage waveform,
- a lower switched voltage of each power semiconductor, resulting in lower switching losses per device, and thus facilitating passive cooling over natural convection,
- the possibility to employ lower voltage power semiconductors, offering an improved device level Figure-of-Merit (FOM) and thus leading to a further increase in system efficiency [16],
- an increased effective switching frequency (f_{eff}, for certain ML topologies)—relevant to output filtering—for a given device switching frequency (e.g., in Flying Capacitor (FC) inverters as shown in **Fig. 1 (a)**).

The main classes of ML inverter topologies are identified as Cascaded H-Bridge (CHB), Neutral-Point Clamped (NPC) and FC inverters [17], which have been studied and compared in literature for various applications [18].

There are also realizations of the same topology with different numbers of levels N for a similar DC link voltage specification, e.g., the FCi operated with an input voltage of 800-1000 V can be found as 3L [19], 5L [20], 7L [21], 9L [22], 10L [23] or even 13L [24] implementation. Naturally, this raises the question about the optimal number of levels of such an ML-FCi. An according analysis was performed by the authors in [25], where efficiency η and power density ρ of a $7.5\,\mathrm{kW}$ IMD have been optimized for the *nominal* operating conditions provided in **Table 1**. Thereby, the lower level counts of $N = 5$ for Si and $N = 4$ for GaN semiconductor technology have been identified as optimal for a simple and idealized FOM-based semiconductor model. For an actual implementation, however, only a limited number of semiconductors with certain discrete blocking voltages, and especially for Si devices low reverse-recovery (Q_{rr}) losses, are available on the market. As a consequence, $N = 7$ for Si and $N = 3$ for GaN are considered for the motor-integrated Multi-Level Flying Capacitor inverter (ML-FCi) discussed here.

3) Short-term Overload Operation Capability

VSDs are exposed to application-specific mission profiles, e.g., servo drive applications include the requirement for providing transient *overload* torques, e.g., during acceleration or braking operation, which exceed the nominal operation torque typically by a factor of two to three for several seconds [26]. This leads to a high transient current stress in the inverter and thus results in high conduction and switching losses respectively, which is especially critical considering the maximum allowed semiconductor junction temperature in combination with the already high ambient operating temperature in the vicinity of the motor.

4) Design and Comparative Evaluation of ML-FCi Systems

In this paper these challenging operating conditions are taken into account for the design of a $7.5\,\mathrm{kW}$ ML-FCi for a motor-integrated inverter, driving a Permanent Magnet Synchronous Motor (PMSM) with a nominal speed of $4500\,\mathrm{rpm}$ and $p = 4$ pole pairs. **Section II** proposes a straightforward and efficient design procedure for a realization with commercially available Si and GaN semiconductors, i.e., as 7L Si FCi and 3L GaN FCi, identifying the most power-dense solution for given boundary conditions like a high short-term overload torque capability (i.e., $i_{\mathrm{out,OL}} = 45\,\mathrm{A}$ phase current amplitude during $3\,\mathrm{s}$) over a broad range of inverter output frequencies f_{out}, i.e., motor rotational speeds, and a $99\,\%$ inverter efficiency during nominal operation (cf. **Table 1**). In **Section III**, the overload capability of the most promising design, i.e., of the 3L GaN FCi, is analyzed in more detail with a transient thermal model. Subsequently, the 3L GaN FCi is realized as a hardware demonstrator and the nominal as well as the thermally critical overload operation are experimentally verified comprehensively. **Section IV** concludes the paper.

II. DESIGN OPTIMIZATION

In order to find the most power-dense realization of the targeted $7.5\,\mathrm{kW}$ IMD, both possible design approaches with a 7L FCi based on Si and a 3L FCi based on GaN semiconductor technology must be optimized and compared. Thereby, the two ML-FCi systems should be dimensioned for the specifications provided in **Table 1** and, in particular, feature a nominal efficiency of 99% and a high short-term overload capability of three times the nominal phase current, i.e., $45\,\mathrm{A}$ peak amplitude, during $3\,\mathrm{s}$.

A. POWER SEMICONDUCTOR SELECTION

In a first step, specific power transistors have to be chosen for the 7L Si FCi and 3L GaN FCi. Thereby, the overload operation capability of the IMD strongly influences the set of feasible devices as the maximum allowed junction temperatures ($175\,^{\circ}\mathrm{C}$ for Si and $150\,^{\circ}\mathrm{C}$ for GaN) must not be exceeded. A straightforward and pragmatic design approach initially considers only the inevitable (temperature-dependent) conduction losses occurring during the short-term overload operation, since they can be quantified easily and allow a quick estimation of the junction temperature.

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TABLE 2: Preliminary semiconductor selection based on the maximum junction temperatures reached during the short-term overload operation ($T_{\mathrm{j,OL,AC}}$ for high output frequencies and $T_{\mathrm{j,OL,DC}}$ for standstill), considering only (temperature dependent) conduction losses and a simple thermal resistance model $R_{\mathrm{th,jhs}}$, assuming a constant baseplate temperature of 100 °C (i.e., excluding semiconductor switching losses and heat spreading in the baseplate).

	Si (200 V, $T_{\mathrm{j,max}}$ = 175 °C)		**GaN** (650 V, $T_{\mathrm{j,max}}$ = 150 °C)	
Device	BSC220N20SFD, 22 mΩ	IPT111N20NFD, 11 mΩ	GS66516-T, 25 mΩ	GS66516-T, 25 mΩ
N_{par}	1	1	1	2
$R_{\mathrm{th,jhs}} = R_{\mathrm{th,jc}} + R_{\mathrm{th,chs}}$	0.7 K/W + 0.75 K/W	0.4 K/W + 0.5 K/W	0.3 K/W + 0.4 K/W	0.3 K/W + 0.4 K/W
$T_{\mathrm{j,OL,AC}}$	127.2 °C	108 °C	118.5 °C	104.2 °C
$T_{\mathrm{j,OL,DC}}$	179 °C	117.1 °C	144.6 °C	108.7 °C

During the short-term overload operation with an AC output voltage (e.g., at 300 Hz inverter output frequency, the current in each switch has an RMS value of $\frac{1}{\sqrt{2}} \cdot \frac{45\,\mathrm{A}}{\sqrt{2}}$, since the total conduction time is, in average, evenly distributed between the High-Side (HS) and the Low-Side (LS) switches in each FCi-Cell [27]. However, e.g., in servo drive applications, it is desired to achieve the overload capability over a large range of inverter output frequencies: the worst-case stress for the semiconductors then occurs during a short-term motor standstill overload (i.e., DC operation with 0 Hz inverter output frequency), where the conduction losses remain evenly distributed between HS and LS of each FC-cell due to an output voltage close to the mid-point voltage (lack of back EMF), but with a significantly higher RMS current per switch of up to $\frac{1}{\sqrt{2}} \cdot 45$ A in the phase carrying the full (DC) overload output current; this corresponds to doubled conduction losses assuming the same on-state resistance (R_{dson}).

In order to estimate the junction temperature, a straightforward thermal model with a single thermal resistance $R_{\mathrm{th,jhs}}$ from the semiconductor junction to the baseplate is used[1]. The baseplate itself is presumed to have a hotspot temperature of 100 °C directly underneath the semiconductor[2] (cf. **Fig. 1**). The adopted temperature difference of $\Delta T = 10\,^{\circ}\mathrm{C}$ between the 90 °C of the motor housing and the hotspot on the baseplate where the semiconductors are mounted accounts for the baseplate's thermal resistance resulting from a practically feasible thickness in the range of several millimeters (cf. **Section II-B4**).

The high currents during overload operation and the resulting high conduction losses in combination with the elevated baseplate temperature motivate the selection of semiconductors with large die areas, i.e., low R_{dson}, and a device package with good cooling capabilities. **Table 2** shows available Si and GaN candidate devices with low R_{dson}. For Si, only devices with low reverse recovery (Q_{rr}) losses in hard-switched applications are considered, resulting in the two bottom-side cooled devices with an R_{dson} of 11 mΩ (IPT111N20NFD [28]) and 22 mΩ (BSC220N20SFD [29]) at 25 °C (both from Infineon). Their respective thermal resistance $R_{\mathrm{th,jhs}}$ is composed of two parts: the junction-to-case thermal resistance $R_{\mathrm{th,jc}}$ provided in the datasheet, and the case-to-heatsink thermal resistance $R_{\mathrm{th,chs}}$, which includes the cooling of the semiconductor package through the Printed Circuit Board (PCB) (with thermal vias and a copper inlay) and a high-performance Thermal Interface Material (TIM) (cf. **Table 4**). $R_{\mathrm{th,chs}}$ was measured for an IPT111N20NFD device in [27] and is scaled up by a factor of 1.5 for the BSC220N20SFD to account for the reduced cooling pad size of the package. For GaN, the top-side cooled device GS66516-T [30] from GaN Systems turns out to be the best-suited device readily available on the market, offering the lowest R_{dson} (25 mΩ at 25 °C) in a package with very good cooling capability. There, $R_{\mathrm{th,jhs}}$ is solely composed of junction-to-case thermal resistance $R_{\mathrm{th,jc}}$ given in the datasheet and the thermal resistance of the TIM (cf. **Table 4**), since no cooling through the PCB is required.

Together with the temperature-dependent R_{dson} provided in the respective datasheets, the minimum losses for each device during AC overload operation (i.e., only conduction losses) can be computed and the ''best-case'' AC junction temperature ($T_{\mathrm{j,OL,AC}}$) obtained. As shown in **Table 2**, all considered semiconductor options remain well below the critical maximum junction temperatures. In contrast, when looking at the standstill overload operation with DC output voltage, the resulting junction temperatures ($T_{\mathrm{j,OL,DC}}$) for the Si 22 mΩ transistor (BSC220N20SFD) and for the GaN option with only one GS66516-T ($N_{\mathrm{par}} = 1$) exceed or are very close to their respective maximum ratings, which leaves no margin for switching losses and/or expected non-ideal heat spreading in the baseplate. This motivates to implement the Si FCi with 11 mΩ semiconductors (IPT111N20NFD) and the GaN FCi with two paralleled GS66516-T devices, which both offer >40 °C junction temperature headroom.

With the power transistors selected, the choice of the switching frequency constitutes the main degree of freedom for the further optimization of the ML-FCi topologies, aiming for maximum power density. Therefore, in the following, first accurate switching loss models for the selected Si and GaN transistors are provided before then discussing the design of the passive components.

[1]This model implies that the periodic loss oscillations from AC output current generation above several tens of Hz are averaged through the thermal capacitances of the semiconductor package [27]. However, the package has a relatively low thermal time constant of several milliseconds to several tens of milliseconds and therefore, during the 3 s overload interval, it reaches its thermal steady state.

[2]This assumption considers ideal heat spreading in the baseplate, which can only be achieved with a very low thermal resistance and/or a very large thermal capacitance allowing to absorb a considerable amount of energy with negligible temperature increase.

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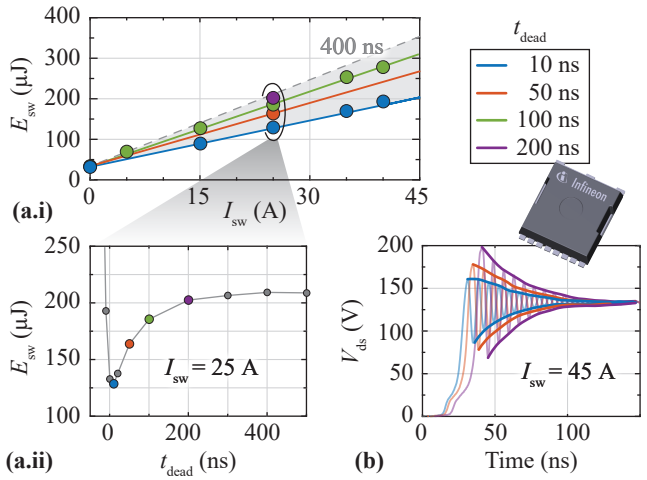

FIGURE 2: (a.i) Calorimetrically measured combined (one turn-on and one turn-off transition) switching losses of the IPT111N20FD at 130 V with $R_{g,on} = 10\,\Omega$ and $R_{g,off} = 0\,\Omega$) and a Gate Driver (GD) supply voltage of +6 V and −3 V. Q_{rr} losses are included in these measurements and depend on the respective dead time. **(a.ii)** Influence of the dead time on the switching losses at 25 A. A steep loss increase is visible for very small dead times because for a brief time interval, an effective short-circuiting of the half-bridge occurs. **(b)** Influence of the dead time on the voltage overshoot during the hard turn-on transition due to the different reverse recovery currents.

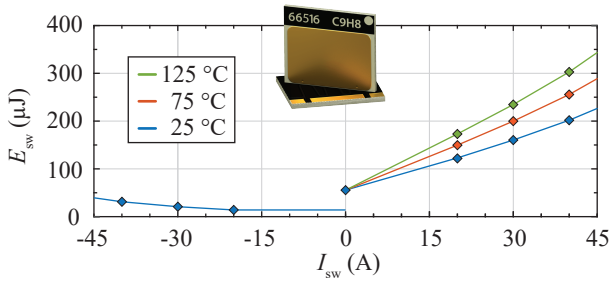

FIGURE 3: HSW and SSW loss energy of the GS66516-T for 400 V provided by the manufacturer. The temperature dependency results from a temperature-dependent transconductance g_m [34].

1) Switching Losses of Si 200 V MOSFET ($N = 7$)

The total switching loss energy (i.e., one turn-on and one turn-off transition) of the IPT111N20NFD are calorimetrically measured in a half-bridge configuration with 130 V DC link voltage, which corresponds to the expected blocking voltage of each cell in the 7L-FCi, and with external turn-on/off gate resistors of $R_{g,on} = 10\,\Omega$ and $R_{g,off} = 0\,\Omega$, respectively (cf. **Fig. 2 (a.i)**). According to measurements of the same device in [31], the Soft Switching (SSW) losses are negligible.

The reverse recovery (Q_{rr}) losses are included in the measured switching losses and can be influenced with the dead time as shown in **Fig. 2 (a.ii)** [32]. For a large deadtime, the resulting switching losses as well as the overshoot of the switch-node voltage increase[3] as shown in **Fig. 2 (b)**. However, for very short dead times, i.e., < 10 ns for 25 A switched current, the half-bridge is effectively shorted for a few nanoseconds, which results in a steep increase in the measured losses. In order to ensure sufficient margin regarding this shorting while minimizing the Q_{rr} losses with limited implementation effort, a fixed dead time of 50 ns is chosen.

The Partial-Hard Switching (PHSW) losses can be considered according to [33] and finally, the total Hard Switching (HSW) losses (including Q_{rr}) are calculated as

$$P_{sw} = f_{sw} \cdot (k_0 + k_1 \cdot I_{sw} + k_2 \cdot I_{sw}^2) \qquad (1)$$

with $k_0 = 31.7\,\mu J$ and the VI-overlap/Q_{rr} loss coefficients $k_1 = 5.3\,\mu J\,A^{-1}$ and $k_2 = 0\,\mu J\,A^{-2}$ extracted from the measurement results[4] shown in **Fig. 2 (a.i)**; these coefficients are valid for 50 ns dead time and $V_{sw} = 130$ V.

2) Switching Losses of GaN 650 V HEMT ($N = 3$)

For a 3L-FCi implementation with GS66516-T devices, the HSW and SSW loss data provided by the manufacturer and shown in **Fig. 3** is used, which includes a temperature dependency as discussed in [34]. The corresponding loss coefficients of (1) for a HSW transition are fitted as $k_0 = 55.2\,\mu J$, $k_1 = 4.8\,\mu J\,A^{-1}$ and $k_2 = 0.037\,\mu J\,A^{-2}$ at a junction temperature of 125 °C, and for a SSW transition as $k_0 = 15.3\,\mu J$, $k_1 = -0.64\,\mu J\,A^{-1}$ and $k_2 = 0.026\,\mu J\,A^{-2}$. A fixed dead time of 100 ns is chosen for the realization, which leads to negligible PHSW losses according to [33], however, at the cost of slightly increased reverse conduction losses above approximately 3 A switched current due to the higher source-drain voltage compared to Si, which results from the absence of a physical body diode.

B. PASSIVE COMPONENTS

With the transistors defined and characterized, the passive components of the ML-FCi remain to be designed/modeled such that the 3L-FCi and 7L-FCi can both be optimized for minimal volume at 99 % nominal target efficiency; the requirement for short-term overload capability must be considered here, too.

1) LC Output Filter Design

The choice of the filter inductance L_{filt} and capacitor value C_{filt} is restricted by the following limits with the specific design values given in **Table 3**:

1) L_{min}: Max. allowed current ripple $\Delta i_{L,pp}$.

[3]For a large dead time, the reverse recovery charge fully accumulates in the pn junction of the MOSFET's body diode and during the hard turn-on of the complementary switch, this charge is extracted via a reverse-recovery current, which results in additional Q_{rr} losses [32] and the correspondingly large reverse-recovery current I_{rr} leads to an increased overshoot of the switch-node voltage. When reducing the dead time, the reverse-recovery charge is not fully accumulated and thus I_{rr} and Q_{rr} losses are reduced, as is the voltage overshoot.

[4]Note that the loss energy k_0 of the IPT111N20NFD, which in theory represents the capacitive switching loss energy occurring for zero switched current I_{sw}, does not strictly coincide with the theoretically expected value $Q_{oss} \cdot V_{sw}$, but instead varies with the utilized $R_{g,on}$. This behavior has already been observed and discussed in [31] and thus, the measured $k_0 = 31.7\,\mu J$ is considered in the subsequent design analysis.

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TABLE 3: Main maximum design parameters for the IMD inverter.

Parameter	Description	Value
$\Delta v_{\mathrm{FC,pp}}$	FC Voltage Ripple (Peak-to-Peak)	13 % of Semiconductor Blocking Voltage
$\Delta i_{\mathrm{L,pp}}$	Inductor Current Ripple	80 % of $i_{\mathrm{out,nom}}$ & $i_{\mathrm{out,OL}}$
$\Delta i_{\mathrm{L,pk,OL}}$	Peak Inductor Current (including Ripple)	64 A
$\Delta v_{\mathrm{out,pp}}$	Output Voltage Ripple	8 V (1 % of V_{DC})
Δv_{L}	Voltage Drop over Inductor at $f_{\mathrm{out,max}}$	83 V (25 % of $v_{\mathrm{out,nom}}$)
Δi_{C}	Reactive Current Amplitude at $f_{\mathrm{out,max}}$	7.5 A (50 % of $i_{\mathrm{out,nom}}$)

2) L_{max}: Max. allowed output voltage drop amplitude v_{L} across L_{filt} at maximum electrical output frequency $f_{\mathrm{out,max}}$.
3) $C_{\mathrm{min,1}}$: Max. allowed voltage ripple $\Delta v_{\mathrm{out,pp}}$ during nominal operation at the output, ultimately defining the output voltage quality.
4) $C_{\mathrm{min,2}}$: Separation by a factor of 5 between the filter resonance frequency f_{LC} and effective switching frequency f_{eff}. Note that this separation also needs to be fulfilled during overload where f_{LC} increases due to the drop in inductance.
5) $C_{\mathrm{max,1}}$: Min. allowed f_{LC} such that the output voltage at $f_{\mathrm{out,max}}$ is not attenuated (separation by factor 5).
6) $C_{\mathrm{max,2}}$: Max. reactive current amplitude i_{C} for $f_{\mathrm{out,max}}$.

The corresponding boundary curves, which define the feasible filter design space [35] (highlighted in red), are visualized in **Fig. 4 (a)**.

Note that in terms of volume, the realization of the filter capacitance is much smaller than the inductor and can thus be neglected. Additionally, for an implementation of C_{filt} with C0G dielectric class I capacitors connected to the DC-link voltage mid-point, negligible losses occur. This motivates the choice of a filter design with minimum inductance L_{filt}.

The frequency of the output current ripple in an ML-FCi can reach several 100 kHz, as the effective switching frequency f_{eff} at the output filter equals $(N-1)$ times the device switching frequency f_{sw} [24]. Therefore, a suitable inductor core material with low HF losses is required, where in addition complete saturation during overload must be avoided. A possible choice of core material is KoolMu HF from Magnetics [36], an iron-based (FeSiAl) powder optimized for low losses at high frequencies. The material features a soft saturation characteristic, i.e., shows a smooth decrease in permeability (inductance) for higher magnetic fields (currents) rather than immediate saturation, i.e., an almost complete loss of the inductance above a certain saturation current, as it is the case with ferrites. This property can be advantageously utilized to design the filter inductor in terms of flux excitation for nominal operation, while during overload a certain drop in inductance is accepted as long as the inductor current peak value $i_{\mathrm{L,pk,OL}}$ does not exceed a certain limit (cf. **Fig. 4 (b)** and **Table 3**).

Additionally, due to the large thermal capacitance of the copper windings and the magnetic core of the filter inductor, only a minor increase in temperature during the short-term overload operation is expected. Thus, the inductor can also thermally be dimensioned for nominal operation, where surface cooling over natural convection is assumed. The maximum allowed inductor temperature is limited to 155 °C by the considered HF litz wires, whereas the KoolMu cores would allow higher temperatures [36]. A TIM thermally couples the core and the winding to improve the cooling of the former during nominal operation and to utilize the thermal capacitance of the core during overload, where mainly the conduction losses are substantially increased and thus cooling of the winding is important. Accordingly, a homogeneous temperature of the core and winding can be expected.

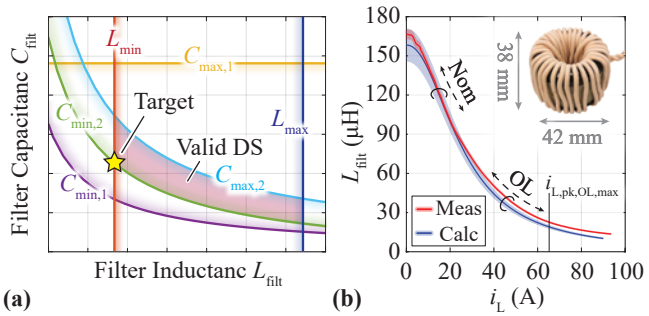

FIGURE 4: (a) Exemplary visualization of the feasible filter Design Space (DS) defined by the boundary curves deduced from the limitations listed in 1)-6). The filter design with minimal inductance is selected (★) since the volume of the inductor dominates the total filter volume. **(b)** Output filter inductance vs. current for a 3L GaN FCi design using an iron powder magnetic core with soft saturation characteristic. Indicated are the maximum overload inductor peak current as well as the nominal and overload operating areas.

For the selected L_{filt} from the presented Design Space (DS), the filter inductor can be dimensioned based on the inductor core material data[5] provided by Magnetics [36] and calculated inductor current waveforms. Thereby, only commercially available toroidal core shapes are considered, which inherently minimize the external magnetic stray field and are thus advantageous for the compact placement in motor-integrated designs (i.e., less critical regarding eddy current losses in close-by metal components and regarding EMI).

2) Flying Capacitor Design

The FCs need to be designed such that a maximum peak-to-peak voltage ripple $\Delta v_{\mathrm{FC,pp}}$ specified in **Table 3** is not exceeded [24], [25] even during overload with three times the nominal current. The optimization considers 450 V X6S capacitors in all FC stages. They feature a superior volumetric capacitance density [25] despite strong decay in capacitance

[5]This type of alloy powder core is not strongly subject to DC-bias dependent losses as it is the case for ferrite [37], [38] and the losses further show only minor temperature dependency [39]. Therefore, the manufacturer data is directly used for the calculation.

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with increasing bias voltage[6]. However, they are only rated up to $105\,^{\circ}\mathrm{C}$ operating temperature. With an estimated thermal resistance of about $80\,\mathrm{K/W}$ per capacitor[7], the expected worst case RMS current in each FC stage of $I_{\mathrm{FC,rms}} = \sqrt{2/(N-1)}\cdot i_{\mathrm{out}}$ [24] and the bias-voltage-dependent Equivalent Series Resistance (ESR) [41], a minimum number of paralleled capacitors for every stage of an N-level ML-FCi is required. This essentially results in two criteria for the FC design, namely a voltage ripple and a thermal limit.

3) High-Frequency DC-Link Capacitor Design

Similarly to the FC design in **Section II-B2** the HF DC-link capacitors are designed for a maximum allowed voltage variation $\Delta v_{\mathrm{DC,pp}}$, which is typically kept in the range of 1% to 2% of the input voltage. For a simple worst-case approximation (i.e., considering a single phase only with no HF-ripple cancellation among the three phases; peak output current during motor standstill, i.e., duty cycles around 0.5) the required minimum capacitance can be approximated with $C_{\mathrm{DC}} = 1/4 \cdot i_{\mathrm{out,OL}}/(f_{\mathrm{sw}} \cdot \Delta v_{\mathrm{DC,pp}})$ [42]. The same $450\,\mathrm{V}$ X6S capacitors are used for the realization as in the FC stages. Thereby, several paralleled capacitors are connected in series to achieve the required blocking voltage of the DC-Link.

4) Heatsink/Baseplate Volume

As already mentioned in **Section I**, the baseplates on which the individual PCBs implementing the phase bridge-legs are placed, are used as heatsink/heat spreader to thermally connect the ML-FCi to the motor housing. The required baseplate volume is calculated assuming that a single FC-cell is mounted on a copper plate, which is laterally attached to the $90\,^{\circ}\mathrm{C}$ motor housing. The width and length of the copper plate are given by the FCi cell dimensions (cf. w_{cell} and l_{cell} in **Fig. 1 (c)**) and the thickness is adjusted to achieve a specified maximum nominal-load temperature rise, with respect to the motor housing, of $\Delta T = 10\,^{\circ}\mathrm{C}$ in the center of the semiconductor mounting area, where the majority of the losses originates (assuming a thermal conductivity of $\lambda_{\mathrm{Cu}} = 394\,\mathrm{W/(m\cdot K)}$). No additional mechanical support structures are considered.

C. OPTIMAL ML-FCI DESIGNS

Considering the 7L Si FCi and the 3L GaN FCi topologies and the respective pre-selected power semiconductors, the loss and volume models of the main components introduced above enable the identification of the switching frequencies that result in the most power-dense realizations under the constraint of an efficiency above $99\,\%$ during nominal operation.

1) Volume Optimization with Constant f_{sw} during Nominal and Overload Operation

In a first approach, the switching frequency is not changed during overload operation, and the resulting designs are hereinafter referred to as ''OLF1'' design (cf. **Fig. 5**). The respective volume distribution (of all three phases) as well as the most important *effective* design parameters, i.e., considering possible parallelization of multiple semiconductor devices, are shown in **Fig. 5 (a.i)** for a Si-based 7L realization and in **Fig. 5 (b.i)** for a GaN-based 3L realization. Thereby, the PCB layout shown in **Fig. 1** is used to estimate the required PCB area of, e.g., GD circuits and signal connections. The FCs (purple in **Fig. 5 (a.i)**) and HF DC-link capacitors (yellow) contribute around $30\,\%$[8] to the total phase volume in the ''OLF1'' design of the 7L Si FCi because they are dimensioned such that the maximum allowed voltage ripple is not exceeded during the short-term overload operation with three times the nominal load current. Consequently, this leads to a low utilization of the capacitors during nominal operation (i.e., results in a lower-than-required voltage ripple).

In **Fig. 5 (a.ii)** and **Fig. 5 (b.ii)** the respective total loss shares of the three-phase inverters during nominal operation is shown, which are dominated by the semiconductor losses with an approximately equal distribution between conduction and switching losses, followed by the total inductor losses. During overload operation the semiconductor conduction losses dominate as expected (cf. **Fig. 5 (a.iii)** and **Fig. 5 (b.iii)** depicting the loss breakdown of one single phase during the worst-case standstill overload).

2) Volume Optimization with Increased f_{sw} during Overload Operation

In order to address the mentioned low utilization of the flying capacitors during nominal operation, the capacitors could instead be designed for the nominal load current. Then, however, a linear increase of the switching frequency with the output current during overload is needed to keep the voltage ripple within specifications [27]: With an increase in switching frequency $(3 \cdot f_{\mathrm{sw,nom}})$ during a simultaneous increase in current $(3 \cdot i_{\mathrm{out,nom}})$, a constant maximum FC voltage ripple can be approximately maintained also during overload. In this way, an overall volume reduction of $24\,\%$ can be achieved for the 7L Si FCi design (cf. ''OLF3'' in **Fig. 5 (a.i)**). This reduction comes at the cost of increased

[6]Consequently, for a certain target capacitance the required number of parallel capacitors increases for higher-voltage FC stages. This also means that further optimizing the lower-voltage FC stages with capacitors rated for lower voltages results in a negligible impact on the total volume.

[7]According to [40], a thermal resistance of approximately $27\,\mathrm{K/W}$ can be expected per similar sized ceramic capacitor (EIA size 2520) if it is placed individually on a PCB without close-by components. Assuming that the capacitors are cooled via their surface area, the total surface area of n capacitors densely placed side by side is about a factor of two lower compared to the same n capacitors placed with sufficient distance to each other. Considering the small thermal margin of $5\,^{\circ}\mathrm{C}$ between the peak baseplate temperature of $100\,^{\circ}\mathrm{C}$ and the rated temperature of the capacitors as well as possible other heat sources nearby, e.g., semiconductors, an additional $50\,\%$ margin is taken into account for the capacitor's thermal resistance R_{th}, which results in about $80\,\mathrm{K/W}$, i.e., allowing losses of $60\,\mathrm{mW}$ per capacitor.

[8]For the physical realization of a DC-supplied drive an additional DC-link energy storage might be required in close connection to the IMD DC input to cover the high power demands during short-term overload operation. Then, in combination with the DC-bus cable inductance (typically in the range of $0.6\,\mu\mathrm{H/m}$ [43]), a resonance can be excited, which needs to be limited by over-voltage protection circuitry and/or a local damping network. A more detailed analysis of this arrangement exceeds the scope of this paper.

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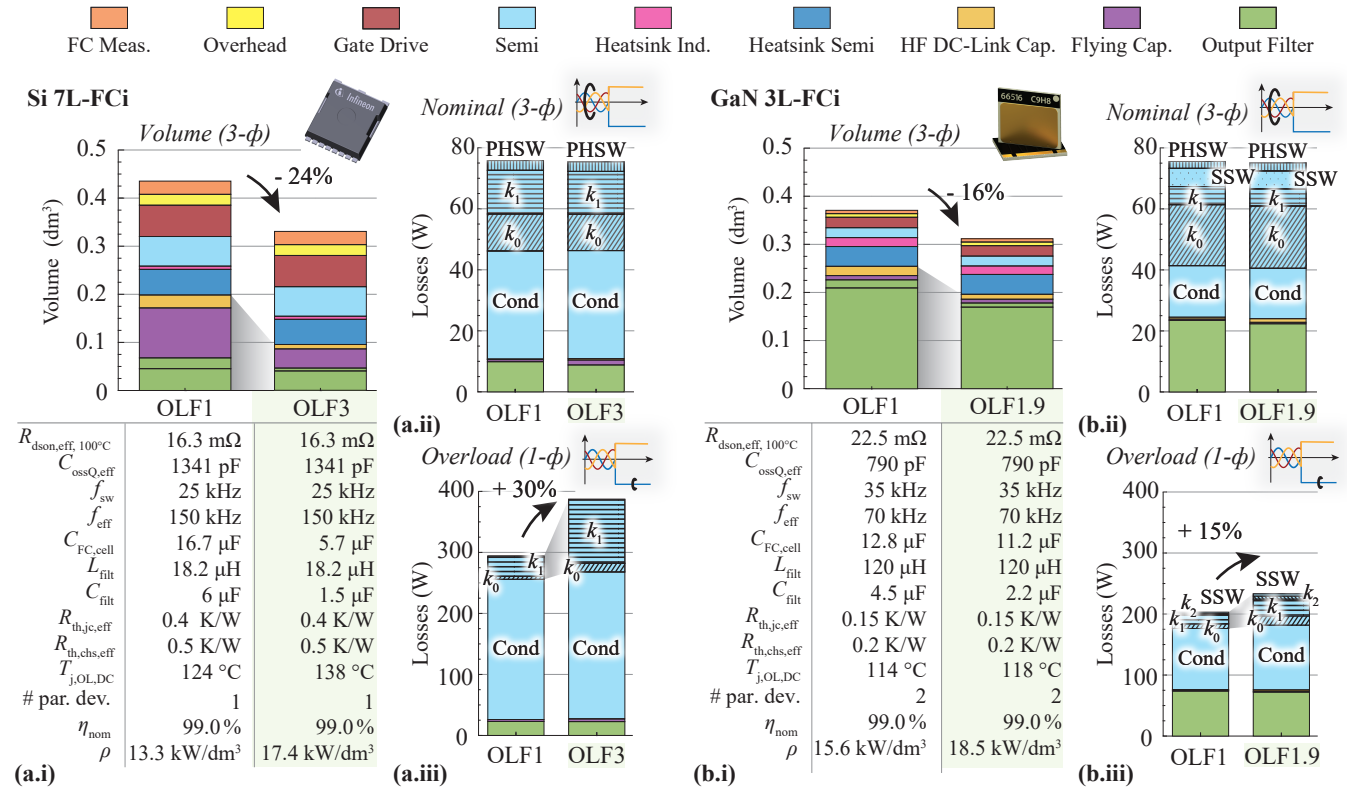

	Si 7L-FCi OLF1	Si 7L-FCi OLF3	GaN 3L-FCi OLF1	GaN 3L-FCi OLF1.9
$R_{\text{dson,eff, 100°C}}$	16.3 mΩ	16.3 mΩ	22.5 mΩ	22.5 mΩ
$C_{\text{ossQ,eff}}$	1341 pF	1341 pF	790 pF	790 pF
f_{sw}	25 kHz	25 kHz	35 kHz	35 kHz
f_{eff}	150 kHz	150 kHz	70 kHz	70 kHz
$C_{\text{FC,cell}}$	16.7 µF	5.7 µF	12.8 µF	11.2 µF
L_{filt}	18.2 µH	18.2 µH	120 µH	120 µH
C_{filt}	6 µF	1.5 µF	4.5 µF	2.2 µF
$R_{\text{th,jc,eff}}$	0.4 K/W	0.4 K/W	0.15 K/W	0.15 K/W
$R_{\text{th,chs,eff}}$	0.5 K/W	0.5 K/W	0.2 K/W	0.2 K/W
$T_{\text{j,OL,DC}}$	124 °C	138 °C	114 °C	118 °C
# par. dev.	1	1	2	2
η_{nom}	99.0 %	99.0 %	99.0 %	99.0 %
ρ	13.3 kW/dm³	17.4 kW/dm³	15.6 kW/dm³	18.5 kW/dm³

FIGURE 5: (a.i) & **(b.i)** Volume distribution of the resulting designs for the 7L-FCi implemented with Si (IPT111N20NFD) and for the 3L-FCi implemented with GaN power semiconductors (two paralleled GS66516-T), including the most important design parameters given below for comparison. Thereby, the designs labeled with "OLF1", assume the same switching frequency in nominal as in overload operation, while in "OLF3", the switching frequency is increased during overload by a factor of 3 for Si and in "OLF1.9" by a factor of 1.9 for GaN in order to ensure a low converter volume. **(a.ii)** & **(b.ii)** Loss breakup of the nominal operation of all three phases. **(a.iii)** & **(b.iii)** Distribution of the losses during the worst-case standstill overload operation (0 Hz inverter output frequency) of the single phase with full 45 A current is shown.

switching losses during overload operation, which is visible in **Fig. 5 (a.iii)**. The increase in switching losses results in a higher junction temperature[9] $T_{\text{j,OL,DC}}$, which, however, is still below the maximum allowed operating temperature (calculated based on the simple thermal model $R_{\text{th,jhs}}$ of **Table 2** ignoring finite heat spreading in the baseplate).

Similarly, for the 3L GaN FCi the increase in f_{sw} during overload results in a reduction of the FC and HF DC-link capacitor volume but the reduction is limited by the minimum required number of parallel capacitors discussed in **Section II-B2** (thermal limitation rather than voltage ripple limitation). However, the inductor filter volume is reduced as the increase of f_{sw} during overload helps to ensure that despite the drop in inductance during overload operation (soft permeable core material), the inductor current never exceeds the peak value of 64 A defined in **Section II-B1**. Consequently, a core with less core material and a stronger drop in inductance over current is allowed (while maintaining the same inductance value during nominal operation as in "OLF1"). Note that in contrast to the 3L-FCi, the inductor design of the 7L did not change noticeably when the switching frequency increase was introduced, as the core size is thermally limited. Additionally, an increase of f_{sw} helps to maintain a certain ratio $f_{\text{eff}}/f_{\text{LC}}$ in order to not excite the filter resonance, which could be possible due to the increase in f_{LC} resulting from the decrease of the effective filter inductance. All in all, increasing the switching frequency up to $1.9 \cdot f_{\text{sw,nom}}$ during overload reduces the total volume of the 3L GaN FCi by 16 % at the cost of increased overload losses (cf. "OLF1.9" in **Fig. 5 (b.i)** and **Fig. 5 (b.iii)**) and increased worst-case junction temperature $T_{\text{j,OL,DC}}$ (again below the maximum allowed value). Note that the f_{sw} only has to be increased by a factor of 1.9 instead of factor 3 found for the 7L Si FCi realization, since in the 3L GaN design the minimum number of FCs is thermally limited, i.e., regarding the allowed voltage ripple, they are over-dimensioned for normal operation. The situation is similar with the inductor design: An increase by factor 1.9 already keeps the inductor from exceeding the peak value of 64 A and prevents a potential resonance excitation of the filter.

[9]Note that contrary to the conduction losses (and also contrary to the switching losses during AC operation) the majority of the switching losses in DC overload occur, e.g., in the LS switches of the FCi. Consequently, their $T_{\text{j,OL,DC}}$ exceeds the one of the HS switches and is referenced here.

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3) Design Selection for Demonstrator Realization

The final expected power densities[10] and efficiencies of the 7L Si and 3L GaN FCi realizations are comparable according to **Fig. 5 (a.i)** and **(b.i)** (column "OLF3" and "OLF1.9" highlighted in green), but for Si a much higher complexity in terms of number of switches, GDs, control signals and FC voltage measurement circuits results. This clearly motivates pursuing the 3L GaN FCi (with an increase in switching frequency of 1.9 during overload) for the further analysis and ultimately the realization of a demonstrator system.

III. 3L GAN FCI HARDWARE DEMONSTRATOR

So far, the overload junction temperature has only been estimated with a simple thermal model facilitating a straightforward design process, which, however, does not include, e.g., finite heat spreading in the baseplate resulting in a hotspot temperature potentially exceeding the previously assumed $100\,^{\circ}\mathrm{C}$. Aiming for a hardware realization, it is therefore necessary to first analyze the chosen 3L GaN FCi design with an extended thermal model to evaluate which overload torque (i.e., which output current) can be delivered for various inverter output frequencies (i.e., motor rotational speeds). Subsequently, in order to show that the chosen design process and the resulting 3L GaN FCi meets the specifications of $99\,\%$ efficiency during nominal load operation as well as the thermally challenging short-time overload operation, a hardware demonstrator of the 3L GaN FCi is built and its performance is experimentally verified.

A. ACHIEVABLE OVERLOAD TORQUE PREDICTION WITH AN ACCURATE TRANSIENT THERMAL MODEL

The achievable short-term overload torque (maximum overload current) is limited by the allowed semiconductor junction temperature $T_{\mathrm{j,OL}}$. By using an accurate dynamic/transient thermal model of the semiconductor arrangement in the 3L GaN FCi, the junction temperature (and therefore the maximum overload torque) can be accurately estimated for different output frequencies (DC up to $f_{\mathrm{out,max}}$) of the inverter. Said thermal model can be obtained by combining a thermal model of the heat spreading in the baseplate extracted from Finite Element Method (FEM) thermal simulations with a thermal model of the semiconductor package provided by the manufacturer.

1) Thermal FEM Simulation of Heat Spreading

In the FEM simulations, the physical transistor arrangement of the 3L GaN FCi shown in **Fig. 6 (a.i)** is simplified by merging all HS and all LS semiconductors into two loss input areas, respectively ($T_{\mathrm{HS,m}}$ and $T_{\mathrm{LS,m}}$; the areas correspond to the total area of the four HS and the four LS semiconductors). For mechanical stability reasons, the baseplate is realized with $7\,\mathrm{mm}$ thick aluminum (AlMgSi, with thermal conductivity $\lambda_{\mathrm{Al}} \approx 200\,\mathrm{W/(m \cdot K)}$ instead of copper, where the thickness

[10]Includes 30% additional air volume expected from the realization.

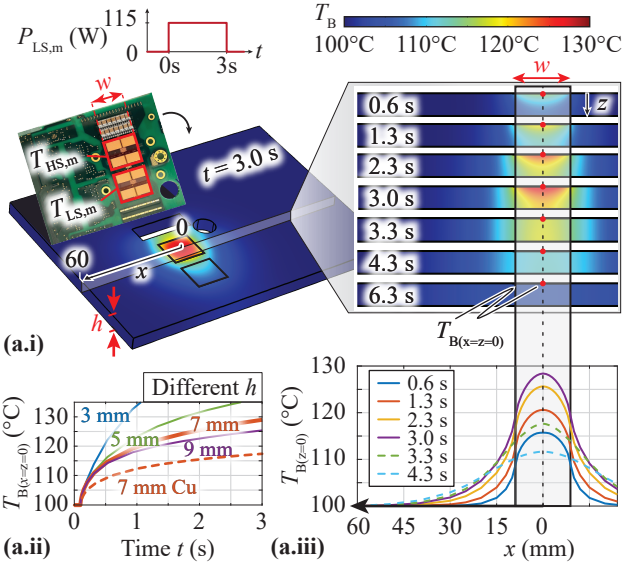

FIGURE 6: (a.i) FEM simulation of the heat spreading in the $7\,\mathrm{mm}$ thick aluminum baseplate during $3\,\mathrm{s}$ standstill overload operation. Considering the similar losses of all HS switches and all LS switches, respectively, the four HS and four LS switches are simplified into one chip area each ($T_{\mathrm{HS,m}}$ and $T_{\mathrm{LS,m}}$). The thermal coupling between the HS and LS area has only a minor influence on the peak temperature during the $3\,\mathrm{s}$ period. With the chosen output current direction, hard-switching occurs in the LS switches, which leads to peak losses of $P_{\mathrm{LS,m}} = 115\,\mathrm{W}$ dissipated from $T_{\mathrm{LS,m}}$. **(a.ii)** Influence of the baseplate thickness h on the peak temperature in the center of the chip area $T_{\mathrm{B}(x=z=0)}$. In the current realization, a baseplate thickness of $h = 7\,\mathrm{mm}$ is implemented and is also considered in the further thermal analysis. **(a.iii)** Heat spreading in the aluminum baseplate over time and position during the $3\,\mathrm{s}$ overload.

compared to an equivalent copper baseplate is doubled in order to account for the lower thermal conductivity.

The simulation clearly visualizes the limited transient heat spreading during an exemplary standstill overload, where a total power of about $P_{\mathrm{LS,m}} = 115\,\mathrm{W}$ must be dissipated from the hard-switched semiconductors (the low-side transistors $T_{\mathrm{LS,m}}$ for negative i_{out}). It was verified that the power dissipated from the soft-switched semiconductor area ($P_{\mathrm{HS,m}} = 52\,\mathrm{W}$ in $T_{\mathrm{HS,m}}$) can be neglected due to the weak thermal coupling of the two heat sources during the $3\,\mathrm{s}$ overload. As visible in **Fig. 6 (a.iii)** the local hot spot temperature just below the semiconductor area is expected to be $127\,^{\circ}\mathrm{C}$, whereas already at a small distance x away from the center, the temperature decays relatively quickly down to $T_{\mathrm{B(z=0)}}(x) = 100\,^{\circ}\mathrm{C}$.

A further increase in thickness of the baseplate (BP) above the current $7\,\mathrm{mm}$ would not lead to a significant reduction of the peak temperature after $3\,\mathrm{s}$ according to **Fig. 6 (a.ii)**, where the local hot-spot temperature $T_{\mathrm{B}(x=z=0)}$ (indicated with red dots in **Fig. 6 (a.i)**) over time for different baseplate thicknesses h is analyzed. In case the $7\,\mathrm{mm}$ thick aluminum baseplate is replaced with a $7\,\mathrm{mm}$ thick copper baseplate (red dashed line in **Fig. 6 (a.ii)**), which features about 1.5 times

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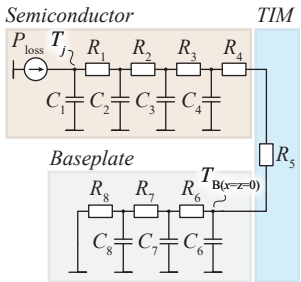
TABLE 4: Thermal Interface Material.

TIM Name	Thermal Conductivity	Pressed Thickness
TG-A1780 [45]	$17.8\,\mathrm{W/(m\cdot K)}$	$0.3\,\mathrm{mm}$



R_{th}	K/W	C_{th}	J/K
R_1	0.008	C_1	$1.48\cdot10^{-4}$
R_2	0.124	C_2	$1.37\cdot10^{-3}$
R_3	0.13	C_3	$12\cdot10^{-3}$
R_4	0.008	C_4	$3.7\cdot10^{-3}$
R_5	0.37		
R_6	0.16	C_6	0.24
R_7	0.4	C_7	0.93
R_8	1.024	C_8	5.05

FIGURE 7: Dynamic thermal model describing the junction temperature T_j increase of a single semiconductor device during the 3 s overload operation. It includes the thermal model of the GS66516-T provided by the manufacturer, an electrically insulating TIM (cf. Table 4) and a thermal model describing the hot-spot temperature $T_{B(x=z=0)}$ in the aluminum baseplate extracted from Fig. 6 (a.ii).

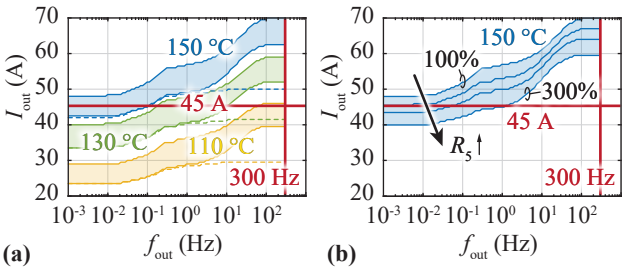


FIGURE 8: **(a)** Achievable short-term overload current versus output frequency for different $T_{j,OL}$ limits (110 °C, 130 °C and 150 °C). For each $T_{j,OL}$ a higher and lower limit of output current is given, where the lower limit includes several nonidealities such as increased switching losses due to slower switching transients and parasitic capacitances, increased conduction losses due to dynamic R_{dson}, and a worse performance of the TIM. The dashed lines indicate the lower current limit if instead of the transient thermal model of the semiconductor package simply the steady-state thermal resistance ($R_1+\ldots+R_4$ of Fig. 7) would be considered. **(b)** Achievable output currents over output frequency for $T_{j,OL} = 150\,°C$ when only the performance of the TIM is reduced (i.e., R_5 is increased from its best-case value in Fig. 7 to up to +200%).

the thermal capacitance (for the same volume) and roughly twice the thermal conductivity compared to aluminum, the increase in $T_{B(x=z=0)}$ after the 3 s overload could be reduced by 40 % to 117 °C. An even lower hotspot temperature could be achieved with the use of two-phase heat exchangers such as vapor chambers, which show substantially better heat spreading capabilities compared to copper [44].

In any case, as expected, the assumption of a homogeneous baseplate temperature during the whole overload duration, i.e., near-perfect heat spreading, can only be used as a first approximation to eliminate clearly physically impossible designs, but cannot predict the junction temperature accurately. Note that the losses during nominal operation are small due to the 99 % efficiency target, and thus no critical local hot-spot temperature occurs; Consequently, in contrast to the overload operation, the assumption of a 100 °C baseplate temperature below the semiconductors remains valid for nominal load.

2) Transient Thermal Model

The required dynamic/transient thermal model of the semiconductor arrangement in the 3L GaN FCi can be represented by a Cauer model with several thermal *RC* stages (cf. **Fig. 7**). Thereby, the Cauer model of the GaN transistor itself (GS66516-T, highlighted in brown) is provided by the manufacturer. The thermal resistance of the TIM (R_5, highlighted in blue) is determined based on the material's thermal conductivity (cf. **Table 4**) and on the physical dimensions of the transistor (cooling pad area of $17.8\,\mathrm{mm}\times5.7\,\mathrm{mm}$). Finally, the Cauer coefficients for the three thermal RC stages describing the local hot-spot temperature $T_{B(x=z=0)}$ of the 7 mm thick aluminum baseplate during overload ($R_6C_6\ldots R_8C_8$, highlighted in grey) are derived from the FEM-simulated step response in **Fig. 6 (a.ii)**.

3) Achievable Overload Torque

Fig. 8 (a) shows the resulting maximum allowed short-term overload output current amplitude for different maximum junction temperatures $T_{j,OL}$ over varying inverter output frequency f_{out} between DC and $f_{out,max}$. For each $T_{j,OL}$ a lower and upper current limit is shown, where the upper output current limits are derived from the loss calculations of **Section II-A2** and the accurate transient thermal model of **Fig. 7**. In order to account for possible nonidealities expected in the thermal setup and/or inaccuracies in the model, lower output current limits are calculated based on the following assumptions:

- 20 % lower thermal conductivity of the TIM compared to the datasheet specification, combined with a 30 % increased final pressed thickness, resulting in $R_5 = 0.6\,\mathrm{K/W}$.
- 20 % increased capacitive switching losses to account for additional parasitic switch-node capacitances, i.e., $k_0' = 1.2\cdot k_0$, cf. (1).
- 20 % lower switching speed increasing the VI-overlap losses, i.e, $k_1' = 1.2\cdot k_1$ and $k_2' = 1.2\cdot k_2$, cf. (1).
- 30 % increase of the on-state resistance R_{dson} due to charge trapping effects (dynamic R_{dson}) known to occur in GaN HEMTs [34] in addition to the pronounced temperature dependency, i.e., $R'_{dson,eff,T_j} = R_{dson,T_j} + 0.3\cdot R_{dson,25°C}$.

From the resulting lower current limits one can conclude that the full overload current (i.e., 45 A) is nearly reached at standstill at a maximum junction temperature of $T_{j,OL} = 150\,°C$ (lower line of the blue area in **Fig. 8 (a)**). An increase of the output frequency to 0.1 Hz (i.e., 1.5 rpm for a PMSM with 4 pole pairs) allows the operation of the system with full overload current amplitude thanks to reduced average losses and the overall thermal capacitance of the setup (in particular the thermal capacitances $C_6\ldots C_8$ of the baseplate). At

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higher output frequencies, the thermal capacitances of the semiconductor package become more influential. This can be clearly seen when they are omitted, i.e., the semiconductor package is only modeled with a total thermal resistance $R_{\mathrm{th,jc,tot}} = R_1 + \ldots R_4$ without thermal capacitances. This leads to a significantly lower overload output current capability at high output frequencies (dashed lines in **Fig. 8 (a)**, only drawn for the lower current limits). Therefore, a certain thermal capacitance close to the heat source is clearly advantageous.

The influence of, e.g., assembly tolerances on the IMD overload performance, can be seen in **Fig. 8 (b)**, where the thermal resistance of the TIM (R_5) is increased by +50%, +100% and +200% compared to the initial best-case scenario given in **Fig. 7** (corresponding to 100 %). For example, an increase of +50% is approximately reached if the TIM is only pressed to a thickness of 0.35 mm instead of 0.3 mm during the assembly of the inverter on the baseplate, while its thermal conductivity is simultaneously about 20% lower than specified in ideal datasheet values. Such tolerances are typically present in practice and have a significant impact on the achievable overload torque.

All in all, especially in industrial applications, it is preferred not to design the system close to the maximum temperature ratings, such that during operation the maximum junction temperatures of, e.g., the semiconductors are well below their temperature limits despite various tolerances[11], which increases their lifetime considerably [46]. In the case at hand, if a maximum junction temperature of 130 °C is selected, the full overload torque can still be safely provided for output frequencies above 10 Hz (i.e., 150 rpm) with this setup, while for DC operation still about twice the nominal torque is possible.

B. HARDWARE PROTOTYPE

Following a phase-modular system approach as described in **Section I**, the power hardware including GDs and measurement circuits of each phase is implemented on a single PCB with a shape defined by the motor housing. This phase module PCB is then placed on an aluminum baseplate, which is thermally connected to the motor housing and, therefore, acts as heatsink. Due to the low complexity of the 3L GaN design, only a part of the total available PCB area is required. As previously shown in **Fig. 1** the control hardware as well as (additional) DC link capacitors are placed on two separate boards, which laterally connect the PCBs implementing the bridge-legs / phase modules together.

Fig. 9 (a.i) and **(a.ii)** show the top view of a single phase module of the 3L GaN FCi with the most relevant components labeled. Furthermore, the employed components are summarized in **Table 5**. The top-side cooled power semiconductors

[11]For example, the motor case temperature could slightly increase above 90 °C and/or the distribution of switching losses between the two parallel devices could be unbalanced due to variations in gate threshold voltage and gate loop inductance, leading to a higher junction temperature than expected from the scenarios considered above.

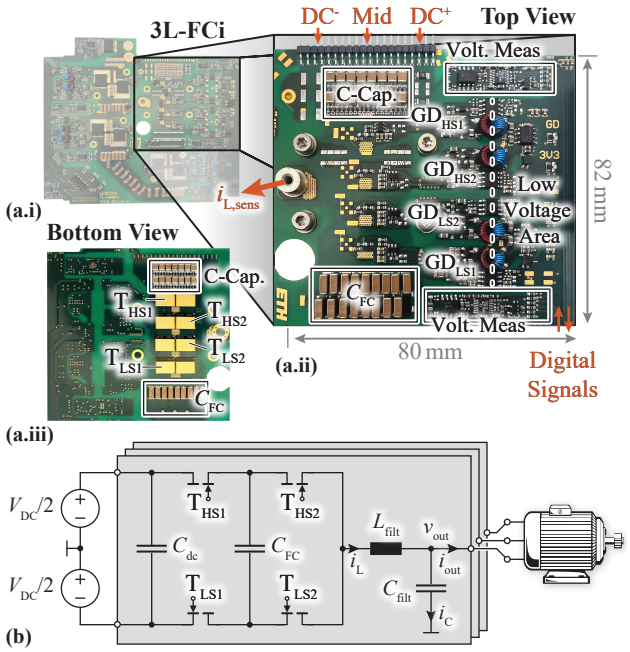

FIGURE 9: (a.i) Implemented phase module of the 3L GaN FCi hardware prototype. The most important components are labeled in the top **(a.ii)** and bottom view **(a.iii)**. **(b)** Circuit of the phase module.

TABLE 5: Main power components and operation parameters of the realized 3L GaN hardware demonstrator shown in **Fig. 9** and its filter inductor shown in **Fig. 4 (b)**. Quantities are given for a single phase module.

Component	Value	Details
Transistors	12.5 mΩ	GaN Systems GS66516T (650 V, 25 mΩ; 2 x parallel per position)
	35 kHz	$f_{\mathrm{sw,nom}}$
	67 kHz	$f_{\mathrm{sw,OL}}$ ($= 1.9 \cdot f_{\mathrm{sw,nom}}$)
Gate Driver (GD)		Infineon 1EDN7511B
GD Insulator		Analog Devices ADuM121N
C_{fc}	11.2 µF	26 x C5750X6S2W225K250KA (X6S, 2.2 µF, 450 V)
L_{filt}	120 µH	Magnetics Powder Core 0076076A7, 3x stacked per inductor, 32 turns of litz wire with 630 strands
C_{filt}	2.2 µF	22 x CGA9Q4NP02W104J280KA (NP0, 100 nF, 450 V)
Current Sensor		Allegro ACS733KLATR-65AB-T
OpAmp Volt. Meas.		Analog Devices LTC6362
ADC		Analog Devices LTC2311-12

are placed on the bottom side (cf. **Fig. 9 (a.iii)**) of the PCB and are electrically isolated with the high-performance TIM given in **Table 4**. Multiple screw holes placed close to the individual semiconductors together with the soft TIM facilitate a uniformly distributed mounting pressure despite the thin (1 mm) PCB. Since the dimensions of the PCB as well as of the baseplate are defined by the motor housing, for a fair comparison of the power density with the calculated results shown in **Fig. 5**, only the dimensions of the populated area of the PCB (80 mm × 82 mm) according to **Fig. 9 (a.ii)** and the realized toroidal filter inductor volume (120 µH nominal, cf.

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Fig. 4 (b)) are considered. The same holds for the baseplate, whose thickness is chosen based on the assumptions detailed in **Section II-B4**. With these considerations, the power density of the hardware demonstrator is about $19.5\,\mathrm{kW/dm^3}$, which closely matches the calculated value of $18.5\,\mathrm{kW/dm^3}$ (cf. **Fig. 5 (a.ii)**).

In order to minimize the VI-overlap losses, fast switching transients (i.e., high $\mathrm{d}v/\mathrm{d}t$, cf. (1)) are necessary, which requires low-inductive power and gate loop designs. Additionally, as each switch of the 3L GaN FCi is implemented with two parallel devices, a good symmetry in the power and gate loop path is essential such that simultaneous switching is achieved to evenly distribute the current and the resulting losses among the paralleled semiconductors. To this end, a symmetric co-planar power loop layout is arranged on the six-layer power PCB. Note that due to the low-inductive power loop design, no additional commutation capacitors are required for the inner commutation loop formed by T_{HS2}, T_{LS2} and the FCs (cf. **Fig. 9 (b)**). The outer power commutation loop consisting of T_{HS1}, T_{LS1}, the FCs and the DC link capacitors, which are placed on a separate DC link board connected via pin headers, has a larger loop inductance and thus requires the placement of additional commutation capacitors on the power board directly next to the semiconductors (cf. "C-Cap." in **Fig. 9 (a.ii)** and **(a.iii)**). The symmetric gate loop is realized with a non-isolated GD integrated circuit (1EDN7511B from Infineon [47]) placed directly over the power transistors on the top layer of the PCB, while mandatory signal isolation as well as the galvanically isolated bipolar supply for the GD ($+6\,\mathrm{V}$ and $-3\,\mathrm{V}$) are placed outside of the power-loop area. This prevents any overlap of fast fluctuating voltage potentials, i.e., voltage steps with logic nets connected to the control board, which would cause undesired CM currents over parasitic capacitances that could lead to errors in the gate and/or measurement signals.

C. EXPERIMENTAL PERFORMANCE VERIFICATION

For the experimental verification, a phase module of the 3L GaN FCi is operated in open-loop, i.e., without active (closed-loop) output current control, however, the FC voltages are actively balanced with a simple closed-loop proportional controller by means of slight adjustments to the individual switching cells' duty cycles [48]. The aluminum baseplate (BP) on which the 3L-FCi is mounted for the measurements is heated to the target operation temperature of $100\,^{\circ}\mathrm{C}$. Similarly, the inductor is heated by a hot plate to reach the nominal surface temperature of $135\,^{\circ}\mathrm{C}$ as determined from its thermal model.

1) Efficiency and Loss Distribution in Nominal Operation at 100°C Baseplate Temperature

Electrical efficiency measurements for a resistive load are performed with a Yokogawa WT3000 precision power analyzer [49], which according to a comparison with calorimetric efficiency measurements published in [50] achieves very accurate measurement results for systems in the $2\,\mathrm{kW} - 10\,\mathrm{kW}$ power range with efficiencies $> 99\,\%$.

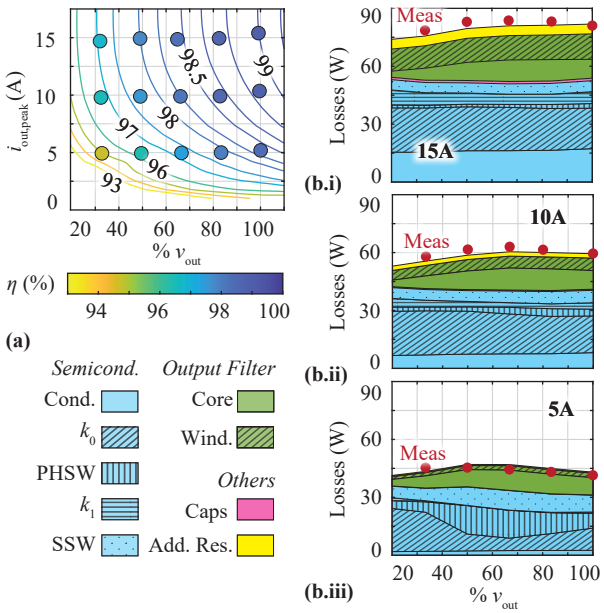

FIGURE 10: (a) Measured (dots) and calculated (lines) efficiencies for different output powers (nominal and partial load operation) with varying output current amplitudes and a baseplate temperature of $100\,^{\circ}\mathrm{C}$. Partial load operation is achieved by linearly reducing the output voltage amplitude as well as the fundamental frequency, corresponding to an operation with a constant ratio V/f (V/f-control based operation). **(b.i)-(b.iii)** Measured total losses and calculated loss breakdown for the considered output current amplitudes for nominal and partial load operation, clearly highlighting the dominant contribution of the semiconductor switching losses.

The measured and calculated efficiencies for nominal operation and several part load scenarios are given in **Fig. 10 (a)**. The nominal operating point is defined according to **Table 1** as $7.5\,\mathrm{kW}$ for a three-phase system, with a peak output current amplitude of $15\,\mathrm{A}$ at $300\,\mathrm{Hz}$ output frequency resulting in a peak output voltage amplitude of $v_{\mathrm{out,nom}} = 330\,\mathrm{V}$ ($100\,\%\,v_{\mathrm{out}}$ in **Fig. 10**). Partial load operation is tested with a fixed output current amplitude and a gradually decreasing output voltage to decrease output power. At the same time, the output frequency is decreased such that a constant ratio of voltage to frequency remains (resembling a V/f-controlled drive system [51]). This corresponds to the practically relevant application scenario where a certain constant torque at reduced rotational speed has to be provided. In the nominal operating point an efficiency of $98.94\,\%$ is measured, which compared to the anticipated $99\,\%$ corresponds to only $1.5\,\mathrm{W}$ of additional losses per phase module. As can be observed in the calculated loss breakdown of **Fig. 10 (b.i)-(b.iii)**, which are obtained with the loss models of **Section II**, the loss discrepancy could be explained with additional ohmic losses (yellow section) originating from a $15\,\mathrm{m\Omega}$ resistance, which could be attributed to, e.g., the contribution of connectors, PCB tracks and the current sensor. At nominal output current (cf. **Fig. 10 (b.i)**) the losses are dominated by the semiconductor conduction (Cond.) and capacitive switching losses

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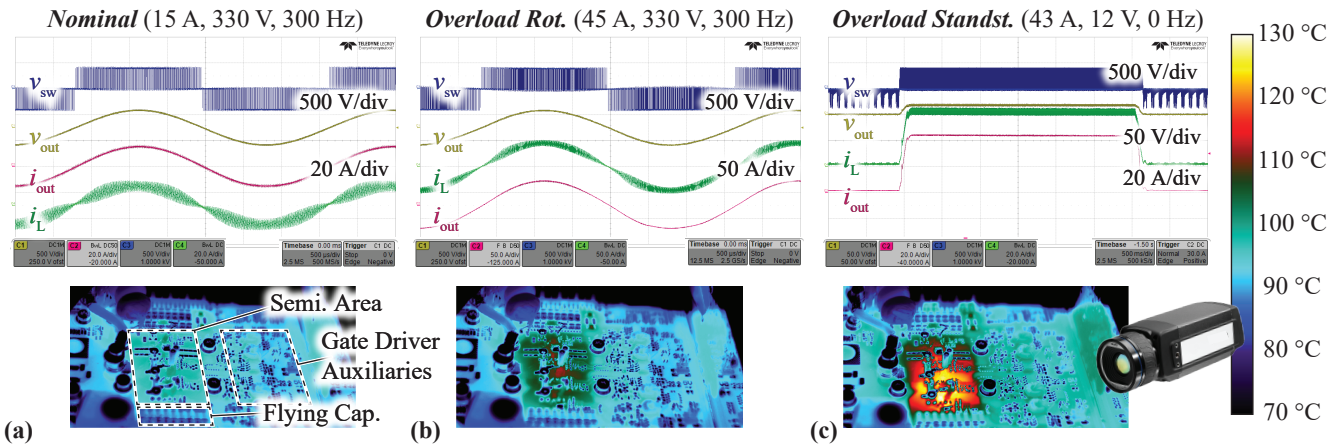

FIGURE 11: Measured waveforms of the switch-node voltage v_{sw}, filtered output voltage v_{out}, inductor current i_{L} and the filtered output current i_{out} during **(a)** nominal load operation, **(b)** overload operation with maximum output frequency (AC overload) and **(c)** standstill overload operation (DC overload), all for $100\,^{\circ}\mathrm{C}$ baseplate temperature. Additionally, the respective thermal images taken with a high-resolution infrared camera (FLIR A655sc) are displayed to qualitatively show the thermal stress during the different operating modes.

(k_0) losses. The slight change in losses with output voltage is explained with the varying average current ripple depending on the modulation depth (i.e., output voltage amplitude), which in turn impacts the switching losses as well as the HF inductor core losses. A higher inductor current ripple reduces the VI-overlap losses (k_1) but increases the SSW losses. For lower output currents (cf. **Fig. 10 (b.ii)** and **(b.iii)**), the higher relative current ripple increases the number of SSW (or PHSW) transitions and thus increases the SSW (or PHSW) loss contribution and reduces the HSW losses (k_0, k_1). In contrast to the semiconductor losses, the contribution of the output filter core losses increases for a higher current ripple (and thus for higher flux density ripple ΔB) following the loss modeling data provided by the manufacturer based on Steinmetz parameters. At the same time, the conduction losses of the output filter windings (Wind.) and also of the semiconductors increase due to a higher RMS current but compared to the overall losses the influence is negligible.

Fig. 11 (a) shows measured waveforms during nominal operation with the characteristic 3L switch node voltage v_{sw} in blue and the inductor current i_{L} in green. The latter has its maximum ripple at $\pm 200\,\mathrm{V}$ output voltage (i.e., 0.25 or 0.75 duty cycle). Due to the output filter, the filtered output voltage (v_{out}, yellow) and output current (i_{out}, magenta) only show negligible distortions.

A thermal image of the PCB's top side, taken with a high-resolution infrared camera (FLIR A655sc [52]), shows equal temperature distribution over the entire board during nominal operation with $100\,^{\circ}\mathrm{C}$ baseplate temperature, which is expected due to the high system efficiency. The semiconductors cannot be directly monitored with the thermal camera, as they are placed on the bottom side of the PCB and are pressed to the aluminum baseplate for cooling. Thus, only the transferred heat through the PCB and vias is visible. Nonetheless, based on the thermal models, T_{j} is expected to be only $2\,^{\circ}\mathrm{C} - 3\,^{\circ}\mathrm{C}$ above the baseplate temperature.

2) Overload Operation at 100°C Baseplate Temperature

The waveforms for short-term overload output currents with and without spinning rotor are given in **Fig. 11 (b)** and **Fig. 11 (c)**, respectively. As soon as the output current exceeds the nominal value of $15\,\mathrm{A}$, the switching frequency is linearly increased with the output current up to a factor of 1.9 at $45\,\mathrm{A}$ as discussed in **Section II-C2**. Contrary to nominal operation, a local increase in temperature around the semiconductor area can be observed during the short-term overload with spinning rotor and even more pronounced for overload at standstill with almost full overload torque, which qualitatively shows the thermal stress caused by the overload losses. Electrical loss measurements show good matching of the losses during standstill overload operation with the respective calculations for $43\,\mathrm{A}$ phase current (measured: $255\,\mathrm{W}$, calculated: $233\,\mathrm{W}$, i.e., $< 10\,\%$ error) when the additional $15\,\mathrm{m\Omega}$ for connectors and traces are considered.

IV. CONCLUSION

In this paper, a phase modular Integrated Motor Drive (IMD) fed by an $800\,\mathrm{V}$ DC link for a $7.5\,\mathrm{kW}$ industrial servo drive application is designed and implemented based on typical specifications. Thereby, the high temperatures close to the motor of around $90\,^{\circ}\mathrm{C}$ are challenging regarding the thermal design, especially when considering the required short-term overload capability of three times the nominal current (i.e., $45\,\mathrm{A}$ phase current amplitude during $3\,\mathrm{s}$).

Aiming for the most compact realization, first, two topology candidates with LC output filters, a 3L Flying Capacitor inverter (FCi) based on GaN and a 7L FCi based on Si power semiconductor technology, are evaluated and compared. The inverter volumes are minimized by allowing an increase in switching frequency during overload operation as it allows to dimension the flying capacitors and the output filter, which is implemented with a soft-permeable inductor core material, mainly for nominal operation as long as thermal limitations during overload operation are respected. Since both, the 3L

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GaN FCi and 7L Si FCi, promise similar power densities the significantly less complex 3L GaN topology is selected for the realization of a hardware demonstrator. First, a transient thermal model that includes also the heat spreading below the semiconductors in the baseplate is proposed for estimating the achievable overload torque (i.e., max overload current) for given maximum semiconductor junction temperatures, various inverter output frequencies (i.e., various motor speeds) and mechanical/electrical tolerances. Finally, the design approach is validated with the realization of a 3L GaN FCi hardware demonstrator, which achieves the expected efficiency of 99% at nominal load and provides rated overload capacity, i.e., up to three times the nominal current for three seconds.

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