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***Abstract*—DC loads or sources like motor drives, batteries, and strings of PV panels with power levels up to the lower single-digit kilowatt range are typically connected to the single-phase mains using bidirectional ac-dc converters providing power factor correction (PFC) functionality. Often, a dc output voltage range spanning from values lower to values greater than the grid voltage amplitude is required and hence the ac-dc converter must provide buck-boost capability. As an alternative to conventionally used two-stage systems, single-stage converters promise lower realization effort and, in particular, fewer active components like power transistors. This paper therefore analyzes a new bidirectional single-stage single-phase ac-dc buck-boost converter with only three power transistors, whose topology is identified using a systematic approach that is briefly summarized. Advantageously, the new ac-dc converter's negative dc output terminal is connected to the mains neutral, i.e., there is no common-mode voltage at the dc output. The operating principle is explained in detail, and a new advanced modulation method is proposed, which reduces the switching losses by more than 33% and lowers the component stresses. A 3.3 kW proof-of-concept (non-optimized) demonstrator is developed, which connects to the single-phase European ac mains (230 V rms, line-to-neutral) and provides a wide dc output voltage range of 300 V to 450 V. Both, the conventional and the proposed advanced modulation method are experimentally verified, confirming an improvement of the peak efficiency from 95.9% to 96.7% (300 V dc output, 2.5 kW output power) for the advanced modulation method.**

***Index Terms*—AC-DC converter, buck-boost, EV charger, PV inverter, low-switch-count converter topologies, single-phase, topology synthesis, zero common-mode.**

I. Introduction

In accordance with the Paris Agreement [1], a growing number of nations worldwide aspire to attain net-zero greenhouse gas emissions by the middle of the century. To meet this objective, a massive expansion of the electrical infrastructure is expected, facilitating a large-scale deployment of renewable power generation systems. On the load side, Power Factor Correction (PFC) rectifiers, i.e., ac-dc converters with sinusoidal input currents, are key components of this energy transition, as they reduce the amount of reactive power drawn from the grid, leading to increased efficiency and reduced energy consumption and realize compliance with power quality standards and regulations, ensuring the stable and reliable operation of electrical systems. Single-phase ac-dc converters are commonly used in a variety of residential and industrial applications such as manufacturing, electric mobility, telecommunications/datacenters, and, operating as inverters, renewable energy generation.

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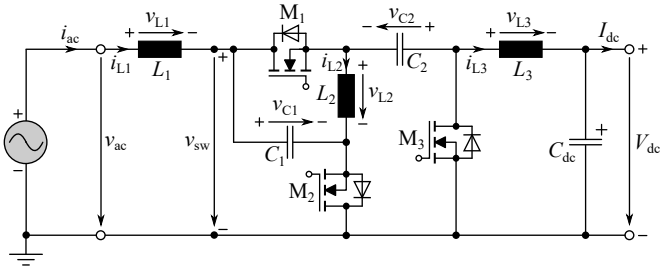

Fig. 1. Main power circuit of the novel bidirectional three-switch single-stage single-phase ac-dc buck-boost converter from [2], providing dc output voltages V_{dc} above and below grid input voltage amplitude $\hat{V}_{ac}$. The considered system specifications are listed in **Tab. I**.

Table I
System Specifications.

Parameter	Variable	Value	Unit
ac voltage	$V_{ac,rms}$	230	V
ac frequency	f_{ac}	50	Hz
dc voltage	V_{dc}	300. . . 450	V
dc output power	P_{dc}	3.3	kW

In many applications, most prominently related to the charging of batteries (e.g., in EV on-board chargers) or also in PV systems (maximum power point tracking), single-phase ac-dc converters must provide a dc output voltage *range* that stretches form values lower to values higher than the grid phase voltage amplitude, i.e., buck-boost functionality is required. Traditionally, for covering this voltage range a standard (boost-type) single-phase ac-dc converter is extended with a (buck-type) dc-dc converter (e.g., [3,4]). This, however, leads to a large number of active components and the energy is processed twice, i.e., by two converter stages, which limits the attainable efficiency. Alternatively, quasi-single-stage ac-dc converters consisting of a passive diode rectifier and a downstream buck-boost dc-dc converter are considered, e.g., [5]–[9]. However, these topologies still suffer from a high component count and only allow unidirectional power transfer due to a input-side diode rectifier. Thus, another option are single-stage ac-dc converters based on a *bridgeless* Single-Ended Primary-Inductor Converter (SEPIC) [11,12] or on a *bridgeless* Ćuk converter [13]–[15]. Furthermore, various al-

Table II
EXAMPLES OF SINGLE-PHASE AC-DC BUCK-BOOST CONVERTERS FROM THE LITERATURE.

Reference	**[4]**	**[8]**	**[10]**	**[16]**	**[17]**	**[18]**	**[19]**	**[20]**	**This P.**
Power Semicond.	**6**	**6**	**8**	**4**	**5**	**4**	**4**	**6**	**3**
Switches	6	1	5	2	4	4	4	6	**3**
Diodes	0	5	3	2	1	0	0	0	**0**
Inductors	2	2	1	1	3	2	2	1	**3**
Capacitors	2	3	2	3	3	4	3	3	**3**
Bidirectional	yes	no	no	no	no	yes	yes	yes	**yes**
Stages	**two**	**quasi-single**	**single**	**single**	**single**	**single**	**single**	**single**	**single**
Common Ground	**no**	**no**	**yes**	**quasi**	**yes**	**no**	**yes**	**quasi**	**yes**
Volt. Stress Switches	$\max(\hat{V}_{ac}, V_{dc})$	$\hat{V}_{ac} + V_{dc}$	$S_{1..4}$: $\frac{\hat{V}_{ac}(1-D)}{D}$ S_5: $\frac{\hat{V}_{ac}}{D}$ [21]	$\hat{V}_{ac} + \frac{V_{dc}}{2}$	$S_{1,4}$: $\hat{V}_{ac}$ $S_{2,3}$: $\hat{V}_{ac} + V_{dc}$	$S_{1,3}$: $\frac{D\hat{V}_{ac}(1-D)}{2D-1}$ $S_{2,4}$: $\hat{V}_{ac}$ [21]	$S_{1,4}$: $\frac{D\hat{V}_{ac}}{2D-1}$ [21] $S_{2,3}$: $\frac{\hat{V}_{ac}(1-D)}{2D-1}$	$S_{1,2}$: V_{dc} $S_{3..6}$: $\hat{V}_{ac} + V_{dc}$	$\hat{V}_{ac} + V_{dc}$
$V_{ac,rms}$ [V]	230	150	230	110	110	110	110	120	**230**
V_{dc} [V]	400	72-240	95	400	80-220	96	60-100	85-200	**300-450**
P_{dc} [kW]	7.7	2	0.7	1	0.5	1	0.3	0.4	**3.3**

Common ground: "quasi" refers to systems where the mains neutral is connected to a capacitive midpoint of the dc output voltage whereas "yes" refers to system where the mains neutral is connected to the negative dc terminal as in **Fig. 1**.

ternative bridgeless single-stage single-phase ac-dc converter topologies with buck-boost functionality have been proposed in the literature [10,11,13,14,16]–[20], however, these require at least four *active* components (power transistors and/or diodes).

In order to reduce the realization effort, topologies minimizing the number of components, and in particular the number of active components, are of high interest. Therefore, some of the authors have proposed a systematic approach for generating such low-switch-count topologies in [2], resulting—amongst others—in a novel bidirectional single-stage single-phase ac-dc buck-boost converter topology with only three power semiconductors. **Fig. 1** shows the converter topology and **Tab. I** lists the key specifications, considering operation in the 230 V (line-to-neutral rms) European mains and an output dc voltage range of 300 V to 450 V, i.e., the dc output voltage can be both, higher or lower than the grid voltage amplitude (i.e., 325 V), allowing for a wide operating range with buck-boost capability. Further, note that the negative dc output terminal is connected to the mains neutral, i.e., advantageously, there are no high-frequency (HF) or low-frequency (LF) common-mode (CM) voltage components at the output terminals. This feature is highly desirable for many applications of ac-dc converters, e.g., transformerless PV (micro-) inverters [22], where this "common-ground" approach effectively mitigates ground leakage currents [23]–[25].

Tab. II compares the three-switch topology investigated in this article (see **Fig. 1**) to selected examples of other buck-boost capable single-phase ac-dc converter topologies discussed above; the examples were chosen with a focus on minimal number of power semiconductors, buck-boost capability and roughly similar specifications to those considered here. Given the vast literature on single-phase ac-dc converters, a detailed comparative evaluation is beyond the scope of this paper; interested readers find further information in, e.g., [21]. A clear advantage of the presented topology is the low number of power semiconductors (three compared to four in case of all—to our best knowledge—other alternatives) and the direct connection of the mains neutral and the negative dc output terminal, which allows a flexible grounding of the dc-side source/load. On the other hand, the voltage stress of the power transistors is comparably high, and three inductors are needed. However, as discussed in [2], all three inductors can be integrated into a single magnetic component which is, however, not further investigated here.

In the following, first **Section II** summarizes the systematic topology derivation process from [2] for the sake of completeness. **Section III** then explains the operating principle of the considered topology from **Fig. 1** in detail and proposes a novel advanced modulation strategy, which results in lower voltage and current stresses of the power components and improved efficiency; further, closed-loop control of the mains current is detailed. To experimentally verify the operating principle and both modulation strategies, a hardware prototype with specifications according to **Tab. I** is built and **Section IV** presents the experimental characterization, including efficiency measurements. Finally, **Section V** concludes the paper.

II. Systematic Topology Derivation

In power electronics, a trade-off exists between different performance metrics such as conversion efficiency, power density, cost, component count, system complexity and more. To overcome the performance limits of existing converter topologies, new converter topologies can be identified based on topology derivation algorithms [2,26]–[28]. The single-phase ac-dc converter topology investigated in this paper (see **Fig. 1**) has been identified with a new topology derivation method proposed in [2], which, for the sake of completeness is briefly summarized here. The interested reader is referred to [2] for further details and further examples of the application of the method.

The systematic method from [2] derives new converter topologies based on a so-called Elementary Converter Cell (ECC) as shown in **Fig. 2a.i**. An ECC comprises an HF port (terminals

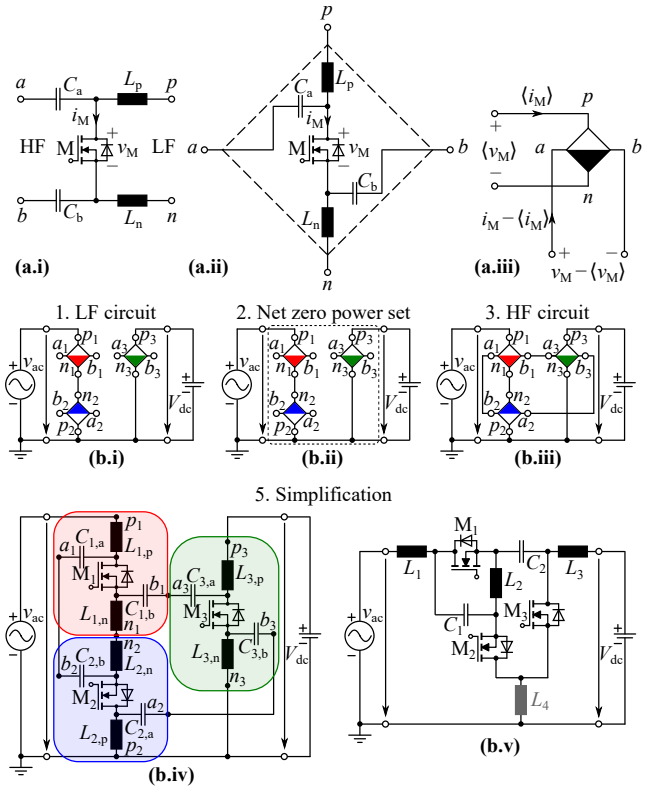

Fig. 2. Steps of the systematic topology derivation method from [2]. **(a.i)** Elementary Converter Cell (ECC) circuit structure with a single switch M, filter elements, HF terminals a and b (the series capacitors block LF currents), and LF terminals p and n (the series inductors block HF currents); **(a.ii)** re-arrangement of the ECC circuit, **(a.iii)** schematic symbol of the ECC with the LF terminals p and n in the vertical direction, and the HF terminals a and b in the horizontal direction. **(b.i-v)** Synthesis of the novel single-stage single-phase ac-dc buck-boost converter topology from **Fig. 1**; the five steps are described in detail in the text. Considering **(b.v)**, out of the three inductors L_1, L_3 and L_4, only two are required; by shorting inductor L_4, the considered topology from **Fig. 1** results.

a, b) and a LF[1] port (terminals p, n), a single power transistor M (e.g., a MOSFET), and two capacitive and two inductive decoupling/filter elements:

- the series capacitors C_a, C_b prevent a LF current flow into the HF port, and
- the series inductors L_p, L_n prevent an HF current flow into the LF port.

Fig. 2a.ii highlights the symmetric ECC structure, which (for identical component values $L_\mathrm{p} = L_\mathrm{n}$ and $C_\mathrm{a} = C_\mathrm{b}$) advantageously results in a CM/DM decoupling of the HF and the LF ports, i.e., a CM voltage applied to the HF terminals does not translate into a CM voltage at the LF terminals and vice-versa. **Fig. 2a.iii** presents the ECC symbol employed in the following derivation steps. $\langle v_\mathrm{M}\rangle$ and $\langle i_\mathrm{M}\rangle$ denote the local (over one switching period) average values of the voltage v_M across and the current i_M through the power transistor M, which thus appear at the LF port. Correspondingly, the HF components $v_\mathrm{M} - \langle v_\mathrm{M}\rangle$ and $i_\mathrm{M} - \langle i_\mathrm{M}\rangle$ appear at the HF port.

Various dc-dc and ac-dc converter topologies can be derived by combining two or more ECCs following a five-step approach detailed in [2]. The five steps are briefly discussed in the following five subsections, aiming at synthesizing a single-stage ac-dc converter topology. Ultimately, this results in the new bidirectional single-stage single-phase ac-dc buck-boost converter from **Fig. 1**.

A. LF Circuit

In a first step, the LF ports p, n of the ECCs are attached to the converter ac input or the dc output as illustrated in **Fig. 2b.i**. As the power transistor M in each ECC shows unipolar voltage blocking capability only (see **Fig. 2a.i**), the first two ECCs (highlighted in red and blue) are connected in an inverse-series configuration to interface the ac input voltage v_ac, which shows both polarities. In contrast, a single ECC (highlighted in green) is sufficient to interface the dc output voltage V_dc and thus, aiming at a low active component count, a minimum number of three ECCs is sufficient for the realization of an ac-dc converter.

B. Net-Zero-Power Sets

Next, each ECC is assigned to a so called "power set". All ECCs within one power set can exchange HF power amongst each others (see next subsection). Therefore, each power set must contain at least two elements [2,26]. As the passive components of the ECCs (capacitors C_a, C_b and inductors L_p, L_n in **Fig. 2a.i**) are designed for HF filtering only, they cannot buffer any LF power (no LF energy storage is possible). Hence, each power set is required to show a net-zero LF input power, i.e., the sum of the LF power flows through the LF port of all ECCs of the power set must be zero.

Here, as indicated in **Fig. 2b.ii**, all ECCs are assigned to the same power set to realize HF power transfer from the ac input to the dc output. Thus, as the power drawn from the single-phase grid shows the characteristic LF pulsation at twice the grid frequency, and as there is no energy storage in the ECCs, also the dc output power fluctuates accordingly. As in any single-phase ac-dc converter, the fluctuation is buffered[2] by a large (electrolytic) output capacitor or an active power pulsation buffer [29], [30].

C. HF Circuit

Next, the HF terminals a, b of all ECCs within the same net-zero-power set are connected; in the most simple case by forming a loop, i.e., by series-connecting all HF ports of the ECCs. It is beneficial to connect the HF terminals (a, b) of the ECCs if their LF ports (p, n) are also connected [2]. Note that the following restrictions apply (see also **Fig. 2a.i**):

- Within an ECC, the terminal a must not be connected to the terminal b as otherwise a potentially destructive shorting of the series capacitors C_a, C_b results when the power transistor M is in the on-state.
- The terminal a of one ECC may not be connected to a terminal a of another ECC as in this case no freewheeling path exists for the series inductors L_p, L_n of both converter

[1]Note that LF refers to slowly changing quantities, i.e., dc or grid-frequency voltages/currents, as opposed to HF, which refers to switching-frequency voltages/currents.

[2]Considering battery charging applications, note that there are also concepts that directly use the pulsating power to charge the battery.

elements in case one of the power transistors M is in the off-state, again with potentially destructive consequences.

Here, the series-connection of the three converter elements as illustrated in **Fig. 2b.ii** is considered, which advantageously enables a further simplification of the power circuit by reducing the number of passive power components in the last derivation step described in **Section II-E** below.

D. Defined Conduction States

In each of the three ECCs, the conduction state of the power transistor M must be strictly defined by the corresponding Pulse-Width Modulation (PWM) switching signal, i.e., no passive rectification via the power transistor body diode (cf. **Fig. 2a.i**) takes place during the off-state. This can be assured if in each power set exactly one power transistor is in the off-state[3] at any given point in time and the remaining power transistors are in the on-state, i.e., for a power set $\mathcal{H}$ comprising k ECCs, the PWM duty cycles $d_\mathrm{j} \in [0, 1]$ (i.e., the relative on-times of the power transistors) are defined such that

$$\sum_{\mathrm{j}\in\mathcal{H}} d_\mathrm{j} = k - 1. \tag{1}$$

Fig. 2b.iv shows the complete power circuit of the derived converter topology and the resulting (allowed) conduction states of the three power transistors $M_{1..3}$ are further detailed in **Section III**.

E. Simplification

After the first four derivation steps, a fully functional converter results as shown in **Fig. 2b.iv**, which, however, may still be further simplified by reducing the number of passive components: Passive series elements (LF-blocking capacitors C_a, C_b and HF blocking inductors L_p, L_n in **Fig. 2a.i**) of two neighbouring ECCs which are connected in series or parallel can be merged into a single component. Further, all LF-blocking capacitors with zero resulting LF voltage during operation may be shorted.

Starting from **Fig. 2b.iv**, thus the inductors $L_{1,\mathrm{n}}$ and $L_{2,\mathrm{n}}$ are combined to inductor L_2 in **Fig. 2b.v**. The same applies to capacitors $C_{1,\mathrm{a}}$ and $C_{2,\mathrm{b}}$, which are combined to C_1 and to $C_{1,\mathrm{b}}$ and $C_{3,\mathrm{a}}$, which result in capacitor C_2. Further, the capacitors $C_{2,\mathrm{a}}$ and $C_{3,\mathrm{b}}$ form a KVL loop with the inductors $L_{2,\mathrm{p}}$ and $L_{3,\mathrm{n}}$ and therefore cannot be subject to any LF offset voltage. Thus, they can be omitted (i.e., replaced with a direct connection). This in turn allows to combine the series-connected inductors $L_{2,\mathrm{p}}$ and $L_{3,\mathrm{n}}$ into a single inductor L_4.

The resulting simplified circuit is depicted in **Fig. 2b.v**, where for any switching state the inductors L_1 and L_3, L_1 and L_4, L_3 and L_4 are connected in series and one of them can thus be omitted. As the inductors L_1 and L_3 are in series to the input and the output terminal, respectively, and thus ensure continuous input and output currents that favourably reduce the Electromagnetic Interference (EMI) filtering effort, L_4 is removed. This, finally, results in the main power circuit of the considered bidirectional single-stage single-phase ac-dc buck-boost converter from **Fig. 1**.

[3]Note that at least one power transistor in each power set / HF loop is required to be in the off-state, as otherwise a potentially fatal short-circuit of the series capacitors occurs in one or several of the ECCs. To assure safe operation, practical realizations require a PWM dead-time, during which two power transistors are in the off-state, resulting in diode conduction during this short time interval.

III. Operating Principle

First, **Section III-A** discusses the operating principle and modulation of the single-stage ac-dc converter depicted in **Fig. 1** based on the conceptual waveforms shown in **Fig. 3**. Further, **Section III-B** presents a new advanced modulation scheme, which leads to a lower number of switching transitions and reduced power transistor voltage and current stresses. This enables an increase in conversion efficiency compared to the standard modulation from [2].

A. Standard Modulation

To achieve PFC operation, the converter must impress a sinusoidal current i_ac in the input inductor i_L1, which is in phase with the grid voltage v_ac (see **Figs. 3a.i,d.i**). Thus, in (quasi)-steady-state operation, the local average value of the ac-side switched voltage v_sw (see **Fig. 1**) is set to $\langle v_\mathrm{sw}(t)\rangle \approx v_\mathrm{ac}(t)$. As discussed in **Section II**, always two out of the three power transistors must be in the on-state. Thus, there are three possible conduction states which are illustrated in **Fig. 4**. The ac-side switched voltage v_sw is defined by the gate signal s_2 of the power transistor M_2 and the capacitor voltages v_C1 and v_C2 as

$$v_\mathrm{sw} = \begin{cases} v_\mathrm{C1}, & s_2 = 1 \\ -v_\mathrm{C2}, & s_2 = 0. \end{cases} \tag{2}$$

The local average value $\langle v_\mathrm{sw}\rangle$ can be defined with the the relative on-time $d_2 \in [0, 1]$ of the power transistor M_2 as

$$\langle v_\mathrm{sw}\rangle = v_\mathrm{C1}\cdot d_2 - v_\mathrm{C2}\cdot(1 - d_2), \tag{3}$$

and for the desired $\langle v_\mathrm{sw}(t)\rangle \approx v_\mathrm{ac}(t)$, the duty cycle d_2 results to

$$d_2 \approx \frac{v_\mathrm{ac} + v_\mathrm{C2}}{v_\mathrm{C1} + v_\mathrm{C2}}, \tag{4}$$

as shown in **Fig. 3b.i**.

For each conduction state (cf. **Fig. 4**), the blocking voltage of the (only) power transistor in the off-state is defined by the sum of the voltages of the two capacitors[4] C_1 and C_2, i.e.,

$$v_\mathrm{M,off} = v_\mathrm{C1} + v_\mathrm{C2}. \tag{5}$$

The voltage across the power transistor M_3 is applied to the positive terminal of the inductor L_3, and in (quasi)-steady-state operation its local average voltage is equal to $\langle v_\mathrm{M3}\rangle \approx V_\mathrm{dc}$ (cf. **Fig. 4**). Thus, the duty cycle d_3 of the power transistor M_3 is set as

$$d_3 \approx 1 - \frac{V_\mathrm{dc}}{v_\mathrm{M,off}}. \tag{6}$$

According to (1), only one power transistor is in off-state for any given point in time, thus the last duty cycle d_1 results to

$$d_1 = 2 - d_3 - d_2. \tag{7}$$

[4]The two capacitors C_1 and C_2 also define the commutation loop of the three power transistors M_1, M_2, and M_3.

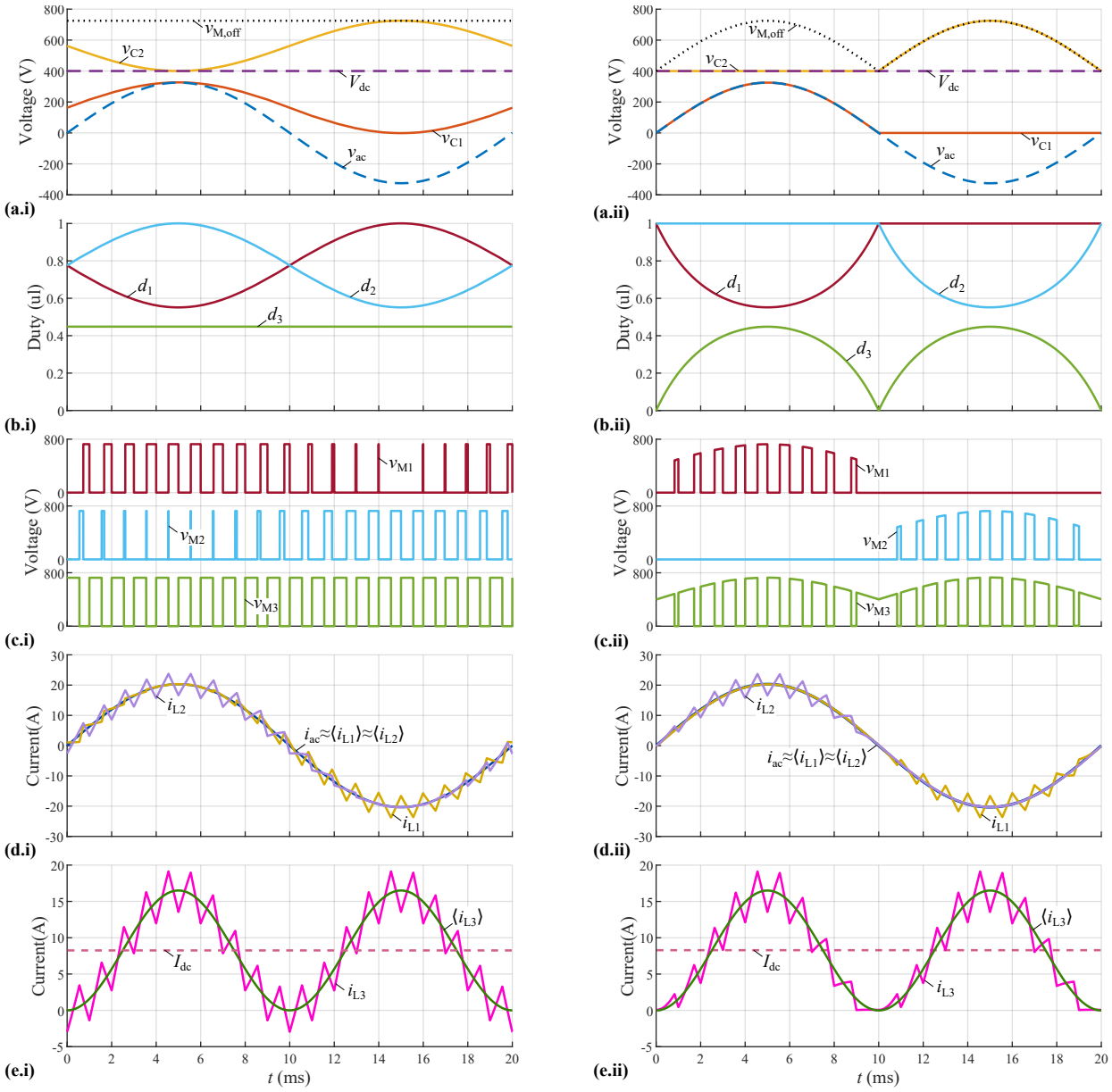

Fig. 3. Conceptual key waveforms of the novel single-stage ac-dc buck-boost converter from **Fig. 1**. **(i)** conventional (see **Section III-A**) and **(ii)** proposed advanced modulation (see **Section III-B**) for a grid period $T_{ac} = 1/f_{ac}$ and considering a low switching frequency $f_{sw} = 20f_{ac}$ for better visibility. **(a)** Input grid voltage v_{ac} and output dc voltage V_{dc}, and capacitor voltages v_{C1} and v_{C2}. Further, the selected constant off-state power transistor blocking voltage $v_{M,off}$ is indicated by a dashed line; **(b)** duty cycles d_1, d_2 and d_3; **(c)** power transistor blocking voltages v_{M1}, v_{M2}, v_{M3}; **(d)** inductor currents i_{L1} and i_{L2} including their respective (switching-frequency) local average values, which are approximately equal to the input grid current i_{ac}; **(e)** inductor current i_{L3} with its local average value and dc output current I_{dc}. The proposed advanced modulation features 33% fewer switching transitions and the minimum possible off-state voltage $v_{M,off}$, which is time-varying.

The resulting duty cycle waveforms d_1, d_2, d_3 are presented in **Fig. 3b.i**. A single sawtooth carrier with two compare levels can be used to generate all three PWM signals $s_{1...3}$. The power transistor blocking voltages v_{M1}, v_{M2}, v_{M3} are shown in **Fig. 3c.i**. With all the duty cycles defined, the capacitor voltages can be derived based on the KVL as

$$v_{C1}(t) = \frac{1}{2}(v_{ac}(t) + v_{M,off} - V_{dc}), \tag{8}$$

$$v_{C2}(t) = \frac{1}{2}(-v_{ac}(t) + v_{M,off} + V_{dc}). \tag{9}$$

Note that the off-state voltage $v_{M,off}$ represents a degree of freedom for the modulation. However, to maintain grid current controllability according to (2), there is a lower bound for both capacitor voltages, i.e., $v_{C1}, v_{C2} > v_{ac}(t)$ (see **Fig. 3a.i**). Thus, when considering a constant off-state voltage $v_{M,off}$, the constraint

$$v_{M,off} \geq \hat{V}_{ac} + V_{dc}, \tag{10}$$

applies, which is similar to an inverting dc-dc buck-boost converter where the power transistors block the sum of the input and the absolute value of the output. Note that this limitation does not constrain the dc output voltage V_{dc} of the ac-dc buck-boost converter, which can be controlled to values both, above

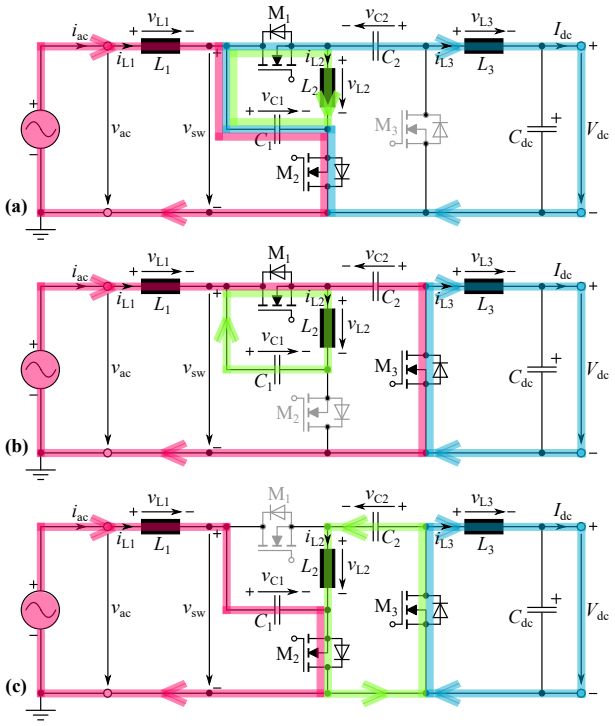

Fig. 4. Conduction states of the ac-dc converter from **Fig. 1**. **(a)** $s_1 = 1$, $s_2 = 1$, **(b)** $s_1 = 1$, $s_3 = 1$, **(c)** $s_2 = 1$, $s_3 = 1$, where $s_{1...3}$ are the gate signals of the corresponding power transistors $M_{1...3}$. The colored current paths are for the positive cycle of the grid voltage v_{ac}.

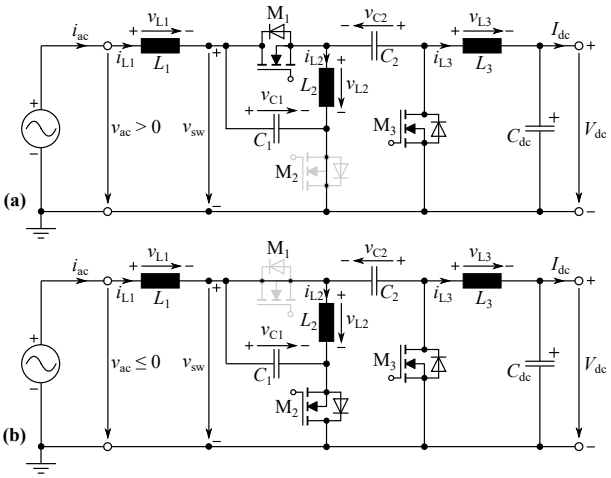

Fig. 5. Explanation of the proposed advanced modulation: the proposed three-switch single-stage ac-dc buck-boost converter from **Fig. 1** can operate in two distinct configurations, i.e., in **(a)** SEPIC mode for $v_{ac} > 0$ V (the switch M_2 is permanently on), and **(b)** Ćuk mode for $v_{ac} \leq 0$ V (the switch M_1 is permanently on). In both cases, only the two respective other transistors are operating with PWM instead of all three transistors as in the conventional modulation.

and below the grid input voltage v_{ac}. In **Fig. 3i**, the minimum constant off-state voltage $v_{M,off} = \hat{V}_{ac} + V_{dc}$ is considered to minimize the power transistor voltage stresses.

Last, **Figs. 3de.i** show the inductor currents i_{L1}, i_{L2}, and i_{L3}. The local average currents $\langle i_{L1} \rangle$, $\langle i_{L2} \rangle$ are identical to the grid ac current i_{ac}, and $\langle i_{L3} \rangle$ reflects the typical twice-grid-frequency power pulsation (which is filtered by a large dc-link capacitor or an active power pulsation buffer) and has a global average (over the grid fundamental period) value equal to the dc output current I_{dc}.

B. Advanced Modulation

For the conventional modulation discussed in **Section III-A**, three switching transitions take place during each switching period. The aim of the proposed advanced modulation is to realize PFC operation with a reduced number of switching transitions and lower power transistor blocking voltage stresses. The corresponding conceptual converter waveforms are presented in **Figs. 3a.ii-e.ii**.

As can be observed from **Fig. 5a**, the considered ac-dc converter is equivalent to a SEPIC buck-boost dc-dc converter [31]–[33] if the power transistor M_2 is replaced with a short and/or is permanently in the on-state while only the power transistors M_1 and M_3 operate with PWM.

Similarly, as shown in **Fig. 5b**, the converter is equivalent to a Ćuk buck-boost dc-dc converter [34,35] if the power transistor M_1 is replaced with a short and/or is permanently in the on-state while only the power transistors M_2 and M_3 operate with PWM.

As the SEPIC is a non-inverting dc-dc converter whereas the Ćuk converter is an inverting dc-dc converter, the two operating modes are accordingly limited to the positive or the negative grid half-period, respectively. The proposed advanced modulation method achieves a reduced number of switching actions by alternating between these two modes during a grid period according to the polarity of the ac input voltage.

Note that the power transistor M_3 is always operated with PWM and its duty cycle is defined for both, SEPIC ($v_{ac}(t) > 0$, duty cycle d_{SEPIC}) and Ćuk ($v_{ac}(t) \leq 0$, duty cycle d_{Cuk}) operation as

$$d_3 = \left\{ \begin{array}{ll} d_{SEPIC}, & v_{ac}(t) > 0 \\ d_{Cuk}, & v_{ac}(t) \leq 0 \end{array} \right\} = \frac{|v_{ac}|}{V_{dc} + |v_{ac}|}. \tag{11}$$

To assure the mutually exclusive PWM operation of the power transistors M_1 and M_2, their duty cycles are set depending on the grid voltage polarity as

$$d_1 = \begin{cases} 1 - d_3, & v_{ac}(t) > 0 \\ 1, & v_{ac}(t) \leq 0, \end{cases} \tag{12}$$

$$d_2 = \begin{cases} 1, & v_{ac}(t) > 0 \\ 1 - d_3, & v_{ac}(t) \leq 0. \end{cases} \tag{13}$$

Fig. 3b.ii shows the corresponding duty cycle waveforms, where a duty cycle equal to one corresponds to a permanent on-state during the entire switching period without any switching transitions and associated switching losses.

As can be observed in **Fig. 3a.ii**, the advanced SEPIC / Ćuk modulation also impacts the capacitor voltages as

$$v_{C1}(t) = \begin{cases} v_{ac}(t), & v_{ac}(t) > 0 \\ 0, & v_{ac}(t) \leq 0, \end{cases} \tag{14}$$

$$v_{C2}(t) = \begin{cases} V_{dc}, & v_{ac}(t) > 0 \\ V_{dc} - v_{ac}(t), & v_{ac}(t) \leq 0, \end{cases} \tag{15}$$

Table III
DETAILS ON THE HARDWARE PROTOTYPE COMPONENTS.

Component	Variable	Value	Unit	Details	Manufacturer
DSP controller	-	150	MHz	TMS320F28335	Texas Instruments
Inductors	L_1, L_2, L_3	600	µH	HEQ 3626A High Flux ($\mu_r = 60$) 60 turns of 0.3 mm flat wire	Chang Sung Corporation
Series capacitor	C_1	4.7	µF	R75PW44704030J	Kemet
	C_2	2.2	µF	R60QW42205030K	Kemet
Output / dc capacitor	C_{dc}	1	µF	R76QW410050H3J	Kemet
Input / ac capacitor	C_{ac}	$4 \cdot 0.1$	µF	890334023023CS	Würth Elektronik
Power transistors	M_1, M_2, M_3	1200	V	C3M0032120K	Wolfspeed
Heatsink & Fan	-	0.75	K/W	LAM 4 100 12	Fischer Elektronik

which results in a time-varying power transistor blocking voltage

$$v_{M,off}(t) = |v_{ac}(t)| + V_{dc} \leq \hat{V}_{ac} + V_{dc}. \tag{16}$$

Thus, as can be observed from **Fig. 3c.ii** (advanced modulation) versus **Fig. 3c.i** (conventional modulation), the advanced modulation features 33% fewer switching transitions, as well as as the minimum possible transistor blocking voltage. It is worth highlighting that the SEPIC / Ćuk modulation results in a different shape of the HF current ripple of the three inductors $L_{1...3}$, whereas the switching-frequency local average currents are identical to those of the conventional modulation (see **Figs. 3e.i/ii**).

C. Closed-Loop Control

In typical applications, the mains current reference i^*_{ac} is generated by an outer control loop, e.g., of the dc output voltage in case of a rectifier or of the power flow in case of a PV inverter. In both cases, closed-loop control of the mains current $i_{ac} = \langle i_{L1} \rangle$ is achieved in a straightforward manner with a proportional (P) or proportional-integral (PI) regulator that calculates the required inductor voltage $\langle v_{L1} \rangle$ as

$$\langle v_{L1} \rangle = k_P \cdot \left(i^*_{ac} - \langle i_{L1} \rangle \right), \tag{17}$$

where k_P is the controller gain. As shown in **Fig. 6**, subtracting $\langle v_{L1} \rangle$ from the measured mains voltage v_{ac} yields the required local average voltage $\langle v_{sw} \rangle$, which can be adjusted via the duty cycle d_2 according to (4) for the standard modulation (see **Fig. 6a**) or via the duty cycle d_3 according to (11) for the proposed advanced modulation (see **Fig. 6b**). As the plant is an inductor only, i.e., L_1, the controller design is straightforward and follows standard methods and/or software tools can be employed. Here, $k_p = 10$ is selected, which results in a cutoff frequency of about 2.5 kHz and a phase margin of about 70°. The same control parameter can be used for both, standard and advanced modulation.

To verify the closed-loop operation of the system, detailed circuit simulations (PLECS) have been carried out, whereby the converter operates between an ac voltage source (representing the mains) and a dc voltage source (e.g., representing a battery). The grid current reference is obtained as $i^*_{ac} = G^* \cdot v_{ac}$, whereby G^* can be positive (rectifier) or negative (inverter) and thus directly defines the power flow level and direction. Further, passive parallel R_dC_d damping of the capacitors C_1 and C_2 is implemented ($C_{1d} = 2C_1$, $C_{2d} = 2C_2$, and $R_{1d} = R_{2d} = 30\,\Omega$) in the simulation model.[5] Alternatively, active damping schemes and/or advanced control methods could be investigated, but likely additional voltage and/or current sensors would be required.

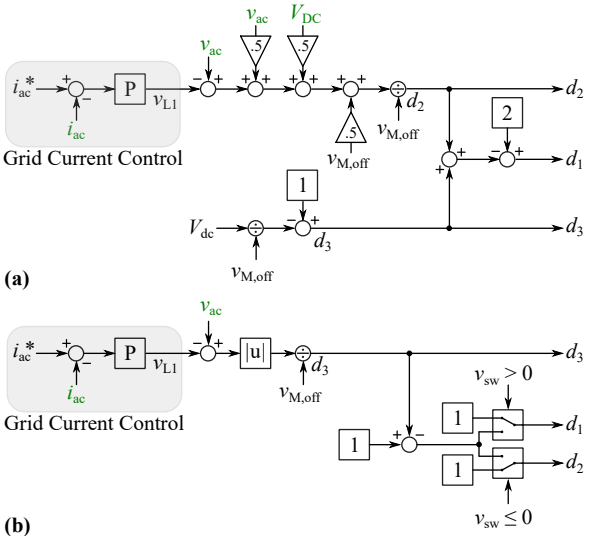

Fig. 6. Control diagram for controlling the grid current i_{ac} for **(a)** the standard modulation and **(b)** the advanced modulation. Note that all variables refer to local average values; the $\langle\rangle$ symbols have been omitted for better visibility.

Fig. 7 shows the thus simulated key waveforms for closed-loop control using the standard modulation and the advanced modulation, respectively. At time $t = 25$ ms, a step change (with a rise time 2 ms) in G^* from the value corresponding to nominal power in rectifier mode to the value corresponding to nominal power flow in inverter mode, is applied. The simulation results clearly confirm adequate tracking of the mains current reference and stable operation of the system even under a rather extreme change of operating points.

IV. Experimental Verification

As [2] has verified the feasibility of the considered converter topology in **Fig. 1** by means of circuit simulations and considering the conventional modulation only, the aim of this section is twofold: First, the basic operating principle verified

[5]Note that in a hardware realization, frequency-dependent ac resistances of coils, PCB traces, etc. provide some damping especially at higher frequencies, which, however cannot be modeled in the simulation.

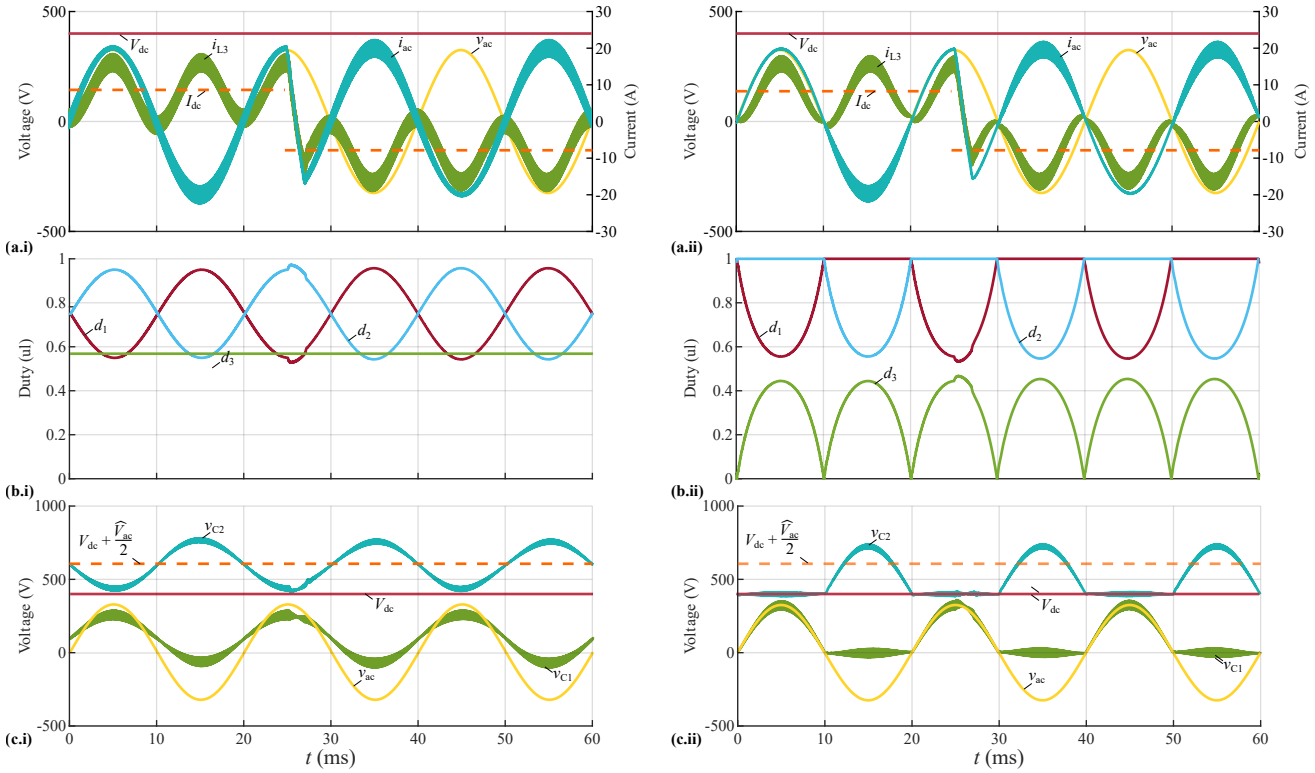

Fig. 7. Simulated key waveforms of the novel single-stage ac-dc buck-boost converter for three grid periods $T_{ac} = 1/f_{ac}$ using closed-loop control of the mains current according to **Fig. 6**, considering a dc voltage of 400 V and **(i)** standard and **(ii)** advanced modulation. At time $t = 25$ ms, the set point is changed from nominal power in rectifier mode (power flow from the ac to the dc side) to nominal power in inverter mode (power flow from the dc to the ac side) within 2 ms. **(a)** Terminal voltages v_{ac}, V_{dc} and currents i_{ac}, i_{L3} (the dc current I_{dc} is equal to the global average value of i_{L3} and indicated with a dashed line); **(b)** duty cycles d_1, d_2 and d_3; **(c)** terminal voltages v_{ac}, V_{dc}, and capacitor voltages v_{C1} and v_{C2}. Component values are as in **Tab. III**.

experimentally, and, second, the efficiency gains of the proposed advanced modulation strategy are assessed.

To do so, a 3.3 kW hardware demonstrator system shown in **Fig. 8a** with specifications according to **Tab. I** and using a switching frequency of $f_{sw} = 72$ kHz (cf. **Fig. 8a**) was developed. With the considered dc output voltage range, the maximum power transistor blocking voltage according to (5) results to 775 V and therefore 1.2 kV SiC Power MOSFETs are employed. The main electrical parameters and details on the power component realizations are listed in **Tab. III**. The detailed converter volume breakdown is provided in **Fig. 8b**. The overall power density is 4.9 kW/dm^3. Note that the demonstrator system does not include an EMI filter and is neither optimized for size or efficiency. The converter was extensively tested in inverter operation (i.e., the dc terminal is connected to a dc voltage source and the ac terminal is connected to a load resistor), as this allows testing in open-loop configuration, which is sufficient for the intended verification of the operating principle as well as for assessing the loss reduction achieved with the proposed advanced modulation method.

A. Steady-State Nominal Power Operation

Figs. 9ab show the measured key waveforms for nominal power operation with the maximum dc output voltage of $V_{dc} = 450$ V for both, the conventional (**Figs. 9ab.i**) and the proposed advanced modulation (**Figs. 9ab.ii**). As can be observed in **Fig. 9a**, the grid current i_{ac} is nicely sinusoidal and in phase with the voltage v_{ac} for both modulation strategies. The only observable difference between the two modulation schemes in **Fig. 9a** is the different envelope of the HF inductor current ripple of i_{L3}. In contrast, the capacitor voltage waveforms in **Fig. 9b** differ substantially for the two modulation strategies and closely match the predicted waveforms from **Fig. 3a**.Note further that no passive $C_d R_d$ damping of C_1 and C_2 has been used for the experiments (in contrast to the closed-loop simulations discussed in **Section III**).

Table IV
MEASURED TOTAL LOSSES AND EFFICIENCIES FOR NOMINAL POWER OPERATION WITH $P_{out} = 3.3$ kW.

	Reg. Modulation		Adv. Modulation	
V_{dc}	Tot. Loss	Eff.	Tot. Loss	Eff.
300 V	155.7 W	95.3%	135.6 W (-12.9%)	95.9%
350 V	151.7 W	95.4%	130.6 W (-13.9%)	96.0%
400 V	156.0 W	95.3%	124.7 W (-20.1%)	96.2%
450 V	155.8 W	95.3%	126.2 W (-19.0%)	96.2%

B. Transient Buck-Boost Operation

After verifying the steady-state operation of the converter, a dc voltage ramp from 200 V to 450 V during 400 ms is applied (remember that the testing is done in inverter mode, and hence the dc source can be ramped accordingly) and the results are presented in **Fig. 9c**. Note that this ramp includes a transition from buck ($V_{dc} < \hat{v}_{ac}$) to boost ($V_{dc} > \hat{v}_{ac}$) operation at $t = 185$ ms, where no transient oscillations are notable. Thus, the experimental results verify the full functionality of the proposed

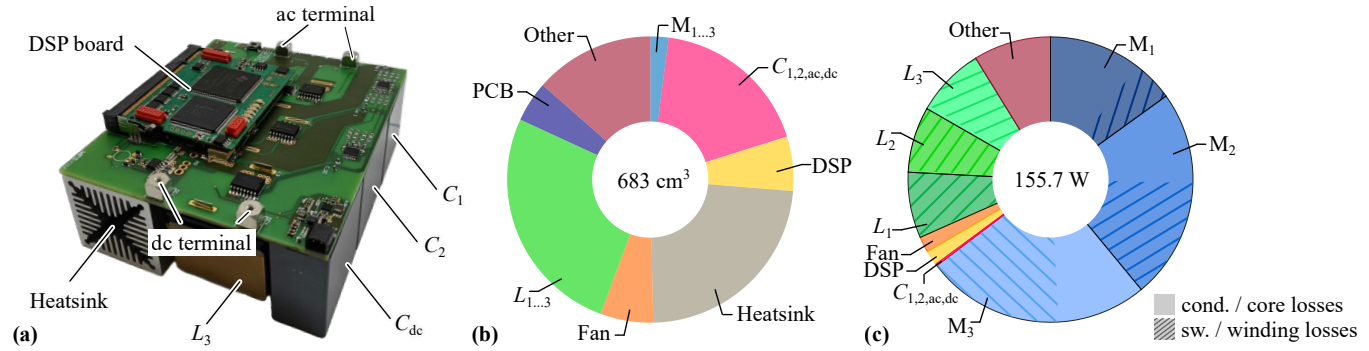

Fig. 8. **(a)** Realized 3.3 kW hardware demonstrator of the novel single-stage single-phase ac-dc buck-boost converter topology with specifications from **Tab. I** and dimensions 125.5 mm × 104 mm × 52.4 mm, which corresponds to a power density of 4.9 kW/dm^3 (79.6 W/in^3). The main electrical parameters and details of the power component realizations are listed in **Tab. III**. **(b)** Converter volume breakdown. **(c)** Calculated loss breakdown for conventional operation with V_{dc} = 300 V and P_{dc} = 3.3 kW. For the power transistor losses, the hatched area represents the switching losses and the rest of the losses are conduction losses. Similarly, for the inductor losses, the hatched area represents the winding losses and the rest of the losses are the core losses, which are negligible. The discrepancy between the calculated (142.0 W) and the measured losses (155.7 W) corresponds to a model error of less than 10% and is labeled as "other".

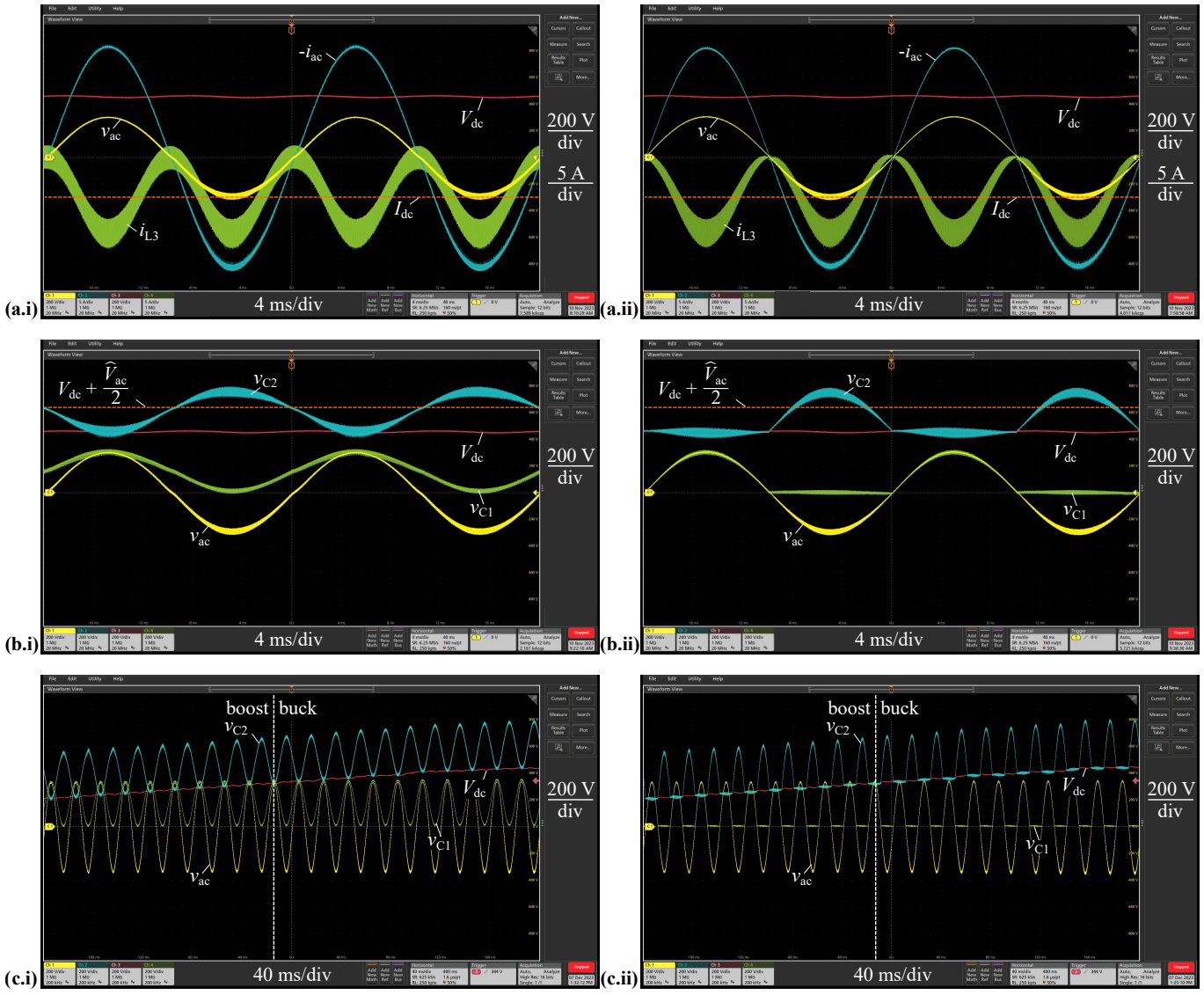

Fig. 9. Measured key converter waveforms of the demonstrator from Fig. 8 operating in inverter mode (supplied by a dc power supply, resistive load on the ac side). **(a), (b)** Steady-state operation with nominal power and a dc voltage of 450 V for **(i)** regular and **(ii)** advanced modulation, specifically: **(a)** terminal voltages v_{ac}, V_{dc} and currents i_{ac}, i_{L3} (the dc current I_{dc} is equal to the global average value of i_{L3} and indicated with a dashed line), and **(b)** terminal voltages v_{ac}, V_{dc}, and capacitor voltages v_{C1} and v_{C2}. **(c)** Transient behavior with an applied dc voltage ramp from V_{dc} = 200 V to V_{dc} = 450 V while maintaining a constant ac mains voltage amplitude $\hat{v}_{ac}$ (by adjusting the modulation parameters accordingly) and thus constant average power P_{dc} = 1 kW; note the smooth transition from buck to boost mode at t = 185 ms.

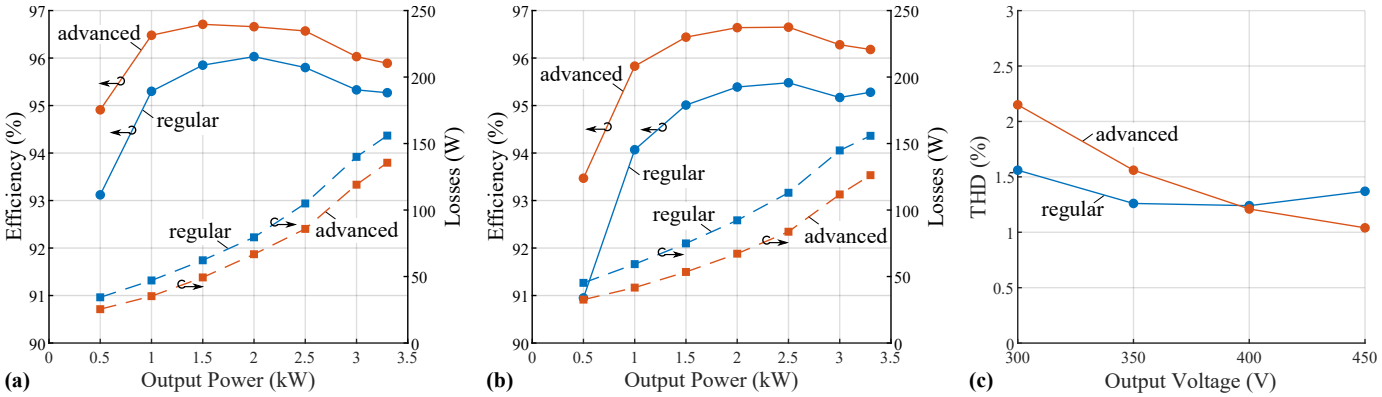

Fig. 10. Measured converter efficiencies (round scatter symbols) and power losses (square scatter symbols) over the output power for **(a)** V_{dc} = 300 V and **(b)** V_{dc} = 450 V, considering the conventional and the proposed advanced modulation techniques. **(c)** Total Harmonic Distortion (THD_{40}) for different output voltage levels and nominal power (P_{out} = 3.3 kW).

converter with both, the standard and the advanced modulation strategy. Note that the lowest output voltage considered in this measurement is V_{dc} = 200 V, i.e., less than the 300 V specified in **Tab. I**.[6] This highlights that there is no hard limit for the minimum output voltage. However, with lower output voltage, the output current increases for a given output power, and hence a power derating for lower output voltages would be needed, i.e., if a lower output voltage is desired, the output power could be reduced (by fixing the maximum output current). Similar considerations apply to use cases where a second, lower grid voltage should be supported (e.g., 120 V or 100 V line-to-neutral rms as available in North America or in Japan, respectively).

C. Efficiency Measurements

A comprehensive loss characterization across the output power and dc output voltage is conducted and the conversion losses and the efficiency are measured with a Norma D 6100 power analyzer (the auxiliary circuitry was powered externally and the associated power consumption was added in post-processing). **Figs. 10ab** show the measured efficiencies for two dc output voltages of V_{dc} = 300 V and V_{dc} = 450 V, respectively, and **Tab. IV** further summarizes the measured power losses and efficiencies at nominal power for several dc output voltage levels. At nominal power, the efficiency for the regular modulation is nearly independent of the dc voltage V_{dc}, which can be attributed to the fact that the power transistor blocking voltage $v_{m,off}$ increases while the conduction losses ($\propto I_{dc}^2$) decrease with increasing V_{dc}. Further, note that the calculated loss breakdown[7] for conventional operation with V_{dc} = 300 V and P_{dc} = 3.3 kW shown in **Fig. 8c** yields a total of 142.0 W, i.e., underestimating the measured loss of 155.7 W by less than 10%, confirming a good modeling accuracy. As can be observed from the loss breakdown, the power transistor conduction and switching losses dominate the total converter losses (≈ 60% of the total losses).

As can be observed in **Figs. 10ab** and from **Tab. IV**, the proposed advanced modulation strategy enables substantial efficiency gains. This is mainly due to (1) the reduced power transistor blocking voltage $v_{M,off}$ (see **Fig. 3c**), and (2) the reduced number of switching actions in each switching period (two instead of three) compared to the conventional modulation, both contributing to a reduction in switching losses. Accordingly, the ratio between switching losses and conduction losses ($\propto I_{dc}^2$) changes and the nominal power efficiency in **Tab. IV** increases with increasing dc output voltage V_{dc}. The proposed advanced modulation achieves a maximum loss reduction of 20% for operation with V_{dc} = 400 V. In summary, the maximum efficiency for nominal power operation can be increased from 95.4% with the standard modulation to 96.2% with the advanced SEPIC/Ćuk modulation. Further, the peak efficiency for P_{out} = 2.5 kW and V_{dc} = 300 V (see **Fig. 10a**) can even be increased from 95.9% to 96.7% with the advanced modulation. Compared with bridgeless SEPIC or Ćuk converter

[6] In the considered design example, the output voltage range (300 V. . . 450 V) was chosen such that an EV battery pack with a typical nominal voltage of 400 V can be completely charged and/or discharged, given the state-of-charge curves for typical lithium-ion batteries.

[7] The power transistor losses are obtained from circuit simulations using PLECS and the device loss/thermal models provided by the manufacturer, assuming a gate resistor of R_{gate} = 10 Ω, a thermal interface material thermal resistance of 0.2 K/W, a heatsink thermal resistance and capacitance of 0.75 K/W and 200 J/K, respectively, as well as an ambient temperature of 25 °C (corresponding to expected operating conditions in a laboratory setting). The inductor winding losses are calculated as $P_w = R_{LF} I_{LF}^2 + R_{fsw} I_{HF}^2$, with R_{LF} = 40 mΩ as the LF and R_{fsw} = 1.4 Ω as the HF winding resistance at 72 kHz measured with an impedance analyzer on a prototype inductor. N = 60 turns of a solid rectangular helical winding are wound around the core, which has a cross section area of A_c = 181 mm² and a volume V_c = 17 cm³. The magnetic core HF loss density ρ_c of the inductors within a switching period $T_{sw} = 1/f_{sw}$ is assessed according to the standard Steinmetz loss model $\rho_c = V_{core} k f^{\alpha} \Delta B_{pk}^{\beta}$ (and then averaged during one grid period) with the single-ended HF peak core flux density ΔB_{pk}, and the frequency $f = f_{sw}$. The Steinmetz parameters of the considered High Flux powder core are k = 1.46, α = 1.32, β = 2.27 [36]. The capacitor losses are calculated assuming that the entire HF rms current occurs at the switching frequency and by using the equivalent series resistance values from the datasheets.

PFC rectifiers [11,12,14,15] which achieve efficiencies between 94% and 97%, a similar efficiency can be achieved.

However, even though the demonstrator has not been optimized, the measured efficiency values are relatively low compared to, e.g., standard boost-type single-phase totem-pole PFC rectifiers employing 650 V GaN or SiC power transistors and reach efficiencies of up to around 99% [37]–[40]. But such systems cannot cover the required buck-boost capability. Further, the dc output terminals of standard systems are subject to HF and LF CM voltage excitations with respect to ground, unlike the dc output terminals of the new single-stage ac-dc converter discussed in this paper. Reducing the number of converter stages and components generally leads to higher component stresses (e.g., the new ac-dc buck-boost converter requires 1200 V power transistors even though the input and the output voltage levels indicate that 650 V devices should suffice). These higher stresses ultimately result in a lower efficiency, which can be seen as the price for a higher converter-level functionality realized per component used.

D. Grid Current Quality

To assess the grid current quality, the measured ac currents i_{ac} (e.g., **Fig. 9a**) were exported, and the grid current total harmonic distortion THD_{40} values according to EN 61000-3-2 were calculated in MATLAB. **Figs. 10c** compares the grid current Total Harmonic Distortion (THD) at nominal power for both, the standard modulation and the advanced SEPIC/Ćuk modulation across the entire dc output voltage range. The worst-case THD_{40} values are low, i.e., 1.6% and 2.2%, respectively. As visible in **Fig. 10c**, the nominal power THD_{40} is lower for the standard modulation for voltages below 400 V, whereas for higher dc voltages the advanced modulation shows slightly lower THD_{40}.

V. Conclusion

Single-phase ac-dc converters play a crucial role in various applications, such as industry automation, renewable energy or electric mobility. In many applications, a wide dc output voltage range is required, i.e., dc output voltages that are lower and higher than the grid input voltage amplitude. Hence, buck-boost capability of the ac-dc converter is essential. Typically, ac-dc converters with buck-boost capability are realized as two-stage systems, which implies a high number of (active) components and a limitation of the efficiency because the power is converted twice. Based on a new systematic approach for synthesizing converter topologies with a minimum number of active components, [2] recently has proposed a new bidirectional single-stage single-phase ac-dc buck-boost converter with only three power transistors. Advantageously, the negative dc output terminal of this converter is connected to the mains neutral and hence zero CM voltage appears at the dc output.

This paper briefly recapitulates the derivation of the converter topology and then explains the operating principle in detail. Further, a new advanced modulation strategy is introduced, which lowers the component stresses and improves the efficiency compared to the standard modulation, and a straightforward closed-loop control method for the mains current is briefly discussed. To verify the theoretical considerations, a 3.3 kW hardware demonstrator interfacing the single-phase European ac mains (230 V rms line-to-neutral) is designed and realized, providing a wide dc output voltage range from 300 V to 450 V. The converter is extensively tested in open-loop inverter configuration. Detailed efficiency measurements show that by applying the proposed advanced modulation, the peak efficiency can be increased from 95.9% to 96.7% (for 300 V dc output voltage and 2.5 kW). These values indicate the trade-off between high functionality per component and high component stresses (e.g., the need for 1200 V power transistors). On the other hand, note that the prototype was designed as a proof-of-concept and has not been optimized regarding size nor efficiency. Possibilities to increase the efficiency include parallel or series interleaving of several building blocks using the new topology. Further, the three inductors can be combined on a common E-core to reduce size and losses, as the inductors of the realized demonstrator account for 26% of the volume and almost 30% of the total losses. Finally, to reduce hard-switching losses, the inductance values can be decreased to achieve TCM operation. This, however, leads to higher rms currents and the need for modulating the switching frequency over the mains period. All in all, the new single-stage single-phase ac-dc buck-boost converter topology shows a very interesting combination of low complexity, realization effort, high functionality, and zero CM voltage at the dc output terminals. Finally, further research should address a comprehensive and fair comparative evaluation against alternative topologies providing these favorable set of features, using a multi-objective optimization routine.

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