Detailed Modeling and In-Situ Calorimetric Verification of Three-Phase Sparse NPC Converter Power Semiconductor Losses

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***Abstract*— The three-phase (3-Φ) three-level (3-L) sparse neutral point clamped converter (SNPCC) combines a 3-L matrix stage and a 3-Φ two-level (2-L) inverter stage to generate 3-L switched output voltages with a reduced transistor count (10 instead of 12 or 18) compared with the classical 3-L NPCC or 3-L active NPCC structure, targeting variable-speed drive (VSD) systems with low ripple of the motor phase currents or bidirectional 3-Φ power factor correcting (PFC) rectifier systems with reduced boost inductor volume. This article analyzes and experimentally characterizes the performance of an IGBT-based 3-Φ 3-L SNPCC and describes, for the first time, a hybrid current commutation effect between inverter-stage diodes and matrix-stage IGBTs that occurs when operating with lower modulation indices and leads to increased switching losses (up to 20%). The proposed new semiconductor loss modeling approach accounts for this effect successfully, which is verified (<10% error) on an 800-V_{dc}, 7.5-kW SNPCC hardware demonstrator using a new in-situ calorimetric method that facilitates accurate stage-level semiconductor loss measurements. Heat spreading effects caused by the asymmetrical losses injection and thermal decoupling between two in-situ loss measurement blocks are carefully checked with finite-element method (FEM) simulations. Furthermore, an experimental evaluation of common-mode (CM) and differential-mode (DM) high-frequency (HF) voltage-time area ripples (as a generic measure for the required filtering effort) for three typical symmetrical and asymmetrical modulation switching state sequences is provided together with the semiconductor loss characterization. Utilizing a low-switching-loss asymmetric modulation scheme that operates the 3-L matrix stage and the 2-L inverter stage with the effective switching frequencies of 16 kHz and 5.3 kHz, respectively, the 3-L SNPCC demonstrator finally achieves a high rated power (7.5 kW, load current phase shift $\phi = 0$) semiconductor efficiency of 98.8%.**

***Index Terms*— Comprehensive semiconductor loss modeling, electric traction inverters, in-situ calorimetric semiconductor loss measurement, three-phase (3-Φ) three-level (3-L) sparse neutral point clamped converter (SNPCC), variable-speed drives (VSDs).**

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I. Introduction

VARIABLE-SPEED drives (VSDs) enable significant system-level electricity saving, e.g., in industrial applications of electric motors (70% of the electricity consumed by industry is used in electric motor systems [1]) and, thus, offer clear economical and ecological advantages [2]. The conventional three-phase (3-Φ) two-level (2-L) inverter topology based on silicon IGBTs is the prevalent solution used in industrial drive systems due to its low cost, high reliability, and low complexity [3]. However, due to the limited number of available voltage space vectors, 3-Φ 2-L converter drives suffer from large high-frequency (HF) differential-mode (DM) and common-mode (CM) voltage-time area ripples of the generated switched output voltages, which ultimately translate into correspondingly large motor torque ripple and CM-related issues, such as motor bearing currents. These are exacerbated by the relatively low switching frequencies of realizations typically based on 1200-V IGBTs (required for dc-link voltages of 720, . . . , 800 V) [4].

Multilevel inverters are an alternative solution with clear advantages, e.g., a higher effective switching frequency and, hence, lower motor current and torque harmonics, and higher allowed dc-link voltage for a given semiconductor voltage rating [5], [6], [7], [8], [9], [10]. The state-of-the-art multilevel converters are commonly synthesized from multilevel bridge legs; i.e., the output of each bridge leg features a multilevel switched phase voltage waveform [11]. Such multilevel bridge legs can be realized with different topologies [5]: diode clamped [12], [13], capacitor clamped [6], [14], and cascaded multicell [15].

In particular, as proposed in 1981 [12], [13], three-level (3-L) neutral point clamped (NPC) inverters, where clamping diodes allow to establish a connection between the dc-link midpoint (neutral point) and a bridge-leg output, are attractive, since multilevel phase voltages with reduced switching frequency harmonics amplitudes are generated, and all power semiconductors still only need to block half the total dc-link voltage. However, a main disadvantage of the NPC is that, due to the unequal loss distribution, the most stressed transistor sets the upper limit of the switching frequency and the allowed phase current [16]. Furthermore, for an increased number of voltage levels, a large number of clamping diodes

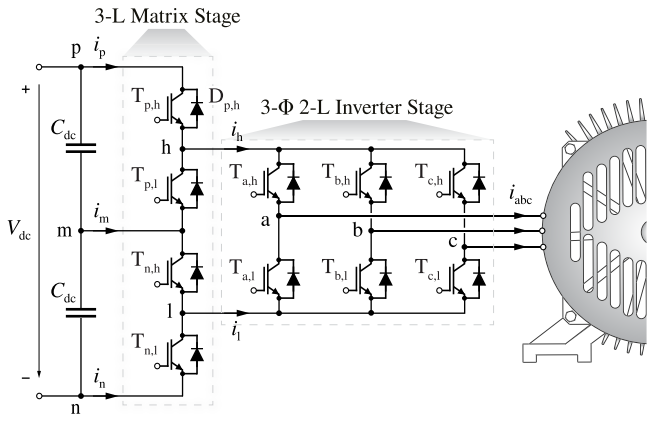

Fig. 1. Schematic of the power circuit of the three-level (3-L) sparse neutral point clamped converter (SNPCC), which is composed of a three-level 3-L matrix stage connected to a three-phase (3-Φ) two-level (2-L) inverter stage.

is required (increased complexity), and capacitor balancing becomes problematic [17]. Therefore, active NPC (ANPC) inverters extend the NPC diode clamping branches with antiparallel transistors, such that a scheme for loss balancing among the semiconductors can be introduced [16], [18].

Nevertheless, a total of 18 transistors are employed in the ANPC converter because of the phase modularity, leading to high costs, significant implementation complexity, and reduced reliability. Thus, extensive research has been conducted on multilevel converters with reduced switch count [19], [20] featuring lower cost and enhanced reliability. In particular, converter-level multistage structures, or so-called multiplexed topologies, are promising multilevel converter candidates, since often cost can be further reduced by, e.g., selecting a lower cost semiconductor technology for a converter stage that operates with a lower switching frequency [21], [22], or because of minimized energy storage that also results in smaller volume and lower weight [23].

Among multiplexed topologies, the sparse NPC converter (SNPCC) [24], [25] is a particularly interesting option, as it can be seen as an ANPC inverter where the dc-link connected parts of the 3-L bridge legs of the phases of a conventional 3-L ANPC are joined into a single 3-L voltage selector (or matrix stage) employing ANPC transistors common for all three phases. The reduced complexity of the resulting system is indicated with the denomination SNPCC. Alternatively, the SNPCC could be considered as a combination of a 2-L inverter with a 3-L dc-link voltage source, where a voltage selector switching stage (or multiplexer) is employed to define the inverter stage dc-link operating voltage level (V_{dc}, $V_{dc}/2$, and 0); i.e., the voltage selector switching stage multiplexes between the three available dc-link voltage levels, considering also the capacitive midpoint/neutral point balancing.

Thus, the SNPCC, illustrated in Fig. 1, is selected and analyzed in this article. The SNPCC was introduced to simplify the 3-L NPC inverter without sacrificing its main advantages. The SNPCC requires only 10 (instead of 12) power transistors and features a cascaded circuit structure, i.e., a 3-L matrix stage (whose switches operate at half the dc voltage) followed by a 3-Φ 2-L inverter stage (whose switches must be rated for the full dc voltage). The matrix stage can regulate the voltage v_{hl} at the input of the inverter stage into a six-pulse shape, such that two inverter phases can be clamped at any given time [so-called 1/3-pulse width modulation (PWM)], resulting in significantly reduced inverter-stage switching losses [26]. Hybrid implementations, i.e., adopting different semiconductor technologies in the matrix and inverter stages, can achieve a further reduction of semiconductor losses [27]. However, in contrast to the conventional 3-L topologies, e.g., the 3-L NPCC, fewer output voltage space vectors are available (in particular, medium-length vectors with an amplitude of $\sqrt{3}V_{dc}/3$ cannot be generated, see below), which results in slightly increased CM/DM filtering effort [25], [26]. Moreover, the semiconductors of the inverter stage need to block and switch the full dc voltage. This is in contrast to the conventional phase-modular 3-L topologies, where all semiconductors are only rated for half of the total dc voltage.

The 3-L SNPCC, or recently also called "coupled ten-switch 3-Φ 3-L inverter" in [28] and [29], has been analyzed with respect to its operating principle and space vector PWM (SVPWM) in [25] and [26]. Various advanced control strategies have been successfully implemented in 3-L SNPCC-based inverter systems, e.g., direct torque control [30] or model predictive control [31]. A topology structure extension, i.e., parallel operation of 3-Φ 3-L SNPCCs is explored in [32], and [22] extends the concept to higher level counts, targeting medium-voltage drive applications. However, the aforementioned analyses mainly focus on the operation with high modulation indices, i.e., with output voltage space vectors in area Ⅱ of the space vector diagram shown in Fig. 2(a). Furthermore, the 3-L SNPCC is simplified from the 3-L ANPCC where fairly complex current commutation strategies exist and could lead to switching overvoltages because of, e.g., the non-active (off-state) switches [33] and additional switching losses [9], [34], [35]. For instance, [34] compares the different switching losses when long or short commutation loops are involved in the current commutation and proposes a new modulation scheme to achieve a better switching performance, and [35] also proposes a novel modulation scheme, which allows assigning to each device either a current conduction or switching function and/or conduction or switching losses. However, such elaborate analyses of the current commutation and its related switching losses for the SNPCC, especially in operating area Ⅰ, are still missing. Moreover, no detailed and experimentally verified model for the SNPCC semiconductor losses over a wide operating range of modulation index, load power factor, and various symmetric/asymmetric modulation sequences is available in the literature.

Accordingly, this work first addresses parasitic current sharing effects and resulting nonstandard commutations that appear when the 3-L SNPCC operates in area Ⅰ, i.e., with low modulation indices. These effects lead to extra switching losses (up to 20%) that are included in a comprehensive semiconductor loss model for the 3-Φ 3-L SNPCC. Second, the loss model is verified with an IGBT-based 800-V_{dc}, 7.5-kW 3-Φ 3-L SNPCC demonstrator and a new in-situ calorimetric semiconductor loss measurement method, which enables individual loss measurements for the 3-L matrix and the 2-L inverter stage. Heat spreading effects caused by the asymmetrical loss

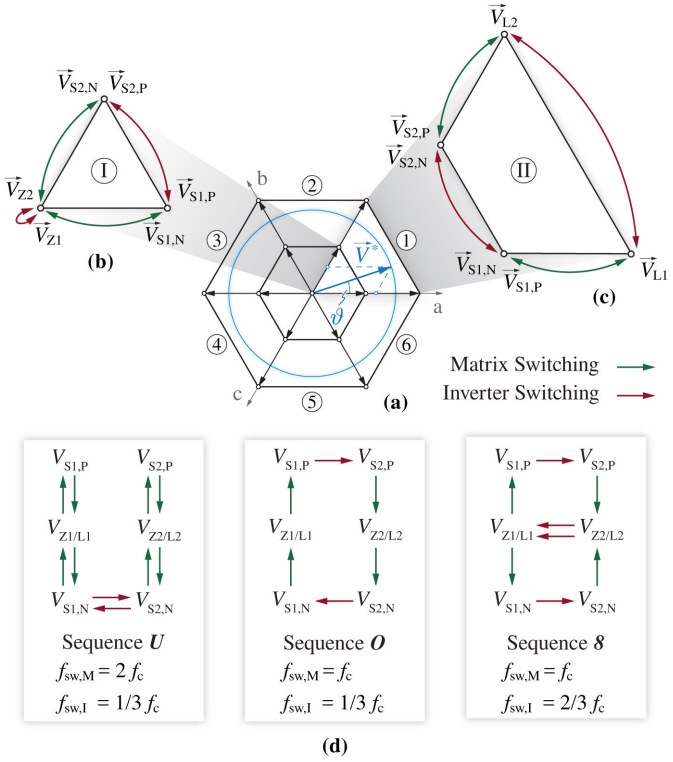

Fig. 2. (a) 3-L SNPCC output voltage space vector hexagon [26] and available voltage vectors in sector ① for (b) area ① and (c) area ②, where $\vec{V}_{\mathbf{Z}}$, $\vec{V}_{\mathbf{S}}$, and $\vec{V}_{\mathbf{L}}$ indicate zero, small, and large vectors, respectively (see Table II). Note that two different types of small vectors, $\vec{V}_{\mathbf{S,P}}$ and $\vec{V}_{\mathbf{S,N}}$, generate the same output voltage but result in different directions of the dc-link midpoint current i_m (see Fig. 1), which facilitates dc-link midpoint balancing. Note further that switching transitions of the inverter stage lead to vector state changes in the tangential direction indicated with **red** arrows, whereas switching transitions of the matrix stage lead to vector state changes in the normal direction indicated with **green** arrows. Furthermore, (d) presents the three most interesting switching state sequences within one switching period and lists the resulting effective switching frequencies $f_{sw,M}$ of the 3-L matrix stage and $f_{sw,I}$ of the 2-L inverter stage [26]. Note that these three modulation sequences, i.e., sequence *U*, sequence *O*, and sequence *8*, are valid for operation in both areas when the respective vectors are used, e.g., $\vec{V}_{\mathbf{Z}}$ in area ① and $\vec{V}_{\mathbf{L}}$ in area ②.

injection and thermal decoupling between two in-situ loss measurement blocks are carefully checked with finite-element method (FEM) simulations. Aiming for comprehensive verification, we consider three different modulation sequences [the symmetric sequence *U*, and the asymmetric sequences *8* and *O*, see Fig. 2(d)]. Third, in addition to the semiconductor losses, these sequences regarding their different impact on the output current quality and/or the filtering effort are also compared. In a generic way, this can be quantified by measuring the specific HF CM and DM voltage-time area ripples resulting from operation with a given modulation sequence. Thus, a comprehensive experimental characterization of a 3-Φ 3-L SNPCC demonstrator is provided.

This article starts with a brief description of the SNPCC operating principle and suitable modulation sequences in Section II, with Section II-C focusing on the nonstandard commutations observed when operating in area ① of the space vector plane [see Fig. 2(b)]. Section III then provides a comprehensive semiconductor loss modeling method that includes also the resulting extra losses in area ①. Next, Section IV presents a built 7.5-kW 3-Φ 3-L SNPCC hardware demonstrator and introduces a new in-situ calorimetric loss measurement method enabling accurate measurement of the 3-L matrix stage and 2-L inverter stage semiconductor losses. Section V considers all the measurement results to verify the proposed loss modeling approach and to experimentally compare the three different modulation sequences regarding semiconductor losses and DM/CM voltage-time area ripples. Finally, Section VI concludes this article.

TABLE I
CONSIDERED SNPCC NOMINAL OPERATING CONDITIONS AND DEMONSTRATOR SPECIFICATIONS

Parameter	Description	Value
V_{dc}	dc-link voltage	800 V
M	Modulation index	0.85
$\hat{V}$	Output phase voltage amplitude	340 V
$\hat{I}$	Output phase current amplitude	14.7 A
$\cos\phi$	Power factor	1
P_{out}	Output power	7.5 kW
f_{out}	Output fundamental frequency	$0 \sim 300$ Hz
f_c	Carrier frequency	16 kHz

II. SNPCC OPERATING PRINCIPLE

The SNPCC features a two-stage cascaded structure, composed of a 3-L matrix stage and a 3-Φ 2-L inverter stage, as shown in Fig. 1. The matrix stage creates a 3-L switched rail-to-rail voltage $v_{hl} \in \{0, V_{dc}/2, V_{dc}\}$. Thus, 3-Φ 3-L switched voltages v_{abc} are available at the 3-Φ 2-L inverter stages' output terminals, which leads to a reduced HF harmonic current stress of a supplied electric machine. Furthermore, 1/3-PWM can be implemented (see Fig. 3) to achieve lower switching losses of the inverter stage by always only operating one out of its three bridge-legs with PWM while clamping the other two bridge-legs to either the positive or the negative rail [26], [36]. The converter specifications and nominal operating conditions considered in the following are summarized in Table I.

A. Converter Switching States

The 3-L SNPCC generates 3-Φ output voltages with sinusoidal fundamental motor phase voltage components using SVPWM. However, different from conventional 3-Φ 3-L converters, e.g., 3-L NPC or 3-L T-type converters, only three types of space vectors exist, i.e., zero vectors $\vec{V}_{\mathbf{Z}}$ with an amplitude of 0, small vectors $\vec{V}_{\mathbf{S}}$ with an amplitude of $V_{dc}/3$, and large vectors $\vec{V}_{\mathbf{L}}$ with an amplitude of $2V_{dc}/3$, as shown in Fig. 2(a). Furthermore, in contrast to the conventional 3-L topologies, medium vectors with an amplitude of $\sqrt{3}V_{dc}/3$ cannot be generated. There are two types of redundant (i.e., resulting in equal output voltages) small vectors, $\vec{V}_{\mathbf{S,P}}$ and $\vec{V}_{\mathbf{S,N}}$, which result in opposite directions of the current i_m flowing into the capacitive dc-link midpoint, which, thus, can be balanced by appropriately selecting among the redundant vectors.

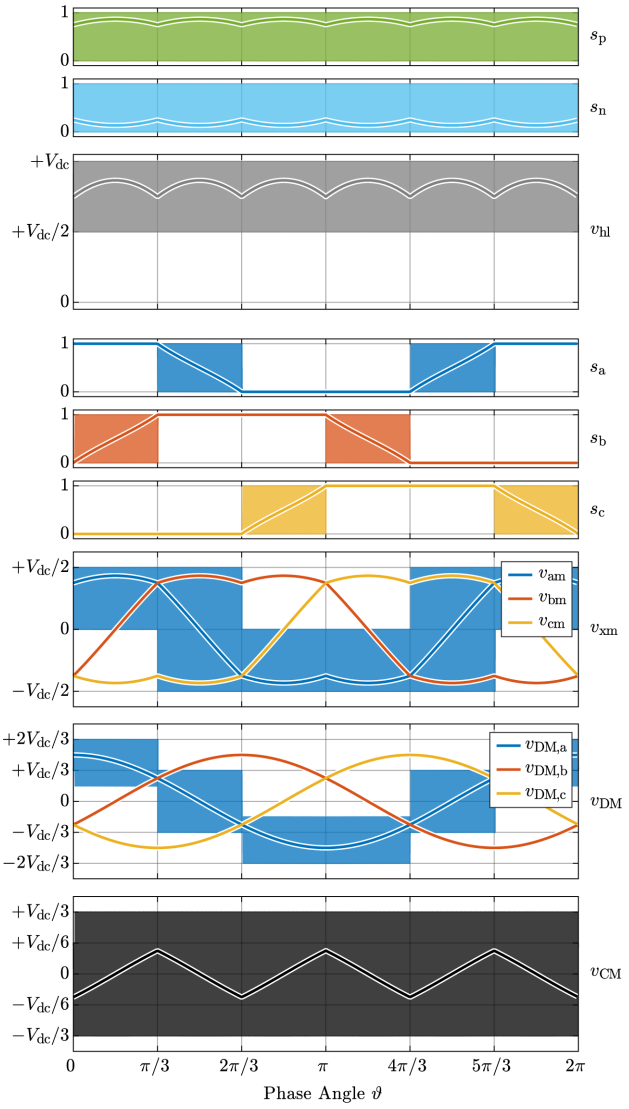

Fig. 3. Bridge-leg switching functions s_p, s_n, s_a, s_b, and s_c, inverter-stage dc rail-to-rail voltage v_{hl}, 3-Φ switched output voltages v_{am}, v_{bm}, and v_{cm} together with their corresponding DM components $v_{DM,a}$, $v_{DM,b}$, and $v_{DM,c}$, and injected triple fundamental frequency CM voltage v_{CM} when operating with sequence U in area Ⅱ ($M = 1$) over one fundamental output period; besides the switched voltage waveforms, respective local average waveforms are also shown as solid lines. Note that the inverter stage operates with 1/3-PWM; i.e., only one out of the three bridge legs is PWM-operated at any given time.

The inverter-stage output voltage space vector is defined by the five bridge-leg switching functions

$$s_x = \begin{cases} 0, & \text{if } T_{x,h} \text{ off}, \ T_{x,l} \text{ on} \\ 1, & \text{if } T_{x,h} \text{ on}, \ T_{x,l} \text{ off}, \end{cases} \quad x \in a, b, c, p, n \tag{1}$$

as listed in Table II considering sector ① as an example. The modulation index is defined as follows:

$$M = \frac{V^*}{1/2\, V_{dc}} \tag{2}$$

where V^* is the amplitude of the 3-Φ output phase voltage reference. Note that, as can be derived from geometric considerations in Fig. 2(a) [26], the two areas (① and Ⅱ) of the SNPCC space vector plane are defined by the boundary

$$M_{lim} = \frac{1}{\sqrt{3}\cos(\theta - \pi/6)} \tag{3}$$

i.e., if $M < M_{lim}$ [see Fig. 2(b)], the converter operates in area ① using zero and small vectors; otherwise [see Fig. 2(c)], it operates in area Ⅱ using small and large vectors.

TABLE II
SUMMARY OF AVAILABLE VOLTAGE SPACE VECTORS, CORRESPONDING BRIDGE-LEG SWITCHING FUNCTIONS, AND VECTOR AMPLITUDES IN SECTOR ① (SEE FIG. 2)

Vector	s_p	s_n	s_a	s_b	s_c	$\lvert\vec{V}\rvert$
$\vec{V}_{Z1}$	0	1	1	0	0	0
$\vec{V}_{Z2}$	0	1	1	1	0	0
$\vec{V}_{S1,P}$	1	1	1	0	0	$V_{dc}/3$
$\vec{V}_{S1,N}$	0	0	1	0	0	$V_{dc}/3$
$\vec{V}_{S2,P}$	1	1	1	1	0	$V_{dc}/3$
$\vec{V}_{S2,N}$	0	0	1	1	0	$V_{dc}/3$
$\vec{V}_{L1}$	1	0	1	0	0	$2V_{dc}/3$
$\vec{V}_{L2}$	1	0	1	1	0	$2V_{dc}/3$

B. Modulation Strategies

The many available switching states, including the redundant small vectors, enable a variety of switching sequences [26], i.e., sequences of switching states applied in one switching period. These can be grouped into two categories, symmetric and asymmetric sequences. Symmetric sequences are always mirrored with respect to the center of a switching period, whereas asymmetric sequences are missing this symmetry property. However, advantageously, asymmetric switching sequences can optimize the harmonic profile and reduce the number of switching instants [37], [38], [39]. Furthermore, each switching sequence results in specific ratios of the *effective* switching frequencies of the 3-L matrix stage, $f_{sw,M}$, and the 2-L inverter stage, $f_{sw,I}$, to the carrier frequency, f_c.

Among all possible modulation strategies, only the ones with full control of the midpoint current i_m; i.e., those that employ all redundant small vectors in one switching period are considered. Thus, three interesting modulation schemes are analyzed in this article [see Fig. 2(d)]. Sequence U, which has already been tested experimentally in [27], is selected as state-of-the-art symmetric modulation sequence [25]. Second, the asymmetric sequence O, where only six switching transitions occur in one switching period, and hence, a considerable reduction of switching losses is achieved (note that the effective switching frequency of the 3-L matrix stage reduces to $f_{sw,M} = f_c$), is considered. Finally, sequence 8 is identified as the preferred candidate due to relatively low switching losses (note the minor increase of the 2-L inverter-stage effective switching frequency to $f_{sw,I} = 2/3\, f_c$) and fairly small HF DM voltage-time area ripple (i.e., ultimately ensuring small motor phase current ripple). Note that, however, such asymmetric

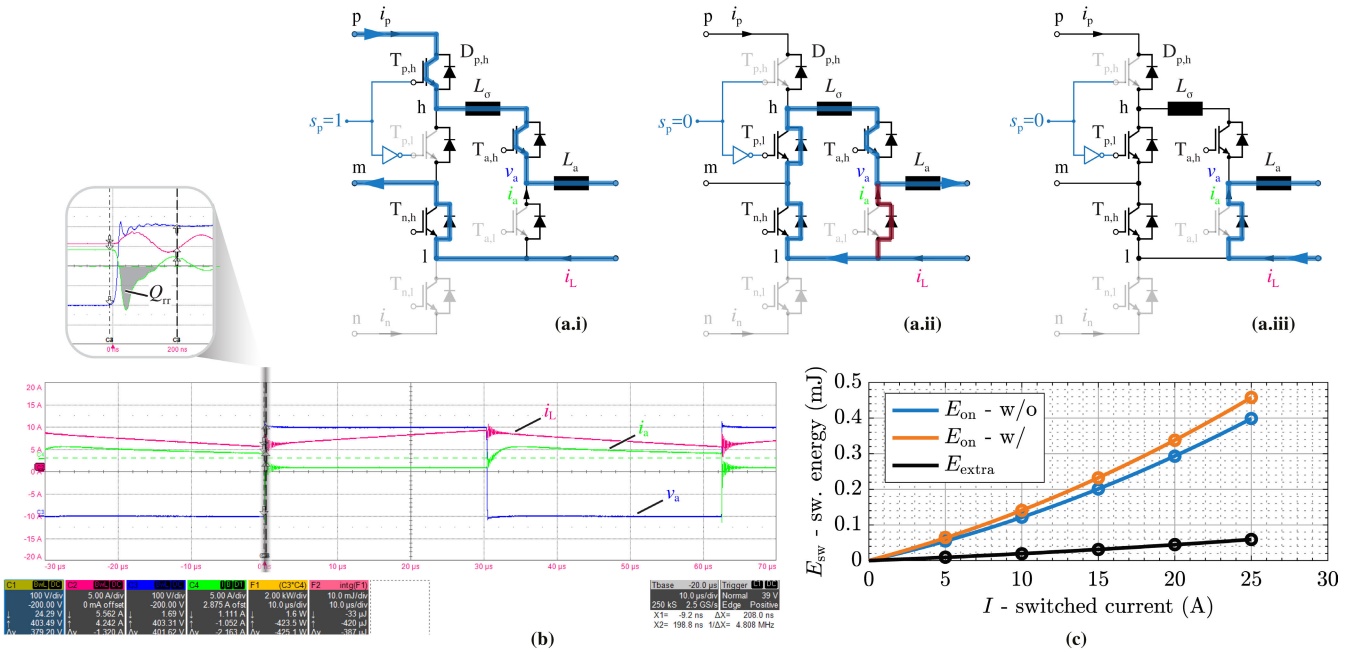

Fig. 4. Verification of hybrid commutations appearing for operation in area ① when switching between the zero vector $\vec{V}_{\mathbf{Z}}$ and a small vector $\vec{V}_{\mathbf{S}}$, considering a simplified 1-Φ cascaded dc/dc circuit composed of the matrix stage and the phase-a bridge-leg where the parasitic inductor L_σ and the phase-a boost inductor L_a are shown. (a.i) Switching states when s_p switches from 1 to 0, but $T_{n,h}$ and $T_{a,h}$ are always on; i.e., when $s_p = 0$ ($s_p = 1$), phase-a's operating state is identical to its state with $\vec{V}_{\mathbf{Z}}$ ($\vec{V}_{\mathbf{S}}$) generated by the 3-Φ 3-L SNPCC. (a.ii) and (a.iii) Redistribution of the load current between $T_{a,h}$ and the antiparallel diode of $T_{a,l}$ during the zero state. (b) Measured [using the demonstrator shown in Fig. 5(a)] switched voltage v_a (100 V/div), output inductor current i_L (5 A/div), and phase-a low-side device current i_a (5 A/div). The zoomed waveforms at the turn-on instant of $T_{p,h}$, i.e., upon leaving the zero state when s_p switches from 0 to 1, clearly show the reverse recovery of $T_{a,l}$'s antiparallel diode, i.e., a hybrid commutation between that diode and the turning-on matrix stage transistor. (c) Extra turn-on losses in $T_{p,h}$ are obtained by subtracting the turn-on energy with and without the cascaded inverter bridge leg present, using simulations based on the manufacturer's SPICE models [41].

modulation sequences come with a special implementation challenge: different from conventional 2-L or 3-L converters, there is no fixed (i.e., with respect to the start of a switching period) point in time at which the sampled instantaneous current equals the local average value over one switching period [40]. However, this issue can be easily addressed considering today's high-performance FPGAs and ADCs that facilitate oversampling and local averaging.

A detailed circuit simulation (see Fig. 3) further illustrates the converter operating principle for an exemplary operating point with $M = 1$ and sequence U. Note that always only one bridge leg out of the inverter stages' three bridge-legs actively switches, and the switching functions of the other two phases are clamped to either 0 or 1. This 1/3-PWM operation saves switching losses as a consequence of the elimination of the (inverter) zero states. Note that 1/3-PWM is only possible when the matrix stage generates a rail-to-rail voltage v_{hl} whose local average equals the envelope of the absolute values of the 3-Φ line-to-line output voltage references. Furthermore, the 3-Φ switched output voltages v_{am}, v_{bm}, and v_{cm} together with their corresponding DM components $v_{DM,a}$, $v_{DM,b}$, and $v_{DM,c}$ are shown. The injected CM voltage v_{CM} is necessary to achieve 1/3-PWM, where the two inverter phases with the maximum and the minimum phase voltages are clamped without switching.

C. Hybrid Commutations in Area ①

While the 3-L SNPCC operates in area ⑪ [see Fig. 2(c)], only conventional half-bridge commutations occur; e.g., switching between $\vec{V}_{\mathbf{L1}}$ and $\vec{V}_{\mathbf{S1}}$ ($\vec{V}_{\mathbf{L2}}$) leads to a commutation within the matrix stages' lower half-bridge (within the inverter stage's phase-b half-bridge), as indicated by the green (red) arrows in Fig. 2(c). Similarly, when operating in area ① [see Fig. 2(b)], such standard half-bridge commutations also occur during the switching transitions between $\vec{V}_{\mathbf{S1}}$ and $\vec{V}_{\mathbf{S2}}$.

However, a special case occurs for operation in area ① when switching between zero vectors and small vectors (e.g., between $\vec{V}_{\mathbf{Z1}}$ and $\vec{V}_{\mathbf{S1,N}}$), because the zero vector is not realized with the inverter stage (1/3-PWM) but by the matrix stage setting $v_{hl} = 0$, regardless of the inverter stages' switching state. During this zero state, the phase currents may, depending on their direction and the inverter stages' switching state, redistribute from inverter-stage IGBTs to their complementary diodes; a process driven by the differences in voltage drops across the involved power semiconductors. To leave the zero state, matrix stage switches and applies $v_h > 0$. During this transition, inverter-stage diodes that have taken over current during the zero state are forced to commutate their current *by the matrix stage*; i.e., there is a *hybrid* commutation that gives rise to reverse-recovery losses in those diodes and correspondingly higher turn-on losses in the matrix-stage transistors.

In the following, the simplified 1-Φ cascaded dc/dc circuit configuration shown in Fig. 4(a) (i.e., in essence a simplified 1-Φ version of the 3-L SNPCC) is implemented to explain and characterize these hybrid commutations. Specifically, this dc/dc circuit consisting of the matrix stage and the phase-a bridge-leg enables an exemplary analysis using two phase-a

operating states; i.e., $T_{n,h}$ and $T_{a,h}$ are always on, and $s_p = 1$ ($s_p = 0$) identifies the phase-a half-bridge operating state corresponding to $\vec{V}_S$ ($\vec{V}_Z$) in sector ① of area Ⓘ. When $s_p = 1$ [see Fig. 4(a.i)], the phase-a output terminal is connected to p, and the phase inductor (motor winding) current i_L flows through $T_{p,h}$ and $T_{a,h}$. After switching s_p from 1 to 0, the current i_L directly commutates in the upper matrix stage half-bridge to $T_{p,l}$ and $v_{pn} = 0$. Hence, also, the output voltage is zero. However, a second path exists for the load current [see the red highlight in Fig. 4(a.ii)]; i.e., i_L could close its path also through $T_{a,l}$'s antiparallel diode without flowing through the matrix stage. The voltage drops across the matrix stage switches ultimately cause a gradual commutation of i_L to $T_{a,l}$'s antiparallel diode [see the measured i_a in Fig. 4(b)]. The extent of this current redistribution as well as the commutation speed depends on the semiconductor (IGBTs and diodes) forward voltage drops, ON-state resistances, and the parasitic inductance L_σ, which is here about 40 nH. For the considered device configuration, it takes approximately 2 µs until the major share of i_L flows through $T_{a,l}$ values, as shown in Fig. 4(a.iii). Note that forward voltage drops of IGBTs and diodes are current-dependent, which has a strong impact on the final current distribution. When s_p switches back from 0 to 1 (i.e., an active vector is applied), the antiparallel diode of $T_{a,l}$ must become reverse-biased as $v_{hl} > 0$, and hence, essentially, a commutation between this diode and the turning-on matrix-stage transistor $T_{p,h}$ occurs. Clearly, this *hybrid* commutation causes reverse-recovery losses in $T_{a,l}$'s antiparallel diode [see the zoomed-in view in Fig. 4(b)] and also generates considerable extra turn-on losses in $T_{p,h}$, which can be quantified using manufacturer's SPICE models [see Fig. 4(c)].

The hybrid commutation behavior in the 3-Φ 3-L SNPCC can be analyzed by extension of the aforementioned 1-Φ cascaded dc/dc circuit; i.e., two more bridge-legs and their corresponding load inductor currents are added and paralleled to the existing 1-Φ bridge leg. However, the commutation follows the same hybrid pattern. After switching from $\vec{V}_S$ to $\vec{V}_Z$, the rail current i_h, i.e., the sum of the 3-Φ load inductor currents, immediately commutates to the two inner semiconductors of the matrix stage, $T_{p,l}$ and $T_{n,h}$ [similar to Fig. 4(a.i)], to achieve zero output voltages in all three phases. Note that the switching state of the 3-Φ inverter stage does not change compared with the earlier active vector $\vec{V}_S$, as the matrix stage realizes the zero vector. However, alternative paths exist for the 3-Φ load inductor currents; i.e., the antiparallel diodes of the respective second half-bridge switches could also provide the conduction path. At the start of the zero vector interval, these load inductor currents still flow through the IGBT transistors as in the previous state $\vec{V}_S$. But, the voltage drop across the inner matrix-stage switches ($T_{p,l}$ and $T_{n,h}$) causes a gradual current commutation/redistribution of the 3-Φ load inductor currents [similar to Fig. 4(a.iii)], which is heavily dependent on the semiconductor (IGBTs and diodes) forward voltage drops and ON-state resistances. Considering the applied transistors, very quickly, the 3-Φ load inductor currents circulate almost entirely in the inverter stage, and only a very small leakage current still flows through the inner matrix stage switches. This behavior [see measurement in Fig. 4(b)] can be accurately captured by circuit simulations with the PLECS software tool. Note that still zero output voltages are ensured effectively by the inverter stage but not the matrix stage. Ultimately, upon leaving the zero vector state, all diodes that have taken over current from the two inner matrix stage switches will be commutated by the turning-on matrix-state transistor, leading to hybrid commutations. These hybrid commutations and the corresponding extra losses are considered in the semiconductor loss modeling approach for operation in area Ⓘ introduced in Section III-B below.

III. Semiconductor Loss Modeling

Considering silicon IGBTs and diodes, the loss modeling in areas Ⓘ and Ⓘ is explained comprehensively in this section, targeting implementations in circuit simulation software packages, such as PLECS. The underlying loss data are obtained from manufacturer datasheets and SPICE models [41]. To improve the loss modeling accuracy, an electrothermal coupling method is applied; i.e., for all parameters, a linear dependency on the junction temperature T_j is considered by the function

$$f(T_j) = 1 + k_T(T_j - T_0) \tag{4}$$

where k_T is the temperature coefficient, and $T_0 = 25$ °C is the base temperature [45].

A. Basic Loss Modeling

The basic IGBT loss models have been comprehensively presented in [42], [43], and [44]. The conduction state of the silicon IGBTs and diodes is modeled by a constant voltage source V_f, i.e., the forward voltage drop in diodes or the collector–emitter saturation voltage in IGBTs, and a series-connected differential resistance r_{on}. Thus, the conduction losses are calculated as

$$P_{cond} = \left(V_f I_{avg} + r_{on} I_{rms}^2\right) \cdot f(T_j) \tag{5}$$

where I_{avg} and I_{rms} refer to the average and the rms currents flowing through the device.

The IGBT switching losses are the sum of all turn-on and turn-off switching energies E_{sw}, whose dependency on the switched voltage and the switched current can be modeled in a polynomial form, i.e., a linear dependency on the switched voltage V_{sw} and a quadratic dependency on the switched current I_{sw} as

$$E_{sw} = V_{sw} \cdot \left(k_{sw} + k_{sw1} I_{sw} + k_{sw2} I_{sw}^2\right) \cdot f(T_j). \tag{6}$$

Similarly, the diode reverse recovery loss energy E_{rr} is modeled as

$$E_{rr} = V_{sw} \cdot (k_{rr0} + k_{rr1} I_{sw}) \cdot f(T_j). \tag{7}$$

A linear approximation is applied for the considered semiconductors, since the quadratic term can be neglected without sacrificing accuracy.

The transistors of the matrix stage always switch half of the dc input voltage, i.e., $V_{dc}/2$, whereas the semiconductors

TABLE III
SUMMARY OF SELECTED SEMICONDUCTORS TOGETHER WITH THEIR CONDUCTION AND SWITCHING LOSS MODEL PARAMETERS [42], [43], [44] BASED ON DATASHEET INFORMATION

Model		Conduction Losses				Turn-on Losses				Turn-off Losses			
Series #	Device	V_f (V)	k_T	r_{on} (mΩ)	k_T	k_0	k_1	k_2	k_T	k_0	k_1	k_2	k_T
IKZ75N65ES5	IGBT	0.71	-1.3 E-3	17	2.3 E-3	378 E-9	34.8 E-9	3.09 E-12	3.4 E-3	85.1 E-9	30.4 E-9	178 E-12	2 E-3
	Diode	0.77	-3.4 E-3	17	4.2 E-3	/	/	/	/	52.8 E-9	8.03 E-9	/	25.7 E-3
IKW40N120CS6	IGBT	0.81	-1.1 E-3	36.4	3.2 E-3	269 E-9	93.5 E-9	384 E-12	2.6 E-3	214 E-9	58.8 n	5.34 E-12	5.9 E-3
	Diode	0.89	-2.1 E-3	48.2	1.7 E-3	/	/	/	/	41.3 E-9	51.2 E-9	/	23.7 E-3

of the inverter stage switch either $V_{dc}/2$ or V_{dc} depending on the switching state of the matrix stage. Therefore, 650-V silicon IGBTs (*Infineon IKZ75N65ES5*) are employed in the matrix stage and 1200-V devices (*Infineon IKW40N120CS6*) in the inverter stage. Considering these devices, Table III lists the coefficients for the described conduction and switching loss models, which are applied to calculate 3-L SNPCC system losses in Section V, by implementing the device loss characteristics in a PLECS circuit simulation.

B. Area ① Loss Modeling

Whereas this basic semiconductor loss model can accurately capture the losses during operation in area ⑪ (only standard half-bridge commutations occur, and hence, datasheet-based loss models are sufficient), the hybrid commutations between $\vec{V}_{\mathbf{Z}}$ and $\vec{V}_{\mathbf{S}}$ when operating in ① incur additional losses (see Section II-C). Thus, a complete area ① semiconductor loss model should include two more loss contributions, i.e., the additional reverse-recovery losses generated in the inverter stage [see Fig. 4(b)] and the corresponding extra turn-on losses in the matrix stage caused by the reverse-recovery charge [see Fig. 4(c)].

Significant reverse recovery losses are generated when switching back from $\vec{V}_{\mathbf{Z}}$ to $\vec{V}_{\mathbf{S}}$ in the inverter-stage diodes, which do not conduct originally in $\vec{V}_{\mathbf{S}}$ but are taking over currents due to the hybrid commutation. As mentioned, this current redistribution phenomenon can be accurately captured by circuit simulations, and hence, the reverse recovery losses can be obtained with the same datasheet-based loss models used for area ⑪ and described in Section III-A.

However, hybrid commutations cause higher turn-on losses in the matrix stage transistor compared with the datasheet values (given for symmetric half-bridges); see Fig. 4(c). Therefore, a different model for the turn-on energies of the matrix-stage switches must be employed for operation in area ①. Note that the extra turn-on losses of $T_{p,h}$, when switching back from $\vec{V}_{\mathbf{Z}}$ to $\vec{V}_{\mathbf{S}}$, are dependent on the *total* reverse recovery charge flowing through this transistor, which, however, might originate from one or more inverter diodes that have taken over current during the zero vector state. Assuming a linear relationship between current and reverse-recovery charge, which is reasonable for the current levels used in the demonstrator system, the extra turn-on energy depends only on the total turn-on current. It can be calculated using SPICE simulations and detailed device models available from the manufacturer [see Fig. 4(c)] and fit with a quadratic polynomial, such as (6), as a function of the turn-on current I_{sw} with the coefficients

$$k_{sw0} = 0.25\ \text{E-9}, \quad k_{sw1} = 4.19\ \text{E-9}, \quad k_{sw2} = 71.7\ \text{E-12}. \tag{8}$$

The temperature dependency is neglected without sacrificing accuracy in this case [see Fig. 4(c)].

IV. HARDWARE DESIGN AND IN-SITU CALORIMETRIC SEMICONDUCTOR LOSS MEASUREMENT

To experimentally quantify the 3-L SNPCC performances, e.g., the semiconductor losses and the DM/CM ripples resulting from different modulation strategies, and to validate the estimation of semiconductor losses especially in area ① using the proposed modification of the loss models, a hardware demonstrator is built, and a novel in-situ calorimetric semiconductor loss measurement method is implemented.

A. Hardware Implementation

The hardware demonstrator is shown in Fig. 5(a). Note that the 3-L SNPCC power PCB layout features a challenging design originating from the direct connection between the matrix and the inverter stage without any passive filtering components in between. All commutation loops of the inverter stage half-bridges always involve the upper, the lower, or both dc-link capacitors and, thus, also the matrix-stage switches. Therefore, to reduce the commutation loop area and the inductance originating from it, the two interconnecting rails **h** and **l** should be routed as close as possible to each other. However, the capacitive coupling between the corresponding traces or polygons directly increases the parasitic output capacitance of the matrix stage semiconductors and, thus, increases the switching losses (from capacitive charging/discharging currents). The selected routing [see Fig. 5(b)], thus, minimizes the overlap of the **h** and **l** polygons but still places them as close as possible to each other.

B. In-Situ Calorimetric Semiconductor Loss Measurement

Calorimetric semiconductor loss measurement methods directly capture losses and, thus, achieve high accuracy, as they avoid the need for measuring voltage and current overlaps of switching transients with high dv/dt and high di/dt [46], [47], [48], [49]. In a typical setup, the analyzed power

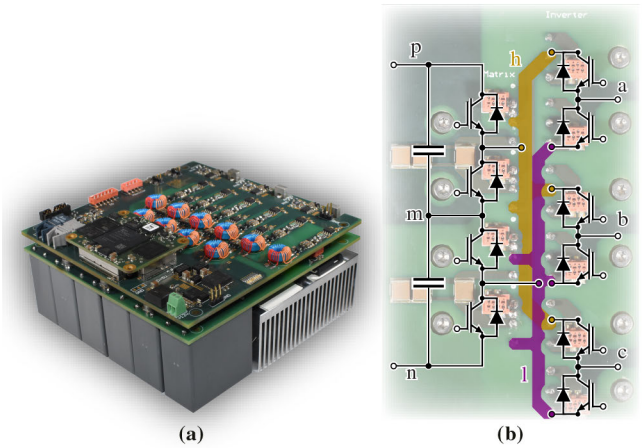

Fig. 5. (a) Hardware demonstrator of the 7.5-kW 3-Φ 3-L SNPCC and (b) PCB layout of the power stage, highlighting the polygons connecting the matrix stage and the inverter stage. The arrangement of these planes corresponding to the rails **h** (yellow) and **l** (purple) is governed by the trade-off between minimizing the capacitive coupling (to reduce the according capacitive charging/discharging losses during switching) and minimizing the commutation loop inductance for the inverter stage half-bridges. Thus, rails **h** and **l** are placed as close as possible to reduce the enclosed area but without overlapping to still minimize the parasitic capacitance.

semiconductor is mounted on a metal (brass[1]) block that is thermally insulated from the ambient. Thus, if (constant) losses P are generated in the semiconductor and injected into the metal block, its temperature linearly increases over time with a slope that depends on the block's thermal capacitance $C_{\text{th,br}}$ and is proportional to P. $C_{\text{th,br}}$ can be obtained from calibration with known loss injection. Then, conversely, using the physical relationship among heat capacitance, temperature change, and energy, the semiconductor losses P can be obtained from the recorded temperature increase ΔT over time Δt as follows:

$$P = C_{\text{th,br}} \cdot \frac{\Delta T}{\Delta t}. \tag{9}$$

Typically, this (and similar) approaches are employed to measure (switching) losses of individual devices or half-bridge configurations using dedicated test setups. In this article, we employ an in-situ approach and directly measure the total stage-level (i.e., matrix or inverter) semiconductor losses using the full converter system by replacing the heat sink with two insulated brass blocks (one for the matrix stage and one for the inverter stage), as shown in Fig. 6. This in-situ approach has the advantage of accounting for all realization-specific (parasitic) effects, such as commutation loop layouts, gate drivers, and so on, and it allows a clear insight into the system's loss breakdown for different operating points and modulation sequences.

The brass block size is designed to target a suitable temperature rise time over the whole range of expected losses; i.e., measurements with smaller brass blocks lead to faster measurements but require a higher temperature sampling rate to ensure accuracy [46]. The realized brass blocks 26 × 54 × 106 mm) are shown integrated in the final converter in Fig. 6(c).

[1]Brass is usually selected because of its high thermal capacitance per volume.

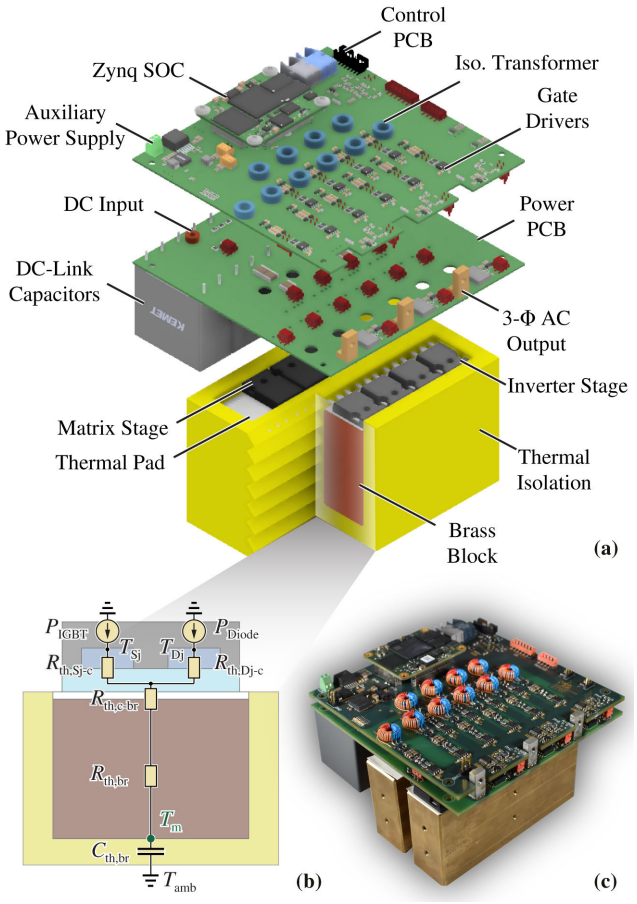

Fig. 6. (a) In-situ calorimetric semiconductor loss measurement setup, where the heat sink is replaced by two thermally insulated brass blocks to measure the matrix-stage and inverter-stage semiconductor losses, respectively. (b) Detailed equivalent thermal network for one TO-247 package (including one IGBT and one diode) and (c) photograph of the realized measurement setup.

Fig. 6(b) shows the exemplary thermal network for one semiconductor package. Each IGBT (diode) injects its losses P_{IGBT} (P_{diode}) from the chip through the thermal resistances $R_{\text{th, Sj-c}}$ ($R_{\text{th, Dj-c}}$) in parallel to the common case and then through the thermal resistance $R_{\text{th, c-br}}$ into the brass block. The temperature of the brass block T_{m} is captured at the center of the block's bottom surface by means of a fiber optic thermometer [50]. Therefore, the thermal resistivity of the brass block results in a semiconductor-position-dependent additional thermal resistance contribution indicated by $R_{\text{th,br}}$.

Different from single-component or half-bridge calorimetric measurements, the corresponding heat spreading effect and the resulting temperature gradients play an important role in the new in-situ calorimetric measurement approach regarding the placement of the temperature sensor, because, e.g., the loss distribution among the four matrix stage semiconductors varies largely between different operating points. Two exemplary extreme cases are tested using FEM simulations with the total losses of 60 W injected either only in the two outer or in the two inner semiconductors, as shown in Fig. 7(a) and (b), respectively.

Clearly, the height of the brass block must be sufficient for the temperature at the sensor location (center of the

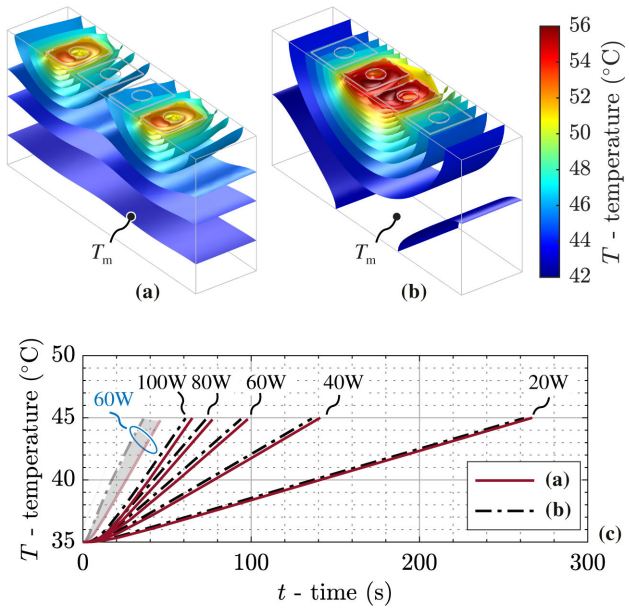

Fig. 7. FEM simulations of the inverter stage brass block temperature distributions at $t = 80$ s considering 60 W of total losses symmetrically injected from two different regions, i.e., (a) only the two outer or (b) only the two inner semiconductors dissipate losses. (c) By comparing the recorded temperatures T_m over the heating time considering different losses and two injection regions, it is confirmed that the total amount of losses can be accurately measured regardless of the loss injection region. This is facilitated by ensuring a tall enough brass block to leverage the heat spreading effect. Note that if the brass block is cut into half of the designed height and, thus, steeper temperature evolution curves (blue) result from loss dissipation of 60 W, a considerable difference of measurement results for heat injection in the two different regions is observed (gray shading).

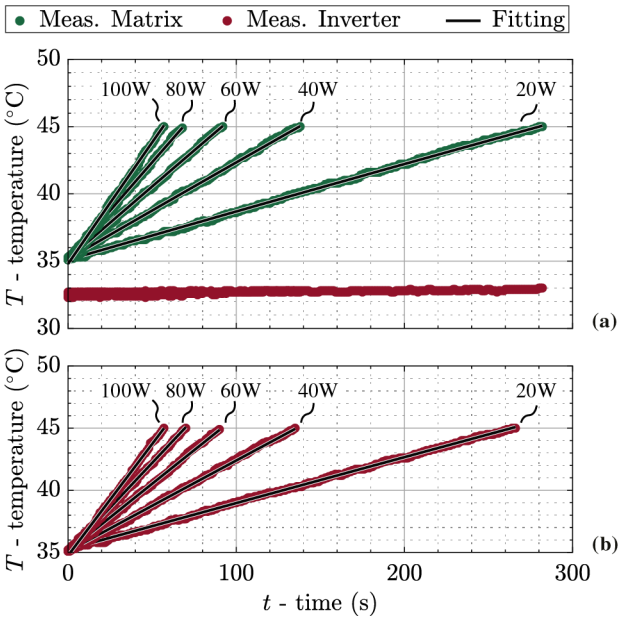

Fig. 8. Brass block calibration results for (a) matrix stage and (b) inverter stage. Note that during the calibration of the matrix stage with 20–100 W, the inverter-stage block temperatures [red in (a)] always stay at the room temperature, which confirms very good thermal insulation (decoupling) between the two brass blocks.

bottom surface) to be rather independent of the loss injection distribution on the top surface. Considering the designed brass blocks, the simulated temperature T_m change over time shown in Fig. 7(c) indicates negligible differences in the resulting temperature slopes when injecting losses from different regions. For example, a maximum slope difference of 4.85% is obtained for a total loss dissipation of 100 W. The importance of considering the heat spreading effect or the actual temperature distribution is further highlighted with a test considering half of the current brass block height with 60-W injected losses [blue in Fig. 7(c)], where a 25.4% slope difference [shaded area in Fig. 7(c)] can be calculated. For the original brass block height of 54 mm footprint of 26 × 106 mm), a 4.4% difference of the slope of the temperature increase over time and/or sufficient accuracy of the final loss measurements can be guaranteed.

The experimental setup with the designed brass blocks must be calibrated. Various known power losses in the range of 20–100 W are dissipated in the semiconductors using an external dc current source, and the brass block temperature T_m is recorded. The injected dc losses can be electrically measured (using *34410A* digital multimeters from *Keysight* Technologies [51]) with high precision. From this calibration data, the thermal capacitance $C_{th,br}$ can be extracted, taking into account all setup-specific non-idealities. The calibration measurements are shown in Fig. 8, which also demonstrates an almost perfect thermal decoupling of the two brass blocks used for the matrix and the inverter stage, respectively.

V. Measurement Results and Analysis

A 3-L SNPCC hardware demonstrator is built (see also Section IV), according to the specifications shown in Table I with 650-V silicon IGBTs (Infineon *IKZ75N65ES5*) in the matrix stage and 1200-V silicon IGBTs (Infineon *IKW40N120CS6*) in the inverter stage, to validate the operation under three typical modulation sequences, i.e., the state-of-the-art symmetric sequence *U*, the low-semiconductor-loss sequence *O*, and the low-DM-voltage-time-area-ripple sequence *8*. Furthermore, small differences between measured and calculated/simulated losses confirm the accuracy of the selected semiconductor loss modeling approach, especially also for operation in area ①.

The expected 3-L SNPCC losses presented below are calculated based on electrothermal simulations with the PLECS software [52], using the semiconductor loss models introduced earlier, including the modifications needed to correctly account for operation in area ①. The semiconductor models, e.g., ON-state resistance, forward voltage drop, and turn-on and turn-off energy, presented in Section III are integrated into this electrothermal simulation to calculate the component-level semiconductor losses, whereby the thermal model from Fig. 6(b) is implemented to accurately estimate the junction temperatures T_{Sj} of the IGBTs, and T_{Dj} of the diodes, assuming a fixed temperature at the bottom of the brass block of $T_m = 40$ °C, which is the median temperature when conducting the in-situ calorimetric measurement that uses a brass block temperature range of 35-45 °C. The conduction loss model, including ON-state resistance and forward voltage drop, ensures an accurate current distribution in the simulation, which is particularly important for the semiconductor loss calculation when the hybrid commutations occur in area ①; i.e., the current redistribution during the zero switching state directly determines

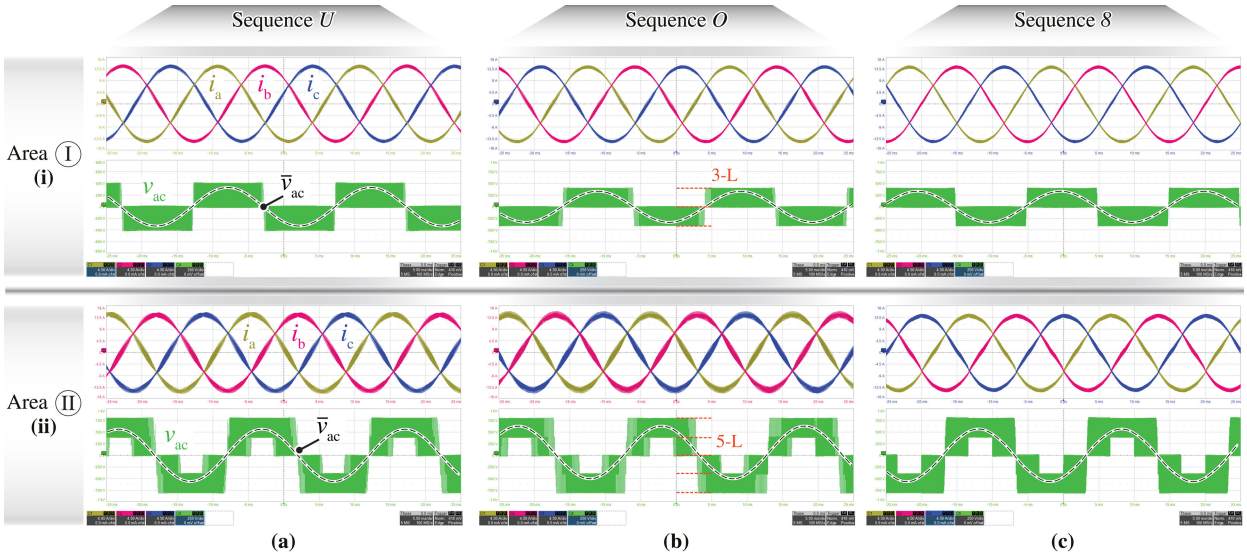

Fig. 9. Measured characteristic waveforms, i.e., 3-Φ output currents i_a, i_b, and i_c (4.5 A/div), and switched line-to-line voltage v_{ac} (250 V/div), of the 3-L SNPCC operating in (i) area Ⅰ ($M = 0.5$) and (ii) area Ⅱ ($M = 0.85$), under the ohmic fundamental load operation with a dc-link voltage of 800 V and an output fundamental phase current amplitude of 14.7 A. Three typical modulation sequences are considered, i.e., (a) state-of-the-art symmetric sequence *U*, (b) sequence *O* generating minimum semiconductor losses, and (c) sequence *8* with minimum DM current ripple [note the low current ripple in (c) compared with (a) and (b)]. The local average line-to-line $\bar{v}_{ac}$ is extracted from the exported oscilloscope waveforms and added on top of the screenshots as dashed lines for illustration purposes.

the reverse recovery losses generated in the inverter stage and the increased turn-on losses in the matrix stage, which are accounted for by using a different turn-on loss model for operation in area Ⅰ.

A. Experimental Waveforms

Fig. 9 verifies the 3-L SNPCC demonstrator operation considering the three discussed modulation sequences in both, area Ⅰ ($M = 0.5$) and area Ⅱ ($M = 0.85$), under the fundamental ohmic load operation (14.7-A phase current fundamental amplitude in phase with the output phase voltage) with a dc-link voltage of 800 V. Note that in area Ⅰ, the line-to-line output voltage v_{ac} switches between three level (0 and ±400 V) due to the low modulation index, whereas in area Ⅱ, a 5-L switched voltage waveform of v_{ac} (with levels $-V_{dc}$, $-(1/2)V_{dc}$, 0, $(1/2)V_{dc}$, and V_{dc}) is clearly observed.

B. Area Ⅱ Experimental Characterization

Fig. 10 comprehensively illustrates the 3-L SNPCC operation in area Ⅱ under the three considered modulation schemes. Fig. 10(i) shows the calculated/simulated and measured semiconductor losses for inverter operation with $V_{dc} = 800$ V and $M = 0.85$ as a function of the output current $\hat{I}_{out}$ under ohmic operation. Fig. 10(ii) shows the losses in dependence of the load phase angle ϕ for a constant apparent power $S = 7.5$ kVA, again with $V_{dc} = 800$ V and $M = 0.85$. In general, note the good agreement of calculated/simulated and measured losses. Clearly, sequence *O* generates the lowest semiconductor losses, especially when considering non-unity power factor. Using this low-switching-loss asymmetric modulation sequence *O*, the prototype achieves a semiconductor efficiency of 98.8% with effective switching frequencies of $f_{sw,M} = 16$ kHz (matrix stage) and $f_{sw,I} = 5.3$ kHz (inverter stage) at nominal ohmic load ($M = 0.85$).

Moreover, the CM and DM filtering effort can be quantified by the corresponding HF CM and DM voltage-time area ripples that the switching stage generates when operated with a certain modulation sequence. Ultimately, these voltage-time ripples determine the required HF flux handling capability of the CM and DM filter inductors, respectively. Therefore, Fig. 10(iii) [Fig. 10(iv)] compares the measured and calculated *envelopes* of the HF CM (DM) voltage-time (Vt) area ripple waveforms (ΔVt_{CM} and ΔVt_{DM}, respectively) at the nominal operating point. The voltage-time area ripples are obtained by integrating the measured 3-Φ switched voltage waveforms. The CM ripples are comparable among the sequences, but sequence *8* results in significantly lower DM voltage-time area ripple. In conclusion, sequence *8* is the best modulation sequence candidate under ohmic operation, considering similarly low semiconductor losses as sequence *O* but clearly reduced DM filtering effort. However, for applications that require a wide range of load phase angles ϕ, sequence *O* should be preferred due to the lower semiconductor losses.

C. Area Ⅰ Experimental Characterization

The SNPCC operation in area Ⅰ is validated in Fig. 11, where again the same three modulation schemes are considered and compared. The semiconductor losses, as a function of load phase angle ϕ under a constant apparent power of $S = 4.4$ kVA ($\hat{V} = 200$ V, $\hat{I} = 14.7$ A, $V_{dc} = 800$ V, and $M = 0.5$) are first recorded. Sequence *O* and sequence *8* generate similar semiconductor losses over a wide load phase angle range, as shown in Fig. 11(i). Importantly, the calculated/simulated semiconductor losses that consider hybrid commutations based on the modeling approach introduced in

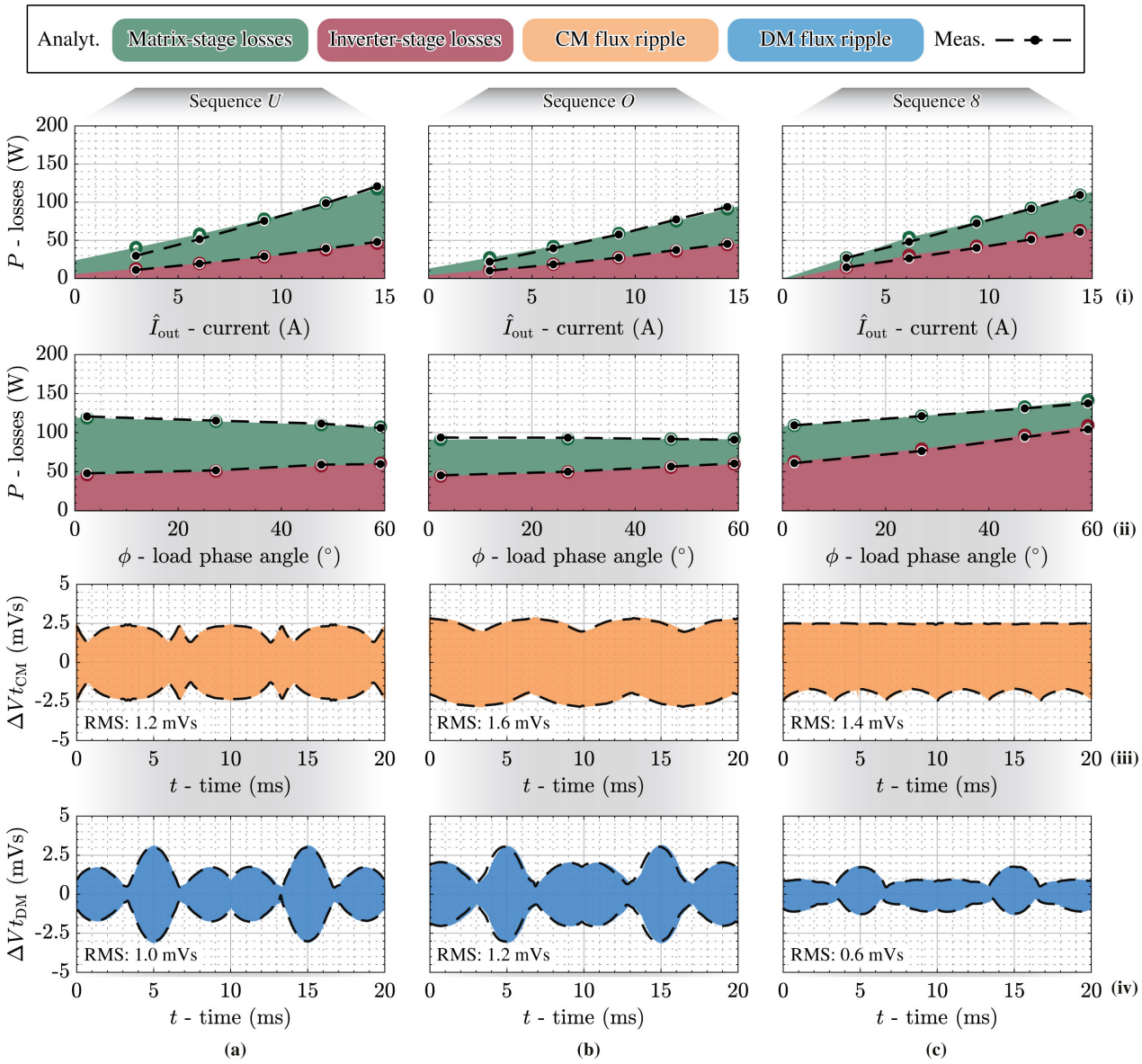

Fig. 10. Measurement results of 3-L SNPCC operation in area ⓫ ($V_{\text{dc}} = 800$ V and $M = 0.85$) with different modulation schemes, i.e., (a) switching state sequence U, (b) sequence O, and (c) sequence 8. The calculated and calorimetrically measured semiconductor losses are compared between the modulation sequences for (i) fundamental ohmic load operation and varying power level and (ii) under constant apparent power $S = 7.5$ kVA ($\hat{V} = 340$ V and $\hat{I} = 14.7$ A) and varying load power factor, i.e., output current and voltage fundamental phase shift ϕ. Note that the asymmetric modulation sequence O always generates the lowest semiconductor losses. Furthermore, (iii) shows the envelope of the HF CM voltage-time area ripple, and (iv) shows the envelope of the HF DM voltage-time area ripple waveforms at the nominal operating point ($V_{\text{dc}} = 800$ V, $M = 0.85$, and $\cos\phi = 1$). Note that the DM voltage-time area ripple of sequence 8 is significantly smaller compared with the other two sequences. In all cases, note the good agreement between calculated (colored swatches) and measured results (black dashed lines).

Section III-B, i.e., which consider additional reverse recovery losses in the inverter stage and extra turn-on losses in the matrix stage, agree well with the calorimetrically measured semiconductor losses. Table IV quantifies the significant modeling accuracy improvement by comparing the new model (i.e., simulation-based, which facilitates accurate accounting for hybrid commutations) with the conventional model used in [26] (fully analytic but, thus, unable to account for hybrid commutations).

Furthermore, Fig. 11(ii) and (iii) shows again the envelopes of the HF CM and DM voltage-time area ripple waveforms for ohmic operation, which are obtained by integrating the measured 3-Φ switched voltage. The CM emissions are comparable among the sequences, but sequence 8 generates significantly lower DM voltage-time area ripple. Thus, sequence 8 is the optimal modulation sequence when operating in area ①, achieving comparably low semiconductor losses and a low DM filtering effort, i.e., a facilitating a design with smaller DM inductors/filter components.

D. DM and CM RMS Voltage-Time Area Ripples

As introduced above, the HF DM and CM voltage-time area ripples are the relevant design parameters for the required DM and CM inductors (or filter components in general), which

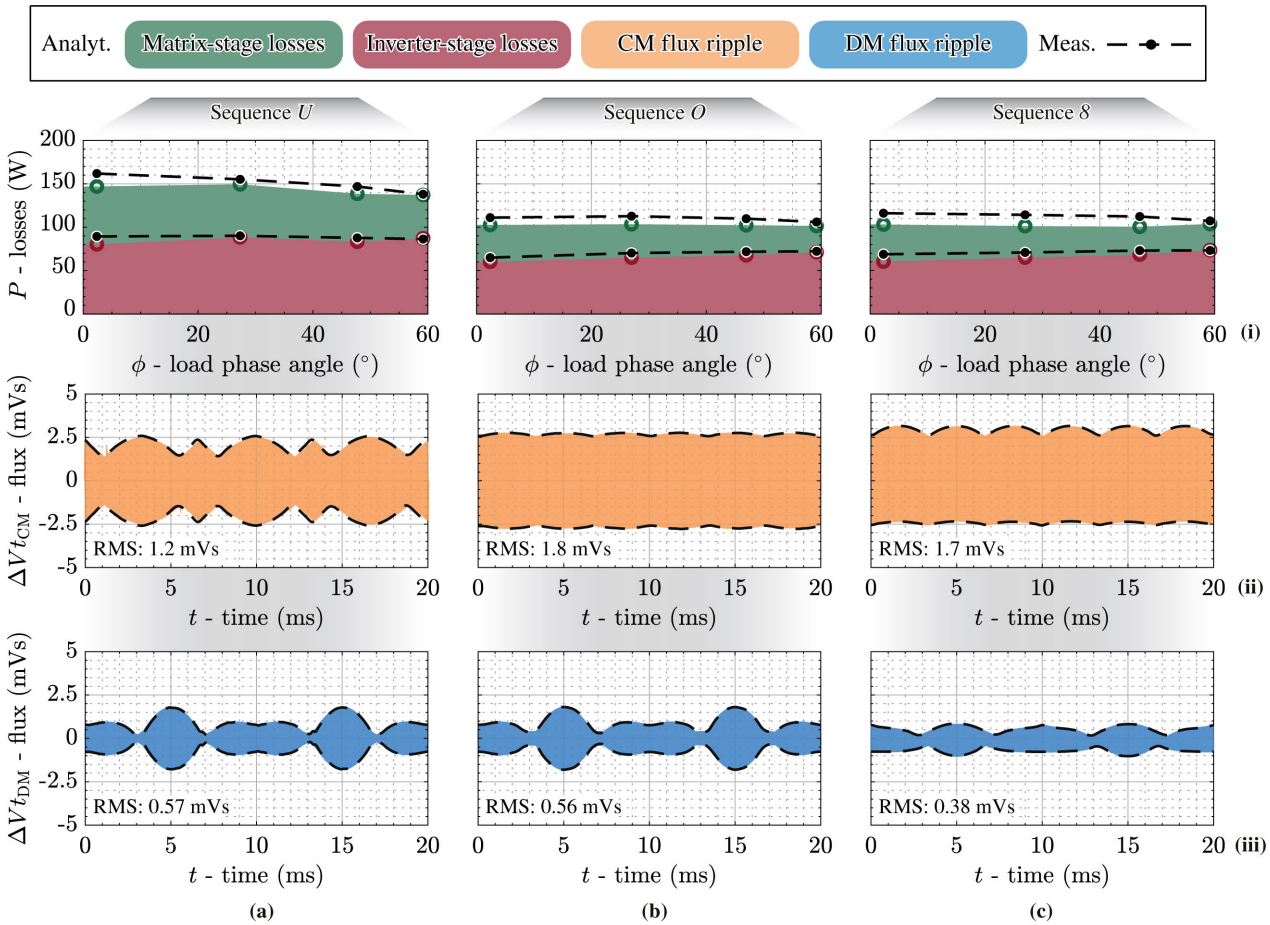

Fig. 11. Measurement results of 3-L SNPCC operation in area ① ($V_{dc} = 800$ V and $M = 0.5$) with different modulation schemes, i.e., (a) switching state sequence U, (b) sequence O, and (c) sequence 8. (i) Calculated and calorimetrically measured semiconductor losses are compared between the modulation sequences under constant apparent power $S = 4.4$ kVA ($\hat{V} = 200$ V and $\hat{I} = 14.7$ A) and varying load power factor, i.e., output current and voltage fundamental phase shift ϕ. Furthermore, (ii) shows the envelope of the HF CM voltage-time area ripple, and (iii) shows the envelope of the HF DM voltage-time area ripple waveforms for ohmic operation. The DM voltage-time area ripple of sequence 8 is significantly smaller compared with the other two sequences. In all cases, note the good agreement between analytic calculations (colored swatches) and measured results (black dashed lines).

TABLE IV

COMPARISON OF SEMICONDUCTOR LOSS MODELING APPROACHES FOR OPERATION IN AREA ① WITH THE ASYMMETRIC SEQUENCE O AND WITH DIFFERENT LOAD PHASE ANGLES ϕ: THE PROPOSED MODEL, P_{new} (SEE SECTION III-B), CLEARLY SHOWS MUCH HIGHER ACCURACY THAN THE CONVENTIONAL MODEL, $P_{conv.}$, FROM [26], WHICH IS FULLY ANALYTIC BUT, THUS, CANNOT ACCOUNT FOR HYBRID COMMUTATIONS. THE VALUES OF P_{meas} ARE THE CALORIMETRICALLY MEASURED SEMICONDUCTOR LOSSES, AND e DENOTES THE RELATIVE ERROR OF THE CALCULATIONS

ϕ (°)	P_{meas} (W)	$P_{conv.}$ (W)	e (%)	P_{new} (W)	e (%)
2.4	111.1	92.0	17.1	102.2	7.9
27.0	112.8	94.3	16.3	103.4	8.3
46.9	109.9	93.3	15.1	102.3	6.9
59.2	106.0	93.4	11.9	101.5	4.3

typically account for a large share of the overall converter volume in applications that require an output filter. Thus, Fig. 12 shows the rms DM and CM voltage-time area ripples

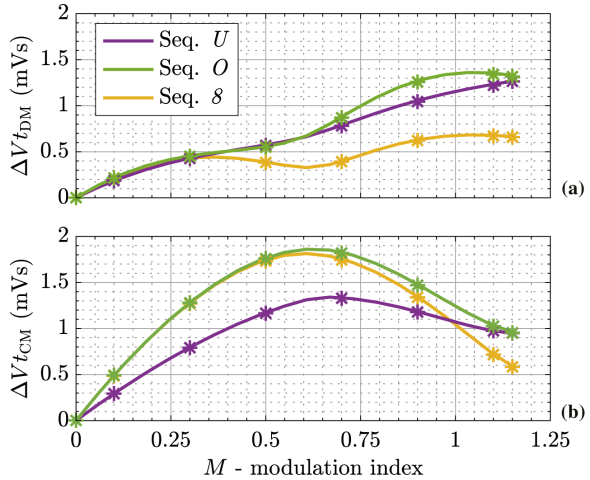

Fig. 12. Measured (asterisk marker) and analytically calculated [26] (solid line) rms values of (a) HF DM and (b) HF CM voltage-time area ripples for the considered modulation sequences U, O, and 8, as the functions of the modulation index M for ohmic operation (14.7-A peak phase current in phase with the output phase voltage) with a dc-link voltage of 800 V. A significant DM voltage-time area ripple reduction, i.e., approximately half at the nominal operating point compared to the other two sequences, is observed when applying sequence 8. Sequence U features the lowest CM voltage-time area ripples over a wide modulation index range.

obtained by the integral of the measured switched 3-Φ output voltages for the three considered modulation sequences as the functions of the modulation index. The experimental values match well with the analytical calculation results in [26]. It is observed that sequence *8* always achieves a significantly lower DM voltage-time area ripple than the other sequences, i.e., approximately half at the nominal operating point. Sequence *U* features low CM emissions over most of the modulation index range (but clearly the highest semiconductor losses). Due to the reduced number of switching instants in the semiconductor-loss-optimum sequence *O*, larger DM and CM filtering efforts have to be accepted.

VI. Conclusion

This article first summarizes the operating principle of the 3-Φ 3-L SNPCC and then provides a detailed analysis of a hybrid current commutation phenomenon that occurs for operation with low modulation indices, i.e., in area ① of the voltage space vector plane (see Fig. 2), thus leading to increased switching losses (up to 20%). The proposed loss modeling approach for IGBT-based systems can account for this effect and achieves high accuracy (<10% error). This is confirmed by a new in-situ calorimetric loss measurement approach implemented in a 800-V_{dc}, 7.5-kW 3-Φ 3-L SNPCC hardware demonstrator. This measurement approach is convenient (no need for additional test PCBs), fast (transient calorimetric measurement), and accurate (all parasitics included) and facilitates stage-level semiconductor loss measurements.

The hybrid current commutation effect introduces additional losses and leads to a lower-than-expected efficiency when operating in area ①, i.e., with low modulation indices. However, these additional losses could be minimized by using diodes with low reverse recovery charge in the inverter stage, e.g., power modules with antiparallel silicon-carbide (SiC) Schottky freewheeling diodes [53].

The further experimental characterization of the prototype considers both a wide range of modulation indices (area ① and ②) and phase shifts of load voltage and current fundamentals ϕ (0°–60°), as well as three typical symmetric and asymmetric modulation schemes, i.e., switching state sequences *U*, *O*, and *8*. The performance evaluations (semiconductor losses, DM and CM voltage-time area ripples) indicate that asymmetric modulation sequences are excellent candidates for effective 3-L SNPCC operation; i.e., sequence *O* generates clearly lowest semiconductor losses, especially under non-ohmic operating conditions, and sequence *8* requires minimum DM filtering effort. Finally, using a low-switching-loss asymmetric modulation sequence *O* (which is advantageously employed for applications that require a wide range of load phase angles ϕ, due to the lower semiconductor losses), the prototype achieves a semiconductor efficiency of 98.8% at nominal ohmic load with the effective switching frequencies of 16 kHz and 5.3 kHz.

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