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Non-Isolated Three-Phase Current DC-Link Buck-Boost EV Charger with Virtual Output Midpoint Grounding and Ground Current Control

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***Abstract*—Non-isolated three-phase AC/DC converter concepts facilitate more compact and more efficient realizations of future EV chargers. However, without the galvanic isolation and/or high common-mode (CM) impedance provided by an isolation transformer, non-isolated chargers must employ other means to suppress CM leakage currents to ground sufficiently and to prevent nuisance tripping of mandatory residual current devices (RCDs). Typically, the required EMI filters reduce high-frequency (HF) CM leakage currents to uncritical values. However, low-frequency CM voltages, e.g., generated by third-harmonic injection, may drive significant LF CM currents through the parasitic capacitances of the DC output (including the battery pack) to protective earth (PE). Therefore, considering a non-isolated three-phase buck-boost current DC-link PFC rectifier system that consists of a buck-type current-source rectifier (CSR) stage and a three-level boost-type DC/DC-stage, this paper first proposes a virtual grounding control (VGC) of the DC output voltage midpoint. VGC employs the DC/DC-stage to compensate the LF (third-harmonic) CM voltage inherently generated by the CSR-stage, and thus controls the LF CM voltage between the DC output midpoint and PE to zero. This enables further a direct connection of the DC output midpoint to PE, where an additionally proposed ground current control (GCC) ensures near-zero LF CM leakage current. The proposed concepts are verified with a 10 kW hardware demonstrator (power density of 6.4 kW/dm^3 or 107.5 W/in^3, full-load peak efficiency of 98.5%) considering TT (Terra-Terra) and TN (Terra-Neutral) grounding systems. With a direct connection of the DC output midpoint to PE, GCC limits the LF CM leakage current to < 6 mA RMS, i.e., significantly below typical RCD trip levels, and, using the human-body impedance model according to UL 2202, achieves a test voltage of 110 mV that is clearly below the most stringent limit (250 mV) of the standard.**

***Index Terms*—Non-Isolated EV Charger, Three-Phase Buck-Boost Current DC-Link PFC Rectifier, Two-Third Pulse-Width Modulation, Virtual Grounding Control, Ground Current Control, Synergetic Control.**

I. Introduction

Decarbonizing transportation is essential to meet climate goals and the world is moving full-force toward transportation electrification. Accordingly, the market penetration of electric vehicles (EVs) is steadily increasing: in 2021, almost 10% of all global car sales were EVs, which is a fourfold increase compared to 2019 [1]. More efficient and compact EV battery chargers are key enablers for a further acceleration of this transition to electric mobility. Even though relevant standards for EV chargers, e.g., UL 2202 [2] or IEC 61851 [3], do not require galvanic isolation between the grid-connected input and the output charging ports (IEC 61851-23 [4], for example, mentions that regulations for non-isolated DC chargers are under consideration), conventional EV chargers typically include either traditional 50 Hz transformers or DC/DC converters with high-frequency (HF) isolation to provide a large common-mode (CM) impedance between the grid and the vehicle to ensure electrical safety [5]–[7]. However, providing galvanic isolation means placing an additional conversion stage, i.e., a low-frequency transformer or an isolated DC/DC converter, in the power flow path and consequently leads to more bulky and more complex systems with increased power losses and costs. To roughly quantify these drawbacks, consider photovoltaic (PV) inverter systems: compared to traditional solutions that include galvanic isolation, their transformerless counterparts feature an efficiency improvement of 1 % to 2 % and about twice the power density [8], [9]. Thus, extensive research has been carried out on non-isolated EV chargers over the recent years [6], [10]–[19].

However, without galvanic isolation, reliable protection against electrical hazards can only be provided by residual current devices (RCDs), or so-called ground fault circuit interrupters (GFCIs), installed at the grid interface, which is thus mandatory according to standards (e.g., IEC 61851, UL 2202) [6]. In three-phase (3-Φ) systems, RCDs measure the sum of the three individual phase currents to detect any deviation from zero, which corresponds to a CM ground current (that potentially could be flowing through a human body touching a live part during a fault situation) and quickly disconnect the converter from the grid if certain trip levels (typ. 30 mA AC and 6 mA DC, see IEC 61851-1 [3]) are reached. **Fig. 1.a** shows a conceptual block diagram of a typical 3-Φ non-isolated EV charger. Note that a connected battery pack, due to its physically large dimensions, often contributes significantly to the total parasitic CM capacitance between the DC output terminals and the vehicle chassis (and thus to protective earth (PE), as safety standards require a grounded chassis).

To achieve compatibility with the wide range of EV battery voltages (200 V to 800 V, see **Fig. 2**), non-isolated EV

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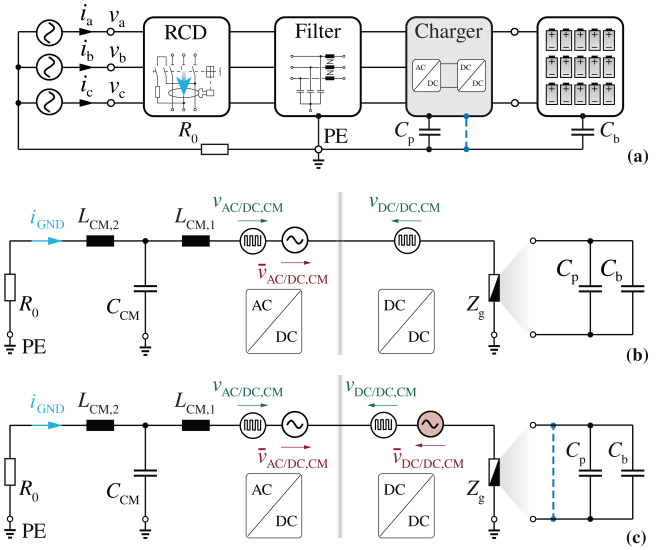

Fig. 1: **(a)** Block diagram of a typical non-isolated three-phase (3-Φ) two-stage AC/DC EV charger, and **(b)** its common-mode (CM) equivalent circuit for conventional operation. High-frequency (HF) CM voltage components are limited by the EMI filter. Low-frequency (LF) CM components generated by the AC/DC rectifier stage (e.g., by third-harmonic injection) appear at the DC output terminals, i.e., across the parasitic capacitance of the DC output to earth, potentially driving leakage currents that could lead to nuisance tripping of the mandatory RCD. Note that both, the converter (C_p) and the connected battery pack (C_b) contribute to the total parasitic capacitance. **(c)** As proposed in this paper, the DC/DC-stage can inject a compensating LF CM voltage, which allows virtual grounding control (VGC), i.e., regulating the LF CM voltage to zero. Similarly, a proposed ground current control (GCC) can be employed to regulate the LF CM leakage current to zero and hence facilitates even a direct connection (blue dashed line) of the output midpoint to ground.

chargers must provide buck-boost functionality and are thus usually realized as two-stage systems that consist of an AC/DC boost-type voltage DC-link PFC rectifier and a buck-type DC/DC converter. As indicated in the CM equivalent circuit of **Fig. 1.b**, both the AC/DC-stage and the DC/DC-stage generate HF CM voltages ($v_\mathrm{AC/DC,CM}$ and $v_\mathrm{DC/DC,CM}$, respectively) due to PWM operation, and the AC/DC-stage may, in addition, generate a low-frequency (LF) CM voltage $\bar{v}_\mathrm{AC/DC,CM}$ if using third-harmonic injection to improve the DC-link voltage utilization. The total CM voltage could drive significant leakage currents through the parasitic capacitors into the protective earth (PE) conductor, where C_p from the power converter and C_b from the battery pack together form the DC-side grounding impedance Z_g. Without countermeasures, such leakage ground currents can easily reach the RCD trip level and thus lead to nuisance tripping [6], [14].

However, as EV chargers are connected to the public mains, EMI standards such as CISPR 11 must be met. Thus, passive differential-mode (DM) and especially also CM filters must be employed, as also (conceptually) indicated in **Fig. 1.b**, which attenuate the HF CM voltages to levels that do not cause significant HF CM leakage currents.[1] Thus, most non-isolated EV chargers discussed in the literature employ corresponding

[1]With respect to **Fig. 1.b**, the HF CM voltages appear across the CM EMI filter inductors, i.e., in this example across $L_\mathrm{CM,1}$ and $L_\mathrm{CM,2}$ as, at HF, their impedances are significantly larger than those of the capacitive elements in the equivalent circuit; i.e., only residual HF voltage fluctuations appear at the DC output terminals and across Z_g.

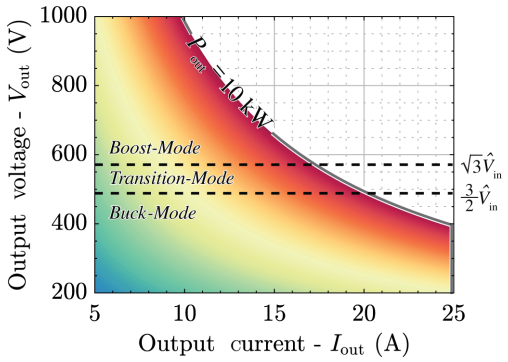

Fig. 2: Typical operating range of EV chargers, including a constant output current $I_\mathrm{out} = 25\,\mathrm{A}$ region when $V_\mathrm{out} < 400\,\mathrm{V}$ and a constant output power $P_\mathrm{out} = 10\,\mathrm{kW}$ when $V_\mathrm{out} > 400\,\mathrm{V}$. Three operating modes, i.e., buck-mode, boost-mode and transition-mode, are required to cover such a wide output voltage range [20].

CM EMI filters, whereby often integrated (or so-called floating filter concepts, i.e., essentially DC-link-referenced first (innermost) CM filter stages [21]–[24], are used, e.g., in [6], [13], [16], [17], [19]. Other approaches target a reduction of the HF CM noise sources by special modulation techniques [18] or CM-free system configurations [15], which, however, rely on the availability of a neutral conductor (three-phase, four-wire systems).

In voltage DC-link boost-type rectifier systems, the generation of an LF CM voltage can be avoided if no third-harmonic injection is used, i.e., by accepting a limitation of the modulation index of $M \leq 1$ compared to $M \leq 1.15$ otherwise, where $M = \hat{V}_\mathrm{in}/(V_\mathrm{DC}/2)$ considering that $\hat{V}_\mathrm{in}$ is the AC phase voltage amplitude and V_DC is the DC-link voltage. Furthermore, to ensure a constant LF CM voltage and hence suppress any LF CM leakage currents, the rectifier stage can actively control the LF CM voltage, as, e.g., suggested for converters interfacing the AC mains and DC microgrids [25] or specifically for non-isolated EV chargers in [16], [17], [19]. Finally, a three-phase voltage DC-link rectifier/inverter can be extended by a fourth bridge-leg, which is then modulated to compensate the LF and HF CM noise emissions generated by the other three bridge-legs. This concept has been proposed for two-level [26] and three-level (3-L) [27] voltage DC-link topologies, but without considering closed-loop control of the ground leakage current.

As demonstrated in [28] for back-to-back 3-Φ T-type rectifier and inverter systems, the rectifier stage can also control the LF CM leakage *current*, provided the system is equipped with a dedicated and highly accurate current sensor measuring the sum of the 3-Φ input currents in the same way an RCD does. Finally, considering two-stage interfaces (i.e., an AC/DC rectifier connected to a DC/DC converter) between a split-phase AC system and a DC microgrid, [29] employs the DC/DC-stage to control the LF CM voltage (see **Fig. 1.c**), whereas [30] also relies on the DC/DC converter to reduce the LF CM voltage, but only with a feed-forward approach instead of closed-loop control.

In contrast to the aforementioned combination of a voltage DC-link boost-type PFC rectifier and buck-type DC/DC-stage, this paper focuses on a non-isolated EV charger implemented

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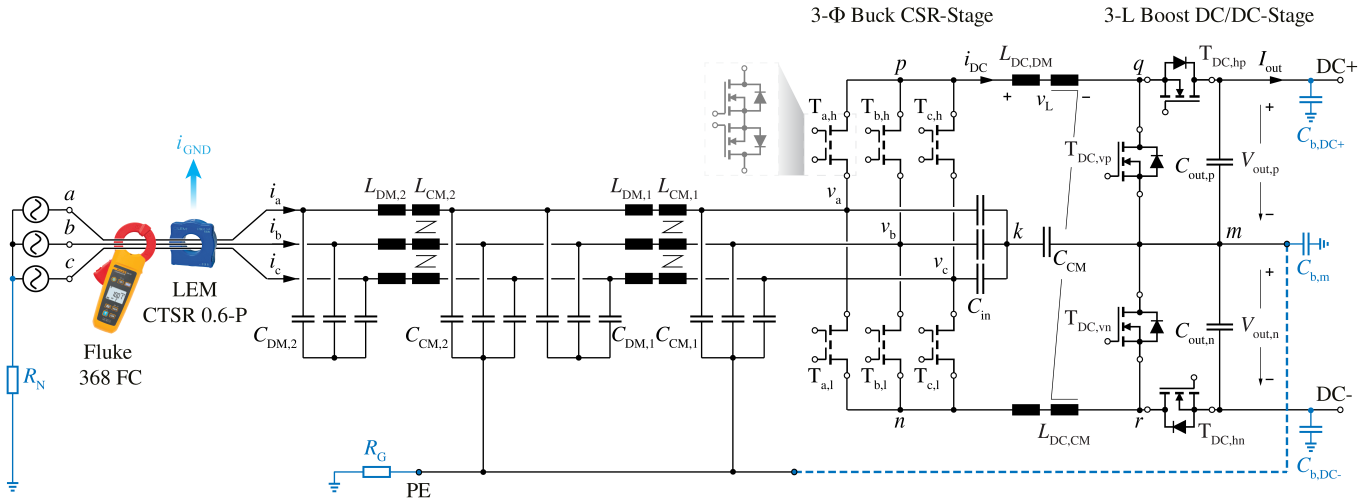

Fig. 3: Power circuit of the considered 10 kW three-phase (3-Φ) two-stage current DC-link PFC rectifier system (see **Fig. 2** for an overview on the operating range and **Tab. I** for detailed specifications) including a CM/DM EMI filter, which employs an integrated first-stage CM filter [22]–[24], [31] to limit the DC output HF CM voltage by connecting the artificial 3-Φ neutral point k and the DC voltage midpoint m with a CM filter capacitor C_{CM}. The proposed virtual grounding control (VGC, see **Section II-B**) uses the DC/DC-stage to inject a LF CM voltage and thus regulate the LF voltage across C_{CM} to zero. Alternatively, the proposed ground current control (GCC, see **Section II-C**) enables a low-impedance connection of the output midpoint m to the PE conductor (dashed blue line) with the LF ground current $i_{\mathrm{GND}} = i_{\mathrm{a}} + i_{\mathrm{b}} + i_{\mathrm{c}}$ regulated to values $< 30\,\mathrm{mA}$, as verified with a leakage current clamp meter *Fluke 368 FC* [39] (see **Section IV**). Note that the experimental verification considers two different grid grounding schemes (details see **Section IV-B1**), i.e., TT (Terra-Terra) with $R_{\mathrm{N}} = 10\,\Omega$ and $R_{\mathrm{G}} = 100\,\Omega$ and TN (Terra-Neutral) with $R_{\mathrm{N}} = R_{\mathrm{G}} = 0\,\Omega$ [6].

with a 3-Φ bidirectional buck-boost (bB) *current DC-link* PFC rectifier system (see **Fig. 3**), which is formed by a 3-Φ buck-type current-source-rectifier (CSR) stage and a subsequent boost-type DC/DC-stage [20], [31]. Compared to a conventional voltage DC-link PFC rectifier approach, the current DC-link system has several advantages, e.g., a reduced number of main magnetic components (only one DC-link inductor instead of three AC-side boost inductors; the DC-link inductor is shared between the CSR-stage and the DC/DC-stage), which facilitates low manufacturing costs and higher volumetric power density. Note that the main structural weakness of CSRs, i.e., the need for switches that feature bipolar voltage blocking capability, is being eliminated by the recent availability of monolithic bidirectional power transistors [32]–[34]. Advantageously, synergetic control [32], [35], [36] of the two-stage system shown in **Fig. 3** achieves minimum-loss operation: in the boost-mode ($V_{\mathrm{out}} \geq \sqrt{3}\hat{V}_{\mathrm{in}}$, where $\hat{V}_{\mathrm{in}}$ is the AC phase voltage amplitude and V_{out} is the DC output voltage, see **Fig. 2**), the DC/DC-stage shapes the DC-link current such that the CSR-stage can operate with 2/3-PWM [37], [38], i.e., with cyclically changing temporary clamping of a phase (only two and not all three phases are generating switching losses), and in the buck-mode ($V_{\mathrm{out}} \leq 3/2 \cdot \hat{V}_{\mathrm{in}}$) the CSR-stage operates with conventional 3/3-PWM to control the output voltage but the DC/DC-stage is clamped without switching; a more detailed description of the operating principle is given below.

Transformerless operation of such a 3-Φ bB current DC-link EV charger has not been investigated and the feasibility of complying with the relevant standards such as UL 2202 [2] or IEC 61851 [3] has not been demonstrated. Different from voltage DC-link rectifier systems, typical modulation schemes for the CSR-stage always result in an LF CM voltage component $\bar{v}_{\mathrm{AC/DC,CM}}$. However, the employed 3-L DC/DC converter stage advantageously also can generate an LF CM voltage, which in principle opens the possibility of compensating the LF CM voltage of the AC/DC rectifier stage by selecting $\bar{v}_{\mathrm{DC/DC,CM}} = \bar{v}_{\mathrm{AC/DC,CM}}$, see **Fig. 1.c**.

Therefore, this paper first provides a comprehensive analysis of a new virtual grounding control (VGC) method, i.e., a feedback control of the LF CM voltage that ensures zero voltage (i.e., a virtual connection) between the artificial neutral point k formed by the AC-side input filter capacitors and the midpoint m of the DC-side output (see **Fig. 3**). Thus, the proposed VGC effectively minimizes the parasitic ground current flowing through $C_{\mathrm{b,m}}$. By further selecting sufficiently large output capacitances $C_{\mathrm{out,p}}$ and $C_{\mathrm{out,n}}$, also the amplitudes of the LF CM voltages at the terminals DC+ and DC- with reference to PE are decreased, which ultimately leads to greatly reduced ground leakage currents through $C_{\mathrm{b,DC+}}$ and $C_{\mathrm{b,DC-}}$.

Furthermore, closed-loop ground current control (GCC) is proposed to allow a direct connection of the output DC-bus midpoint m to the system PE connector (see also the blue dashed line in **Fig. 1.c** and **Fig. 3**) by controlling the ground current $i_{\mathrm{GND}} = i_{\mathrm{a}} + i_{\mathrm{b}} + i_{\mathrm{c}}$ (i.e., the leakage current measured and limited by RCDs) of the analyzed current DC-link system to near-zero. GCC prevents nuisance tripping of mandatory RCDs and is hence considered an enabling concept for future transformerless EV chargers. Importantly, such a direct connection also removes the impact of any parasitic ground capacitance, e.g., $C_{\mathrm{b,DC+}}$ or $C_{\mathrm{b,DC-}}$, that might vary between different battery packs. These parasitic ground capacitors are then directly in parallel with the relatively large output capacitors $C_{\mathrm{out,p}}$ and $C_{\mathrm{out,n}}$.

In the following, **Section II** first derives the CM equivalent circuit of the analyzed 3-Φ bB current DC-link PFC rectifier system and explains the operating principle of the

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TABLE I: System Specifications.

	Description	Value
V_{in}	Phase RMS volt.	230 V
V_{out}	DC output volt. range	300 V∼1000 V
P_{out}	Rated output power	10 kW
$I_{out,max}$	Output current limit	25 A ($V_{out} < 400$ V)
f_{CSR}	CSR-stage sw. freq.	100 kHz
$f_{DC/DC}$	DC/DC-stage sw. freq.	100 kHz
$L_{DC,DM}$	DC-link DM inductor	250 µH
$L_{DC,CM}$	DC-link CM inductor	14 mH
C_{in}	Input filter capacitor	3×6 µF
$C_{out,p} = C_{out,n}$	Output filter capacitor	2×11.2 µF
C_{CM}	Integrated CM filter cap.	88 nF
$L_{DM,1} = L_{DM,2}$	EMI DM inductor	10 µH
$C_{DM,1} = C_{DM,2}$	EMI DM capacitor	3 µF
$L_{CM,1} = L_{CM,2}$	EMI CM inductor	1.2 mH
$C_{CM,1} = C_{CM,2}$	EMI CM capacitor	18.8 nF

proposed VGC and GCC concepts. **Section III** then presents the corresponding control structure that realizes the synergetic operation of the two converter stages and implements VGC or GCC. Finally, **Section IV** provides experimental results of a 10 kW hardware demonstrator that verify the proposed VGC. Using a direct grounding of the DC output midpoint and the proposed GCC, we further demonstrate total leakage currents of well below the typical RCD trip level of 30 mA for TT (Terra-Terra) and TN (Terra-Neutral) grid grounding schemes (these are explained in detail in Section IV-B1), and (for TN systems) an output voltage of the human-body impedance model according to UL 2202 of clearly less than the limit of 250 mV, i.e., full compliance with applicable standards over a wide output voltage and power range.

II. Operating Principle

The considered bidirectional two-stage 3-Φ bB current DC-link PFC rectifier system shown in **Fig. 3** connects the 3-Φ AC mains to a DC load through a buck-type current-source rectifier (CSR) stage and a cascaded boost-type 3-L DC/DC output stage, which advantageously share the main magnetic components, i.e., the DC-link inductor L_{DC} and the integrated CM filter inductor $L_{DC,CM}$ [20], [31]. In conventional rectifier operation, the buck-type CSR-stage first steps down the 3-Φ AC mains voltages (v_a, v_b, v_c) to a lower DC voltage v_{pn} using PWM; or, considering the more illustrative reverse current conversion, the 3-Φ mains currents (i_a, i_b, i_c) are generated by pulse-width-modulated distribution of the constant DC-link current to the three phases. As long as the output voltage is below the maximum DC-side voltage that the CSR-stage can generate ($V_{out} < 3/2\hat{V}_{in}$, buck-mode), the DC/DC-stage is not needed and can be clamped, i.e., $T_{DC,hp}$ and $T_{DC,hn}$ are permanently on. If the output voltage is higher ($V_{out} > \sqrt{3}\hat{V}_{in}$, boost-mode), the boost-type DC/DC-stage must be operated to step up v_{pn} to the higher output voltage accordingly. Note that the artificial 3-Φ neutral point k formed by the CSR-stage's DM input filter capacitors C_{in} and the DC output voltage midpoint m are connected through a CM filter capacitor C_{CM}, i.e., C_{CM} and $L_{DC,CM}$ form an integrated CM filter [22]–[24], [31].

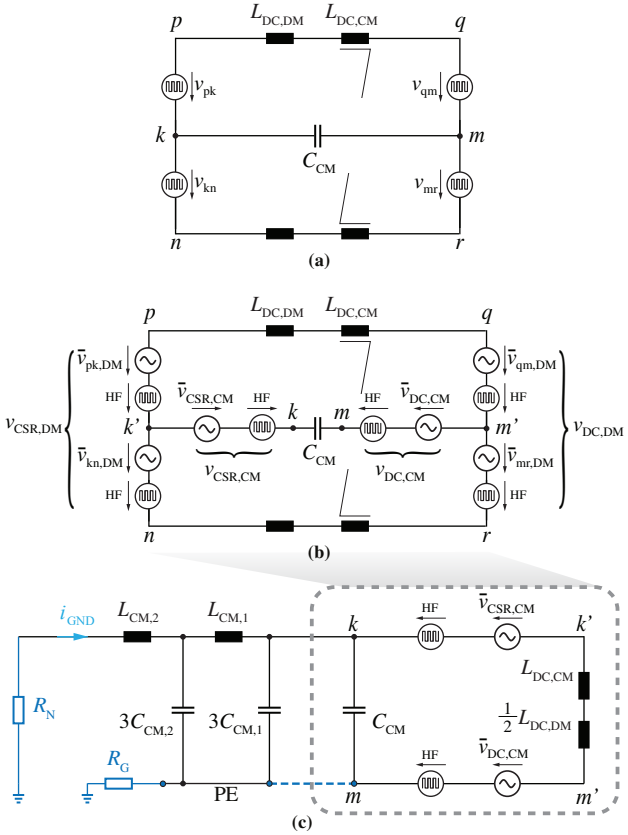

Fig. 4: Derivation of the CM equivalent circuit of the 3-Φ bB current DC-link PFC rectifier system from **Fig. 3**. Neglecting the EMI filter in a first step, **(a)** shows the main power converter consisting of the CSR-stage and the DC/DC-stage which are replaced by switched voltage sources. **(b)** These switched voltage sources are decomposed to present DM and CM as well as HF and LF components explicitly. **(c)** The final CM equivalent circuit is obtained from **(b)** by retaining only the LF and HF CM voltage sources and adding the CM EMI filter as well as the grounding scheme of the grid. Note that an LF CM voltage $\bar{v}_{DC,CM}$ generated by the DC/DC-stage can compensate the LF CM voltage $\bar{v}_{CSR,CM}$ inevitably generated by the CSR-stage. This enables the proposed VGC (where the DC output is not explicitly grounded) or the novel GCC (where the DC output is hard grounded as indicated by the dashed blue line and the ground current i_{GND} is controlled to zero in closed loop).

In this section, first, a CM equivalent circuit of the converter shown in **Fig. 3** is developed to then facilitate clear explanations of the proposed virtual grounding control (VGC) and ground current control (GCC) concepts, considering both, boost-mode and buck-mode operation.

A. CM Equivalent Circuit

Neglecting the grid-side EMI filter in the first step, the analyzed converter can be represented by the equivalent circuit shown in **Fig. 4.a**, where the CSR-stage's upper and lower switching cells are replaced by the voltage sources v_{pk} and v_{kn}, respectively, and the DC/DC-stage's upper and lower half-bridges (HBs) by v_{qm} and v_{mr}. These voltage sources contain HF components (i.e., switching frequency and its harmonics) and LF components (i.e., at frequencies significantly below the switching frequency, such as DC or low-order harmonics of the grid frequency). It is then useful to separate the voltages

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generated by both stages into DM and CM components, which yields the equivalent circuit shown in **Fig. 4.b**, whereby

$$v_{\mathrm{CSR,CM}} = \frac{v_{\mathrm{pk}} - v_{\mathrm{kn}}}{2}, \qquad v_{\mathrm{DC,CM}} = \frac{v_{\mathrm{qm}} - v_{\mathrm{mr}}}{2}, \quad (1)$$

$$v_{\mathrm{CSR,DM}} = v_{\mathrm{pk}} + v_{\mathrm{kn}}, \qquad v_{\mathrm{DC,DM}} = v_{\mathrm{qm}} + v_{\mathrm{mr}}. \quad (2)$$

The final CM equivalent circuit (see **Fig. 4.c**) includes the two-stage CM EMI filter and the impedances modeling the considered grid grounding schemes (TT and TN). Note the similarity to the conceptual drawing discussed earlier (see **Fig. 1.c**), i.e., HF CM components are suppressed by a passive multi-stage EMI filter, which in particular features an integrated CM filter formed by C_{CM} and $L_{\mathrm{DC,CM}}$.

Therefore, focusing on the LF components, $\bar{v}_{\mathrm{CSR,DM}} = \bar{v}_{\mathrm{DC,DM}}$ must always be attained in steady-state operation if neglecting the minor LF voltage difference needed to shape the DC-link current into the six-pulse shape in boost-mode operation with 2/3-PWM. Considering the state-of-the-art synergetic operation, the two output DC voltages are balanced ($V_{\mathrm{out,p}} = V_{\mathrm{out,n}}$) [35] and thus the two half-bridges of the DC/DC-stage are modulated with equal duty cycles so that $\bar{v}_{\mathrm{qm}} = \bar{v}_{\mathrm{mr}}$ and, hence, zero LF CM injection ($\bar{v}_{\mathrm{DC,CM}} = 0$) results. In contrast, typical CSR modulation schemes do not achieve $\bar{v}_{\mathrm{pk}} = \bar{v}_{\mathrm{kn}}$ [31], and hence we have $v_{\mathrm{CSR,CM}} \neq 0$. As a result, an LF CM voltage $\bar{v}_{\mathrm{mk}} = \bar{v}_{\mathrm{CSR,CM}} - \bar{v}_{\mathrm{DC,CM}} \neq 0$ appears across the integrated CM filter capacitor C_{CM}, i.e., between the DC output midpoint, m, and the (artificial) grid star point k.

As can be seen in **Fig. 4.c**, $\bar{v}_{\mathrm{mk}}$ is approximately equal to $\bar{v}_{\mathrm{mPE}}$ considering a symmetric 3-Φ mains. Thus, this LF CM voltage prevents a direct low-impedance connection of m and PE, as then significant LF CM leakage currents would flow, i.e., $L_{\mathrm{CM,1}}$ and $L_{\mathrm{CM,2}}$ can only provide limited LF impedance. In the case of TN grounding systems with nonzero R_{G}, significant touch voltages (i.e., voltages between the local PE and true earth) could appear. On the other hand, **Fig. 4.c** also clearly shows that, in principle, the DC/DC-stage can inject an LF CM voltage $\bar{v}_{\mathrm{DC,CM}} = \bar{v}_{\mathrm{CSR,CM}}$ such that $\bar{v}_{\mathrm{mk}} = 0$, which is possible without interfering with the LF DM voltage regulation. This (virtually) ties m to PE (i.e., $\bar{v}_{\mathrm{mPE}} = 0$) and thus facilitates a direct connection of these two points, i.e., hard grounding of the DC output midpoint m. Furthermore, $\bar{v}_{\mathrm{mk}} = 0$, ideally, leads to zero LF CM current flowing through the CM inductor $L_{\mathrm{DC,CM}}$ of the integrated filter, which allows a more compact CM inductor realization because of reduced saturation margin and/or a larger CM capacitance C_{CM} and, for a given attenuation requirement, thus a lower $L_{\mathrm{DC,CM}}$ can be selected.

B. Virtual Grounding Control (VGC)

The analyzed converter operated with synergetic control provides buck-boost functionality and thus features two main operating modes, i.e., boost-mode ($V_{\mathrm{out}} > \sqrt{3}\hat{V}_{\mathrm{in}}$) and buck-mode ($V_{\mathrm{out}} < {}^{3}\!/_{2}\hat{V}_{\mathrm{in}}$), as described in [35]. In the following, the generic analysis from above will be explained in detail for each of these two operating modes.

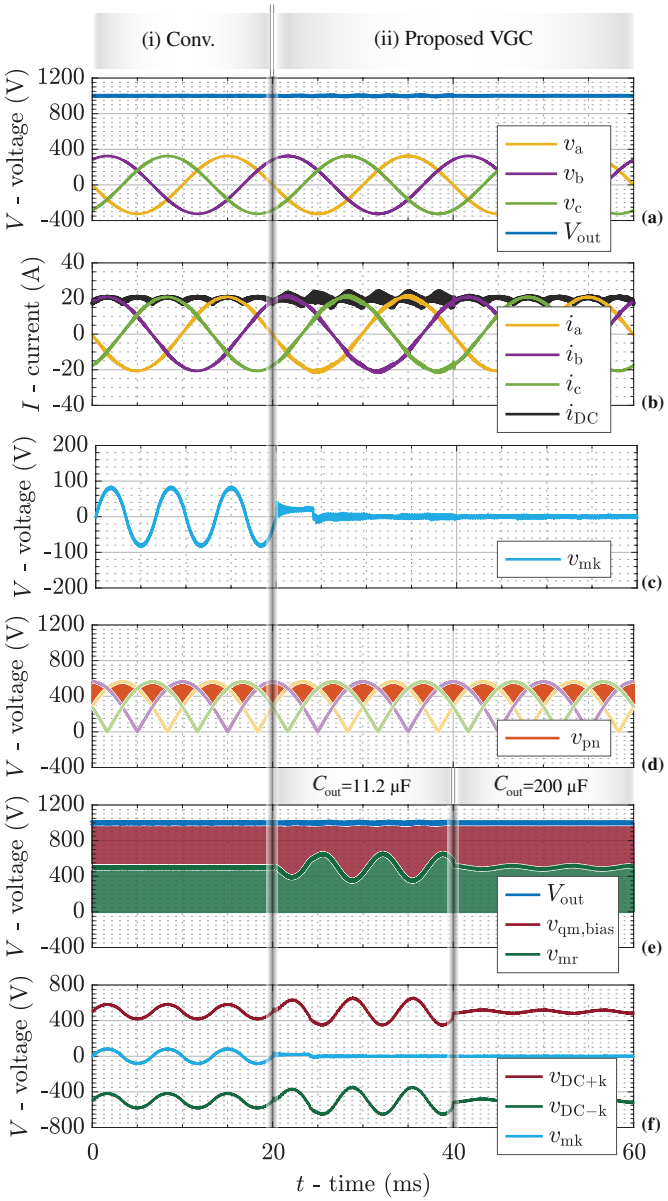

Fig. 5: Simulated key waveforms for operation in the boost-mode, **(i)** regulated by conventional synergetic control without VGC and **(ii)** with the proposed VGC. **(a)** 3-Φ mains voltages v_{a}, v_{b}, v_{c} and DC output voltage V_{out}. **(b)** 3-Φ mains currents i_{a}, i_{b}, i_{c} and DC-link current i_{DC}. Note that the peak-to-peak ripple of the DC-link current i_{DC}, increases from 2 A to 6 A when activating the proposed VGC because of the then time-varying output capacitor voltages and the therefore modified duty cycles of the DC/DC-stage; the DC-link current ripple reduces again if larger output DC capacitors are used. **(c)** CM voltage v_{mk}. **(d)** Switched voltage v_{pn} at the output of the CSR-stage; note that 2/3-PWM does not employ the zero (shoot-through) switching state of the CSR-stage (v_{pn} never attains 0 V). **(e)** Switched voltages $v_{\mathrm{qm,bias}} = v_{\mathrm{qm}} + V_{\mathrm{out,n}}$ and v_{mr} at the input of the DC/DC-stage's upper and lower HBs; note that the lower envelope of $v_{\mathrm{qm,bias}}$ and the upper envelope of v_{mr} indicate the output capacitor voltages $V_{\mathrm{out,p}}$ and $V_{\mathrm{out,n}}$, which vary with 150 Hz individually if VGC is active, while the sum of both, i.e., the output voltage V_{out}, remains constant. **(f)** LF CM voltages $v_{\mathrm{DC+k}}$, $v_{\mathrm{DC-k}}$, v_{mk} at the DC output terminals, which could drive ground leakage currents through the parasitic capacitors $C_{\mathrm{b,DC+}}$, $C_{\mathrm{b,DC-}}$, and $C_{\mathrm{b,m}}$ (see **Fig. 3**).

1) Boost-Mode

In boost-mode operation (see **Fig. 5.i**), the CSR-stage operates with 2/3-PWM where no zero switching states are employed (v_{pn} never attains 0 V in **Fig. 5.d**), i.e., one phase is

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always clamped, which advantageously reduces the switching losses. To still ensure sinusoidal 3-Φ mains currents, the DC/DC-stage is required to regulate the DC-link current to follow the six-pulse shape defined by the envelope of the phase current absolute values, as needed for 2/3-PWM (see **Fig. 5.b**). As mentioned above, the CSR-stage inevitably generates an LF CM voltage $\bar{v}_{\text{CSR,CM}}$, which is independent of the output voltage since the CSR-stage operates identically over the boost-mode operating range [31]. Different from the CSR-stage, only HF CM noise (no LF CM voltage) is generated by the DC/DC-stage in case of conventional synergetic control [31], since typically the two output capacitor voltages, i.e., $V_{\text{out,p}}$ and $V_{\text{out,n}}$, are equal and the DC/DC-stage's upper and lower HBs operate with the same duty cycles. Thus, the LF CM capacitor voltage becomes $\bar{v}_{\text{mk}} = \bar{v}_{\text{CSR,CM}}$ and contains major LF components (see **Fig. 5.i.c**). Note that therefore also the voltages between each of the three output nodes (m, DC+ and DC-) and PE (same potential as the node k) contain significant LF components (see **Fig. 5.i.f**) that might drive comparably high LF CM currents through the corresponding parasitic ground capacitors; note that especially $C_{\text{b,DC+}}$ and $C_{\text{b,DC-}}$ are dominated by the connected battery pack and can be as high as several µF [15], [40].

To suppress the LF CM voltage $\bar{v}_{\text{mk}}$, the virtual grounding control (VGC) is proposed, where the DC/DC-stage is modulated to actively compensate the LF CM voltage generated by the CSR-stage such that $\bar{v}_{\text{mk}} \approx 0\,\text{V}$, i.e., the potentials m and k are virtually connected. Only a minor (and hence here neglected) LF DM voltage component is needed to obtain the six-pulse shape of the DC-link current, resulting in the DM requirement $\bar{v}_{\text{CSR,DM}} = \bar{v}_{\text{DC,DM}}$. To enable the proposed VGC, the CM requirement $\bar{v}_{\text{CSR,CM}} = \bar{v}_{\text{DC,CM}}$ directly leads to the conditions $\bar{v}_{\text{qm}} = \bar{v}_{\text{pk}}$ and $\bar{v}_{\text{mr}} = \bar{v}_{\text{kn}}$, see also **Fig. 4.a**. Then, the local average power balance at the input (i.e., DC-link side) and the output of the upper DC/DC-stage HB can be written as

$$\bar{v}_{\text{pk}} \cdot \bar{i}_{\text{DC}} = V_{\text{out,p}} \cdot (I_{\text{out}} + C_{\text{out,p}} \cdot \dot{V}_{\text{out,p}}), \tag{3}$$

where $\bar{i}_{\text{DC}}$ is the local average value of the DC-link current. Assuming a constant output current I_{out}, $V_{\text{out,p}}$ must show a time-varying behavior defined by the time-varying power flowing through the CSR-stage's upper commutation cell, which mainly consists of a 150 Hz (i.e., third harmonic of the grid frequency) variation when using 2/3-PWM. Likewise, the power balance for the lower commutation cell is obtained as

$$\bar{v}_{\text{kn}} \cdot \bar{i}_{\text{DC}} = V_{\text{out,n}} \cdot (I_{\text{out}} + C_{\text{out,n}} \cdot \dot{V}_{\text{out,n}}). \tag{4}$$

Neglecting the capacitive current flowing through the output capacitors, the sum of the two equations leads to

$$(\bar{v}_{\text{pk}} + \bar{v}_{\text{kn}}) \cdot \bar{i}_{\text{DC}} = \bar{v}_{\text{CSR,DM}} \cdot \bar{i}_{\text{DC}} = (V_{\text{out,p}} + V_{\text{out,n}}) \cdot I_{\text{out}}, \tag{5}$$

where the left-hand side describes the constant input power delivered by a symmetric 3-Φ system. Thus, since the load current I_{out} is constant, operation with VGC still ensures a constant total output voltage $V_{\text{out}} = V_{\text{out,p}} + V_{\text{out,n}}$. On the other hand, as the VGC circuit simulation results from **Fig. 5.ii** show, the individual output capacitor voltages $V_{\text{out,p}}$ and $V_{\text{out,n}}$ vary complementarily at 150 Hz (see **Fig. 5.ii.e**). Note further that the CM voltage becomes $\bar{v}_{\text{mk}} \approx 0\,\text{V}$ while the CSR-stage still advantageously operates with 2/3-PWM (see **Fig. 5.ii.c** and **Fig. 5.ii.d**).

In this context, note that the overall LF CM voltage generated by the DC/DC-stage has two contributions: A CM component added to the duty cycles of the upper and the lower HBs, and the difference between the two output capacitor voltages $V_{\text{out,p}}$ and $V_{\text{out,n}}$ contribute to the CM voltage before modulation of the two HBs. In other words, if a large voltage variation is accepted, correspondingly smaller CM duty cycle components are needed to realize a given $\bar{v}_{\text{DC,CM}}$, which will be an important consideration for buck-mode operation (see **Section II-B2**).

The proposed VGC regulates the output midpoint to potential k (equivalent to PE), which almost completely suppresses parasitic LF ground currents flowing through $C_{\text{b,m}}$. However, as can be seen in **Fig. 5.ii.f**, the LF voltage fluctuations of the output capacitor voltages still result in LF CM voltages $v_{\text{DC+k}}$ and $v_{\text{DC-k}}$ across the parasitic capacitors $C_{\text{b,DC+}}$ and $C_{\text{b,DC-}}$ at the terminals DC+ and DC- (see **Fig. 3**). However, the two output capacitances $C_{\text{out,p}}$ and $C_{\text{out,n}}$ are a degree of freedom to lower the amplitudes of these LF CM voltages as needed to limit the ground leakage currents through $C_{\text{b,DC+}}$ and $C_{\text{b,DC-}}$. Note that the ground current control (GCC) proposed below mitigates these leakage currents without the need for larger output capacitances, as it allows and/or actively introduces a variation of the DC output midpoint CM voltage v_{mk} such that the total ground current is controlled to zero.

The output capacitor voltage variation also affects (increases) the maximum blocking voltage of the DC/DC-stage's power transistors. It is therefore important to calculate the maximum voltage ripple ΔV_{pp} of each of the two output capacitors. The output capacitor voltages mainly consist of a DC component of $^1/_2 V_{\text{out}}$ and an LF (150 Hz) variation. Neglecting other (minor) LF harmonics, this LF voltage variation can be accurately calculated from (3), resulting in a closed-form

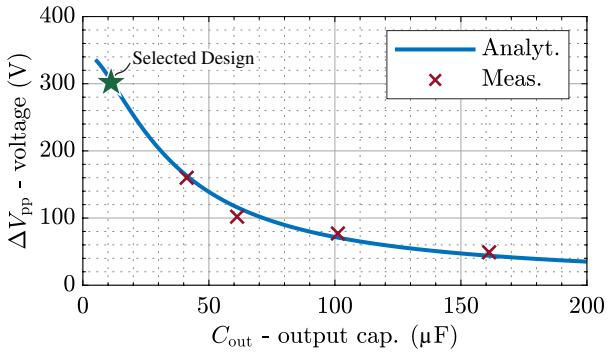

Fig. 6: Peak-to-peak variation ΔV_{pp} of the voltages of the two output capacitors $C_{\text{out,p}}$ and $C_{\text{out,n}}$ (see **Fig. 3**) under the proposed VGC as a function of the DC output capacitance C_{out} when operating at $V_{\text{out}} = 1000\,\text{V}$ and $P_{\text{out}} = 10\,\text{kW}$. The analytical calculation results are confirmed by measurements taken with the hardware demonstrator described in **Section IV**, whereby the DC output capacitance has been externally increased above the design value of 11.2 µF to realize the other indicated capacitances.

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expression for the peak-to-peak voltage ripple as

$$\Delta V_{\mathrm{pp}} = \frac{2\mathrm{A}\,\omega_1 \sin\theta_1 + 2\mathrm{B}\cos\theta_1}{(\mathrm{A}\omega_1)^2 + \mathrm{B}^2} + \frac{2\mathrm{A}\,w_2 \sin\theta_2 + 2\mathrm{B}\cos\theta_2}{(\mathrm{A}\omega_2)^2 + \mathrm{B}^2}, \tag{6}$$

with

$$\mathrm{A} = \frac{C_{\mathrm{out}}\,V_{\mathrm{out}}}{\hat{i}_{\mathrm{in}}\,\hat{v}_{\mathrm{CSR,CM}}}, \mathrm{B} = \frac{2I_{\mathrm{out}}}{\hat{i}_{\mathrm{in}}\,\hat{v}_{\mathrm{CSR,CM}}}, \theta_1 = \omega_1 t_{\mathrm{p}}, \theta_2 = \omega_2 t_{\mathrm{p}}, \tag{7}$$

where $\omega_1 = 2\pi(f_{\mathrm{CSR,CM}} + f_{\mathrm{in}})$, $\omega_2 = 2\pi(f_{\mathrm{CSR,CM}} - f_{\mathrm{in}})$, and $t_{\mathrm{p}} = {}^{1}/_{\omega_1} \cdot \mathrm{atan}({}^{\mathrm{A}\omega_1}/_{\mathrm{B}})$. Furthermore, f_{in} is the grid frequency and $\hat{v}_{\mathrm{CSR,CM}}$ and $f_{\mathrm{CSR,CM}}$ denote the amplitude and the frequency of the LF CM voltage injected by the CSR-stage, which should be compensated by the DC/DC-stage using VGC. The equation is visualized and verified in **Fig. 6** considering $V_{\mathrm{out}} = 1000\,\mathrm{V}$ (i.e., the worst-case operating point in terms of voltage stress for the DC/DC-stage transistors), $P_{\mathrm{out}} = 10\,\mathrm{kW}$ and different output capacitance values C_{out}. Note that an increased C_{out} leads to a reduced ΔV_{pp} as expected. Furthermore, a clear trade-off between the blocking voltage rating of the transistors in the DC/DC-stage and the system's power density is observed, i.e., a large output capacitance can be implemented to reduce the LF voltage variation but leads to a lower volumetric power density. Finally, $C_{\mathrm{out}} = 11.2\,\mu\mathrm{F}$ as originally designed based on a HF voltage ripple criterion and without taking into account VGC results in a peak blocking voltage stress on the DC/DC-stage HBs of $500\,\mathrm{V} + 150\,\mathrm{V} = 650\,\mathrm{V}$, which is compatible with the employed $900\,\mathrm{V}$ SiC transistors. Therefore, no design modifications are needed for VGC operation.

2) Buck-Mode

In the buck-mode operation, the output DC voltage is low enough to be directly generated by the buck-type CSR-stage. Then, the DC-link current is constant and equals the output current, i.e., $i_{\mathrm{DC}} = I_{\mathrm{out}}$ (see **Fig. 7.i**), and the CSR-stage operates with 3/3-PWM. As the step-up functionality of the DC/DC-stage is not needed, an advantageous synergetic control [35] allows to automatically clamp the DC/DC-stage, i.e., $\mathrm{T}_{\mathrm{DC,hp}}$ and $\mathrm{T}_{\mathrm{DC,hn}}$ are permanently turned on to reduce switching losses. However, this implies that $\bar{v}_{\mathrm{DC,CM}} = 0$ and hence the CM voltage becomes $\bar{v}_{\mathrm{mk}} = \bar{v}_{\mathrm{CSR,CM}} \neq 0$ as all typically employed 3/3-PWM switching sequences of the CSR-stage result in certain LF (mainly third-harmonic) CM voltage components [31].

However, it is of course possible to select a slightly higher DC-link current ($i_{\mathrm{DC}} = k_{\mathrm{VGC}} \cdot I_{\mathrm{out}}$ with $k_{\mathrm{VGC}} > 1$), such that the DC/DC-stage must be activated to step down the DC-link current to the output current. This, in principle, again opens the possibility of injecting a CM voltage $\bar{v}_{\mathrm{DC,CM}} = \bar{v}_{\mathrm{CSR,CM}}$ to compensate the CM voltage generated by the CSR-stage as shown in **Fig. 7.ii**. Thus, VGC can be achieved in the buck-mode, too, but results in switching losses of the DC/DC-stage, i.e., forgoes the advantageous clamping of the DC/DC-stage; however, relatively low additional switching losses are expected because of the low switched voltages. Furthermore, the DC-link current must be increased above the minimum necessary value, i.e., I_{out} in the buck-mode, to facilitate VGC. The required increase quantified by k_{VGC}, i.e., the sufficient margin for LF CM voltage injection by the DC/DC-stage, is thus clarified in the following.

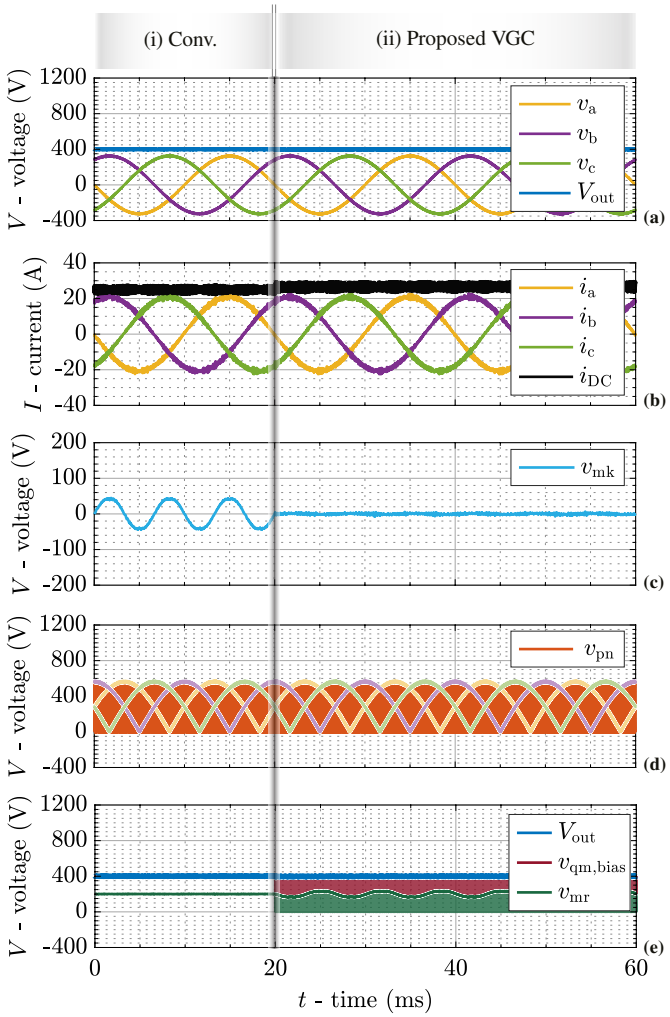

Fig. 7: Simulated key waveforms for operation in the buck-mode, **(i)** without and **(ii)** with VGC. **(a)** 3-Φ mains voltages v_{a}, v_{b}, v_{c} and DC output voltage V_{out}. **(b)** 3-Φ mains phase currents i_{a}, i_{b}, i_{c} and DC-link current i_{DC}. **(c)** CM voltage v_{mk}. **(d)** Switched voltage v_{pn} at the output of the CSR-stage; note that 3/3-PWM is used (i.e., the zero and/or shoot-through states are employed). **(e)** Switched voltages $v_{\mathrm{qm,bias}} = v_{\mathrm{qm}} + V_{\mathrm{out,n}}$ and v_{mr} at the input of the DC/DC-stage's upper and lower HBs. Note that the DC/DC-stage must be activated to realize VGC, which requires a slight increase of the DC-link current by about 5 % from 25 A to 26.4 A, see (b), as explained in the text.

Similar to the boost-mode operation, the value of the DC output capacitors C_{out} has a significant impact on the circuit operation. A smaller C_{out} leads to an increased output capacitor voltage variation (i.e., ΔV_{pp} increases) but this decreases the variation of the duty cycles d_{p} and d_{n} of the two DC/DC-stage HBs, which is required to generate the compensating $\bar{v}_{\mathrm{DC,CM}}$. This means that the duty cycles remain closer to unity, which, in turn, means that the required increase of the DC-link current over the output current becomes smaller. Thus, a smaller C_{out} is preferable for buck-mode operation as shown in **Fig. 8**, e.g., $i_{\mathrm{DC}} = 26.4\,\mathrm{A}$ ($k_{\mathrm{VGC}} = 1.05$, i.e., a 5 % increase) is needed at $400\,\mathrm{V}$, $10\,\mathrm{kW}$ to eliminate the LF CM emission ($\bar{v}_{\mathrm{mk}} = 0$) if $C_{\mathrm{out}} = 11.2\,\mu\mathrm{F}$ (realized design) but $i_{\mathrm{DC}} = 28.1\,\mathrm{A}$ would be necessary if a higher $C_{\mathrm{out}} = 200\,\mu\mathrm{F}$ would be used.

The dependencies of the needed DC-link current to enable VGC on the output voltage show distinct kinks at

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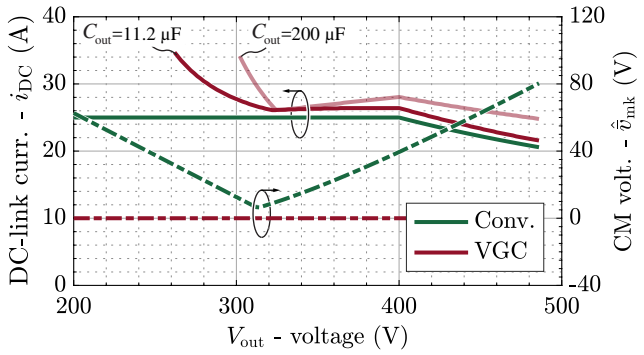

Fig. 8: Minimum buck-mode DC-link current i_{DC} (at rated load) and resulting peak LF CM voltage $\hat{\bar{v}}_{mk}$ at the DC output when operating with conventional synergetic control (green), i.e., with the DC/DC-stage clamped so that $\bar{v}_{mk} = \bar{v}_{CSR,CM}$, or the proposed VGC (red), where the DC/DC-stage injects a compensating LF CM voltage to realize $\bar{v}_{mk} = 0$. Note that a higher output capacitance C_{out} leads to a higher required DC-link current to facilitate VGC, e.g., $i_{DC} = 26.4\,A$ is needed at $400\,V$, $10\,kW$ to achieve zero LF CM emission if $C_{out} = 11.2\,\mu F$ (realized design) but $28.1\,A$ would be necessary if $C_{out} = 200\,\mu F$. The kink observed in the capacitance curves at around $V_{out} = 320\,V$ is explained in the text.

around $320\,V$ (see **Fig. 8**). This can be explained as follows: if the CSR-stage operates with a large modulation index $M = \hat{I}_{in}/I_{DC}$, i.e., $M > 0.65$ for $V_{out} > 320\,V$, the LF CM voltage $\bar{v}_{CSR,CM}$ generated by the CSR-stage is predominantly composed of the CM voltage contributions of the active switching states. Thus, increasing i_{DC} as required by VGC leads to a reduction of the LF CM voltage $\bar{v}_{CSR,CM}$ of the CSR-stage due to the shortened active switching states, i.e., advantageously *reduces* the LF CM voltage to be compensated by the DC/DC-stage. However, in the low-modulation-index region, i.e., for $M < 0.65$ at $V_{out} < 320\,V$, the CSR-stage's LF CM voltage $\bar{v}_{CSR,CM}$ is mainly defined by the zero switching state. Thus, increasing i_{DC} as needed to enable VGC also *increases* the LF CM voltage of the CSR-stage, which should be compensated in the first place. As a result, an even higher DC-link current would be required to achieve sufficient modulation margin for the DC/DC-stage, etc. This effect defines the lower output voltage limit of the proposed non-isolated EV charger, for which VGC can reasonably be employed (about $300\,V$ in the case at hand).

Thus, VGC is feasible in the buck-mode, too, but comes at the price of slightly increased switching losses (the DC/DC-stage switches comparably low voltages) and also slightly higher conduction losses (about $5\,\%$ higher DC-link current) compared to optimum synergetic operation with a clamped DC/DC-stage. The proposed VGC concept can thus achieve zero LF CM voltage ($\bar{v}_{mk} = 0\,V$) over a wide buck-boost output voltage range of $300\,V$ to $1000\,V$, which is crucial for the targeted EV charging application.

C. Ground Current Control (GCC)

So far, it has been shown how the proposed VGC can achieve zero LF CM voltage, i.e., $\bar{v}_{mk} = 0\,V$, in principle, and **Section III** discusses a closed-loop implementation that actually *controls* $\bar{v}_{mk}$ to zero. However, unless relatively large output capacitors are employed, still significant LF CM voltage components appear across the parasitic ground capacitors at the battery terminals, i.e., DC+ and DC-. Increasing the output capacitors, first, reduces the power density of the system and, second, increases the required extra DC-link current in buck-mode operation.

Therefore, it is desirable to implement a low-impedance grounding of the DC-output midpoint m, i.e., a direct connection of m to PE (see the dashed blue line in **Fig. 3** and **Fig. 4.c**), which essentially removes the parasitic capacitances at the battery terminals from the equivalent circuit schematic (since they are effectively connected in parallel to the relatively large output capacitors). Then, however, direct feedback control of the LF CM ground *current*, i.e., the proposed ground current control (GCC), is needed, which is also the most reliable way to prevent nuisance tripping of RCDs. The ground current is thus best measured as the sum of the three-phase mains phase currents, i.e., $i_{GND} = i_a + i_b + i_c$ as shown in **Fig. 3**, as the same measurement method is implemented in RCDs. Note that the considerations made in the context of VGC (e.g., regarding the voltage stress of the DC/DC-stage's power transistors, etc.) remain valid, as in theory (and considering sufficiently large output capacitors) achieving $\bar{v}_{mk} = 0$ is equivalent to realizing zero LF ground current, i.e., $i_{GND} = 0$. The latter, however, can advantageously also be achieved with small output capacitors.

III. Control Strategy

After clarifying the ideal operation of the two converter stages to achieve the proposed VGC or GCC, this section discusses the implemented control strategy that realizes that desired behavior. The proposed control strategy (see **Fig. 9**) is closely based on the synergetic control concept described in [35], and therefore especially the modifications necessary to implement VGC or GCC are highlighted in the following. Note that the proposed control strategy can also cope with irregular mains conditions, as is briefly discussed in the **Appendix**.

A. Output Voltage and DC-Link Current Control

The outermost control loop performs the output voltage regulation (see *Output Voltage Control* block in **Fig. 9**). The difference between the measured V_{out} and the reference output voltage V_{out}^* defines the input power reference P^* through a PI-controller. To ensure ohmic mains behavior, this power reference is then translated into an input conductance reference

$$G^* = \frac{P^*}{\frac{3}{2}\hat{V}_{in}^2}. \tag{8}$$

In the following *DC-Link Current Reference Generation* block, this ensures 3-Φ sinusoidal mains current references i_a^*, i_b^*, and i_c^* that are proportional to the corresponding 3-Φ input voltages v_a, v_b, and v_c, i.e., realizes ohmic behavior.

For operation in the boost-mode with 2/3-PWM, the upper envelope of the absolute 3-Φ sinusoidal mains current references defines the (time-varying) DC-link current reference $i_{DC,2/3}^*$. In contrast, for buck-mode operating points, the DC-link current must be at least as high as the output current reference. However, note that if VGC (or GCC) is employed, this minimum value must be slightly increased by a factor

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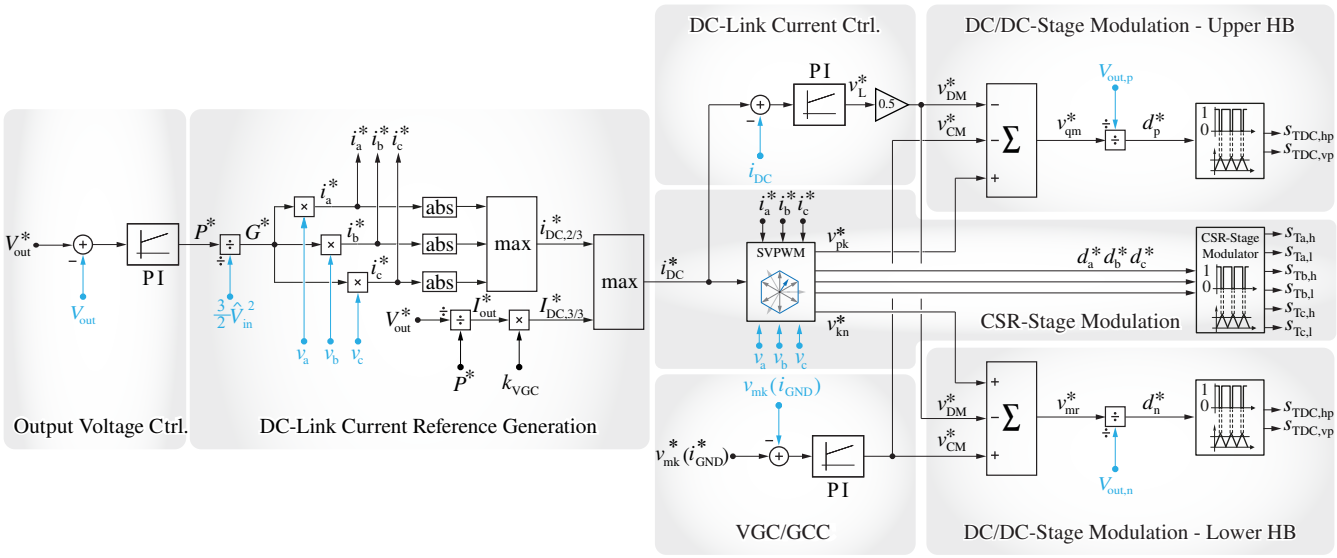

Fig. 9: Proposed control block diagram for the 3-Φ bB current DC-link PFC rectifier system shown in **Fig. 3**. It is based on the synergetic control concept from [20] but in addition implements virtual grounding control (VGC) or ground current control (GCC). The functionality and the interaction of the individual control blocks are described in the text. Note that all quantities refer to local average values here.

$k_{\mathrm{VGC}} > 1$ (see **Section II-B2** above), with typical values being in the order of about $k_{\mathrm{VGC}} = 1.05$, i.e., $I^*_{\mathrm{DC,3/3}} = k_{\mathrm{VGC}} \cdot I^*_{\mathrm{out}} = k_{\mathrm{VGC}} \cdot P^*/V^*_{\mathrm{out}}$. Finally, selecting the DC-link current reference as $i^*_{\mathrm{DC}} = \max\left(i^*_{\mathrm{DC,2/3}}, I^*_{\mathrm{DC,3/3}}\right)$ ensures automatic transitions between 2/3-PWM in the boost-mode and 3/3-PWM in the buck mode.

The inner DC-link current control loop calculates the required voltage v^*_{L} across the DC-link inductor L_{DC} by comparing the reference i^*_{DC} and the measured i_{DC} DC-link current in the *DC-Link Current Control* block. To achieve the proposed VGC or GCC, the DC/DC-stage needs to operate at all times (especially also in the buck-mode, which is different from conventional synergetic control [35] without VGC), the control voltage v^*_{L} is exclusively realized by the DC/DC-stage, e.g., a positive v^*_{L} is generated by a decreased input voltage v_{qr} of the DC/DC-stage.

B. Virtual Grounding Control & Ground Current Control

The *VGC/GCC* block, finally, implements either VGC or GCC with a PI controller to calculate the LF CM voltage injection reference v^*_{CM} for the DC/DC-stage. Specifically, for VGC v^*_{CM} is obtained by feeding the difference between the reference v^*_{mk}, i.e., in most cases $v^*_{\mathrm{mk}} = 0\,\mathrm{V}$, and the measured v_{mk} CM voltage thought a PI controller. For GCC, the error between the reference $i^*_{\mathrm{GND}} = 0\,\mathrm{A}$ and the measured i_{GND} ground current serves as the controller input. The system modeling and the PI controller tuning are conducted based on [28] and not detailed here for the sake of brevity.

C. CSR-Stage and DC/DC-Stage Modulation

The CSR-stage modulation is implemented in the *CSR-Stage Modulation* block. The 3-Φ mains current references and the DC-link reference current serve as inputs to an SVPWM (Space Vector based Pulse Width Modulation) unit, which generates the 3-Φ duty cycles d^*_{a}, d^*_{b}, and d^*_{c}, which the PWM modulator finally translates into the switch-level gate signals that ensure correct commutation sequences for the CSR-stage's commutation cells. Furthermore, the SVPWM unit calculates the LF voltages v^*_{pk} and v^*_{kn} at the output of the CSR-stage's upper and lower commutation cell from the measured 3-Φ input voltages v_{a}, v_{b}, and v_{c}, which are then used as feed-forward terms for the DC/DC-stage modulation.

In the *DC/DC-Stage Modulation* block, the DC-link current controller output v^*_{L}, the feed-forward voltage terms v^*_{pk} and v^*_{kn} from the CSR SVPWM unit, and the VGC/GCC controller output voltage v^*_{CM} are summarized to obtain the input voltage reference of the upper DC/DC-stage HB as

$$v^*_{\mathrm{qm}} = v^*_{\mathrm{pk}} - v^*_{\mathrm{DM}} - v^*_{\mathrm{CM}}, \tag{9}$$

and of the lower HB as

$$v^*_{\mathrm{mr}} = v^*_{\mathrm{kn}} - v^*_{\mathrm{DM}} + v^*_{\mathrm{CM}}. \tag{10}$$

Selecting $v^*_{\mathrm{DM}} = 0.5 v^*_{\mathrm{L}}$ ensures that the DM control voltage v^*_{L} is generated by the upper and lower HBs equally to avoid CM voltage injection and thus disturbing or interfering with the CM control loop. Furthermore, the upper and lower HBs realize the CM control voltage v^*_{CM} without generating DM voltages, which is proved by v^*_{CM} appearing in v^*_{qm} and v^*_{mr} with opposite sign but identical amplitude. Thus, the DM and CM control loops are fully decoupled and independent. Finally, the DC/DC-stage duty cycles d^*_{p} and d^*_{n} are calculated, taking into account the respective measured output capacitor voltages, $V_{\mathrm{out,p}}$ and $V_{\mathrm{out,n}}$.

IV. Experimental Results

To validate the proposed VGC and GCC concepts, a hardware demonstrator (see **Fig. 10**) of the 3-Φ bB current DC-link PFC rectifier system has been realized according to the specifications shown in **Tab. I** with 1200 V SiC MOSFETs (CREE *C3M0021120K*) in the CSR-stage and 900 V SiC

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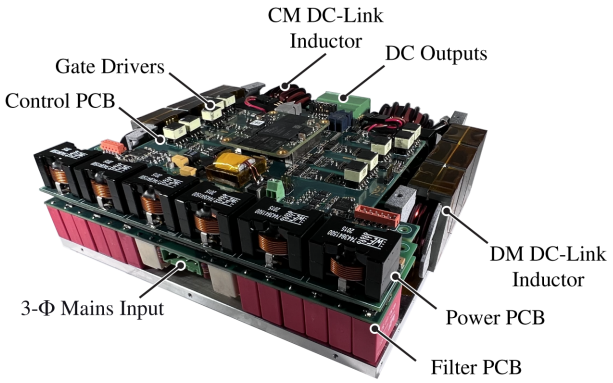

Fig. 10: Photo of the realized 10 kW 3-Φ current DC-link buck-boost PFC rectifier (see **Fig. 3**) hardware demonstrator, which interfaces a 400 V mains and a DC output voltage in the range of 300 V to 1000 V; detailed specifications are given in **Tab. I**. Employing 1200 V SiC (CSR-stage) and 900 V SiC (DC/DC-stage) MOSFETs, the converter achieves a power density of $6.4\,\mathrm{kW/dm^3}$ ($184\times172\times49\,\mathrm{mm^3}$) or $107.5\,\mathrm{W/in^3}$ ($7.2\times6.8\times1.9\,\mathrm{in^3}$).

MOSFETs (CREE *C3M0010090K*) in the DC/DC-stage. The experiments focus on operation in the boost-mode, as this can be considered a more challenging scenario (the DC/DC-stage shapes the DC-link current to facilitate 2/3-PWM of the CSR-stage *and* now also realizes the VGC or GCC functionality). The results demonstrate that GCC facilitates compliance with the relevant standards for EV chargers such as UL 2202 [2] and IEC 61851 [3], considering two different grid grounding systems (TT and TN [41]). The VGC and GCC functionalities are achieved without a significant efficiency penalty compared to the state-of-the-art synergetic operation, which is finally verified by measured efficiencies of the realized demonstrator.

A. Operation with VGC

Fig. 11 and **Fig. 12** show measured key waveforms when the hardware demonstrator (see **Fig. 10**) is operated with the conventional synergetic control [35], i.e., without VGC, or with the proposed VGC, respectively. In both cases, a resistive load of $110\,\Omega$ is used and the output voltage is varied to realize operating points between $V_{\mathrm{out}} = 700\,\mathrm{V}$, $P_{\mathrm{out}} = 4.5\,\mathrm{kW}$ and $V_{\mathrm{out}} = 1000\,\mathrm{V}$, $P_{\mathrm{out}} = 9.1\,\mathrm{kW}$. The output midpoint m is left floating, i.e., the grounding impedance is defined by the parasitic capacitors only.

The experimental results confirm the simulation results provided earlier in **Fig. 5**. The LF component of the CM voltage v_{mk} originally contains a significant (80 V amplitude) component at 150 Hz (see **Fig. 11**), which VGC reduces to almost zero (2.2 V RMS at $V_{\mathrm{out}} = 1000\,\mathrm{V}$, see **Fig. 12**). Note that even though the two output capacitor voltages vary, the total output voltage is always a constant DC value also with the proposed VGC. This confirms that the regulation of the CM voltage does not interfere with the system's DM behavior, i.e., CM and DM quantities can be controlled independently. Finally, **Fig. 13** shows the spectra of v_{mk} as calculated from the recorded waveforms, which confirms the suppression of the LF CM voltage components and highlights that the proposed VGC results in the amplitudes of all harmonics below 5 kHz to be less than 1 V.

B. Operation with GCC

First, the required ground current i_{GND} measurement for GCC is realized by feeding the three input phase conductors through a high-precision *LEM CTSR-0.6P* [42] current sensor with a measurement range of up to 600 mA (see **Fig. 3**), which is intended for leakage current measurements in transformerless PV inverters. The bandwidth of the designed ground current controller is 1.5 kHz. The proposed GCC is then tested under the same load scenario as used with VGC above, and the measured key waveforms shown in **Fig. 14** are, as expected, very similar to those obtained for VGC (see **Fig. 12**). With GCC, however, the ground current i_{GND} is directly regulated instead of the CM voltage v_{mk}. Note that by connecting m to PE, the battery parasitic capacitors, e.g., $C_{\mathrm{b,DC+}}$, $C_{\mathrm{b,DC-}}$, and $C_{\mathrm{b,m}}$ as shown in **Fig. 3**, are effectively short-circuited or connected in parallel to the output capacitors, and are thus irrelevant. Therefore, GCC achieves ground current regulation capability without the need for large output capacitances (the demonstrator uses only $C_{\mathrm{out}} = 11.2\,\mu\mathrm{F}$), which facilitates compact non-isolated EV chargers.

1) TT and TN Grounding Systems

Moreover, two different grid grounding systems [6] must be distinguished when evaluating the performance of the proposed GCC.

- TN (terra-neutral): in a TN system, the converter's PE and the mains neutral point (i.e., the star-point of the nearest transformer's LV-side winding system) are directly connected via a dedicated PE conductor. Thus, with respect to **Fig. 3**, $R_{\mathrm{G}} = R_{\mathrm{N}} = 0\,\Omega$ models a TN grounding system.
- TT (terra-terra): in a TT system, there is no dedicated PE conductor. Instead, the mains neutral point is locally grounded via an impedance in the order of $R_{\mathrm{N}} = 10\,\Omega$ [6], and the converter's PE terminal is connected to ground locally, too, whereby a worst-case grounding impedance of $R_{\mathrm{G}} = 100\,\Omega$ according to IEC60364-4 [41] must be assumed. Note that in contrast to a TN system, any ground current flows through R_{G}, which results in a corresponding voltage drop between the local PE and true earth and thus potentially endangers a person touching the vehicle chassis while standing next to it. Therefore, for example, UL 2202 and also IEC 61851 require a so-called touch current test (see **Section IV-B3** below).

In the test setup, R_{N} and R_{G} are realized with explicit resistors to mimic the two scenarios.

2) Ground Current Measurements

Fig. 15 shows the measured ground current i_{GND} at different output power levels and for $V_{\mathrm{out}} = 700\,\mathrm{V}$ and $V_{\mathrm{out}} = 1000\,\mathrm{V}$. Considering that i_{GND} features an amplitude in the range of several milliamperes only, a special leakage current clamp meter *Fluke 368 FC*, specifically designed for RCD testing, is used to accurately measure i_{GND}. The device performs a true-rms measurement with 0.01 mA resolution, considering a frequency range of 40 Hz to 1 kHz [39].

Note that i_{GND} occurring in the TN system ($R_{\mathrm{G}} = R_{\mathrm{N}} = 0\,\Omega$ in **Fig. 3**) is always larger than i_{GND} resulting in the TT system ($R_{\mathrm{G}} = 100\,\Omega, R_{\mathrm{N}} = 10\,\Omega$) due to the increased series impedance. However, all measured values are between 2.8 mA

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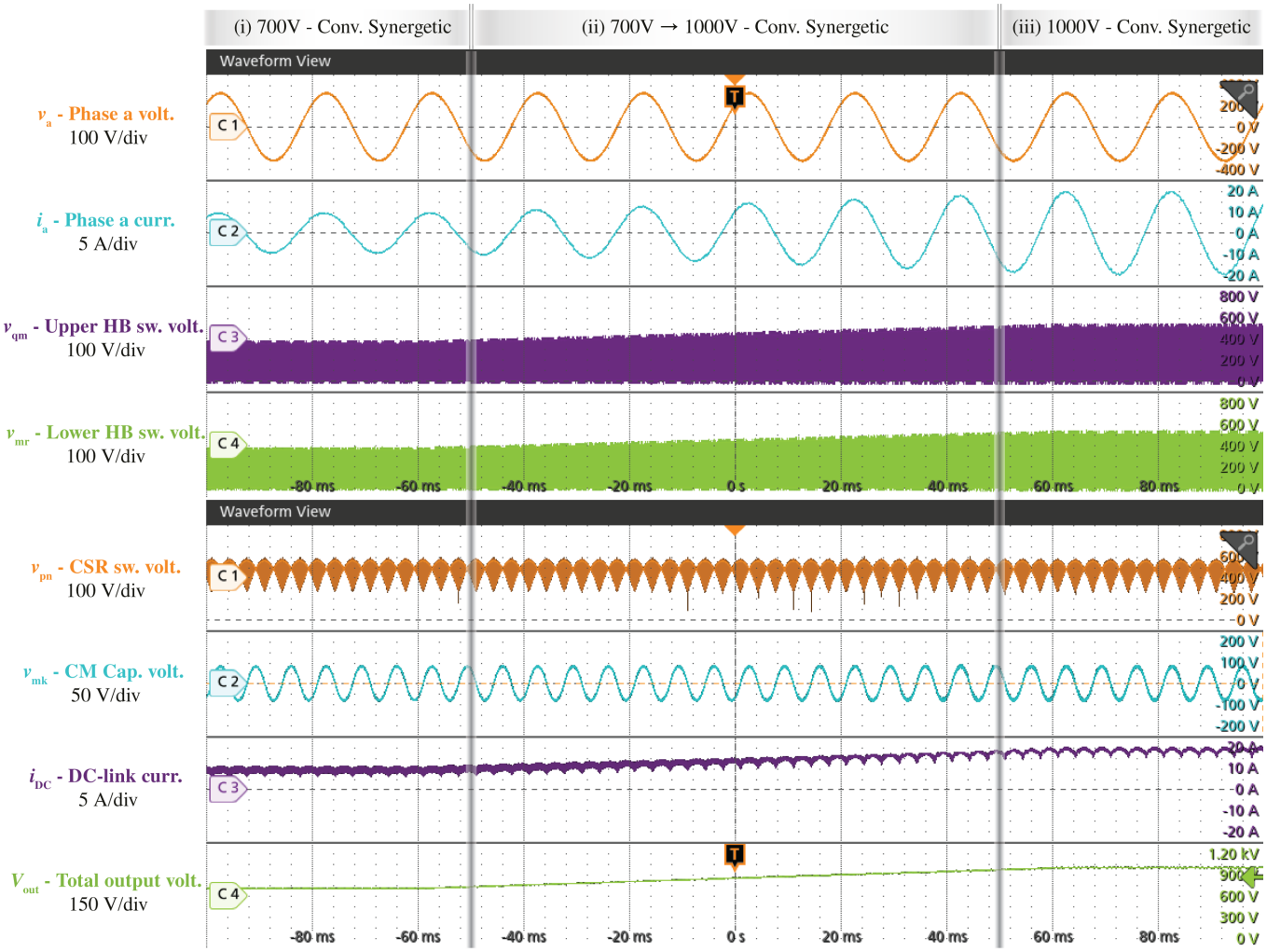

Fig. 11: Experimental waveforms of the converter operating with the conventional synergetic control strategy [35], i.e., without activating the proposed VGC or GCC. Using a resistive load of 110 Ω and varying the output voltage, different operating points between $V_{out} = 700\,V$, $P_{out} = 4.5\,kW$ and $V_{out} = 1000\,V$, $P_{out} = 9.1\,kW$ are covered. Note that the CSR-stage operates with 2/3-PWM (boost-mode), and especially note that the CM voltage v_{mk} shows a pronounced 150 Hz component with an amplitude of approximately 80 V, which originates from the SVPWM of the CSR-stage [31].

(TT system, 10 kW) and 5.4 mA (TN system, 2 kW), and thus far below the typical RCD trip levels of 30 mA [2], [3]. The values are, in particular, also below the permissible PE conductor current in normal operation (7.25 mA RMS for a 10 kW system) according to IEC 61140 [43].

3) Touch Current Test

Even though the TT system's higher grounding impedances, i.e., R_G and R_N, lead to lower ground current values, the ground current flowing through R_G creates a potential difference between the local EV PE (e.g., the chassis) and true earth, which implies a risk for electric shocks to humans [6]. Thus, standards (UL 2202, IEC 61851) require a so-called touch current test, where an impedance network modeling the frequency-dependent impedance of the human body is connected between the local EV PE (note that in case of GCC, a direct connection of PE and the DC output midpoint m is used) and true earth, see **Fig. 16**. The figure also shows the body voltage V_{body} obtained by post-processing the voltage V_{touch} with the impedance networks' transfer function; V_{touch} is measured across the explicit resistor R_G used to realize a TT grounding system. The resulting $V_{body} \approx 110\,mV$ is well below the most stringent limit of 250 mV defined by UL 2202 [2]. There is little dependence on the output voltage and power level, because mainly LF CM components, which are strongly suppressed by the GCC, contribute to V_{body} (the human body impedance network features a low-pass filter characteristic). Note that only the TT system is considered here since the TN system's dedicated PE conductor ($R_G \approx 0$) prevents any significant voltage between the chassis and true ground (i.e., $V_{touch} \approx 0$) even for non-zero ground current.

4) Efficiency

Fig. 17 shows the measured system efficiencies when operating the demonstrator at two different output voltages ($V_{out} = 700\,V$ and 1000 V), with or without the proposed GCC enabled. All efficiencies have been measured with a Yokogawa WT3000 power analyzer over a wide output power range. GCC has only little impact on the efficiency for the following reasons: (i) The same converter conduction losses, which are solely dependent on the DC-link current if neglecting HF

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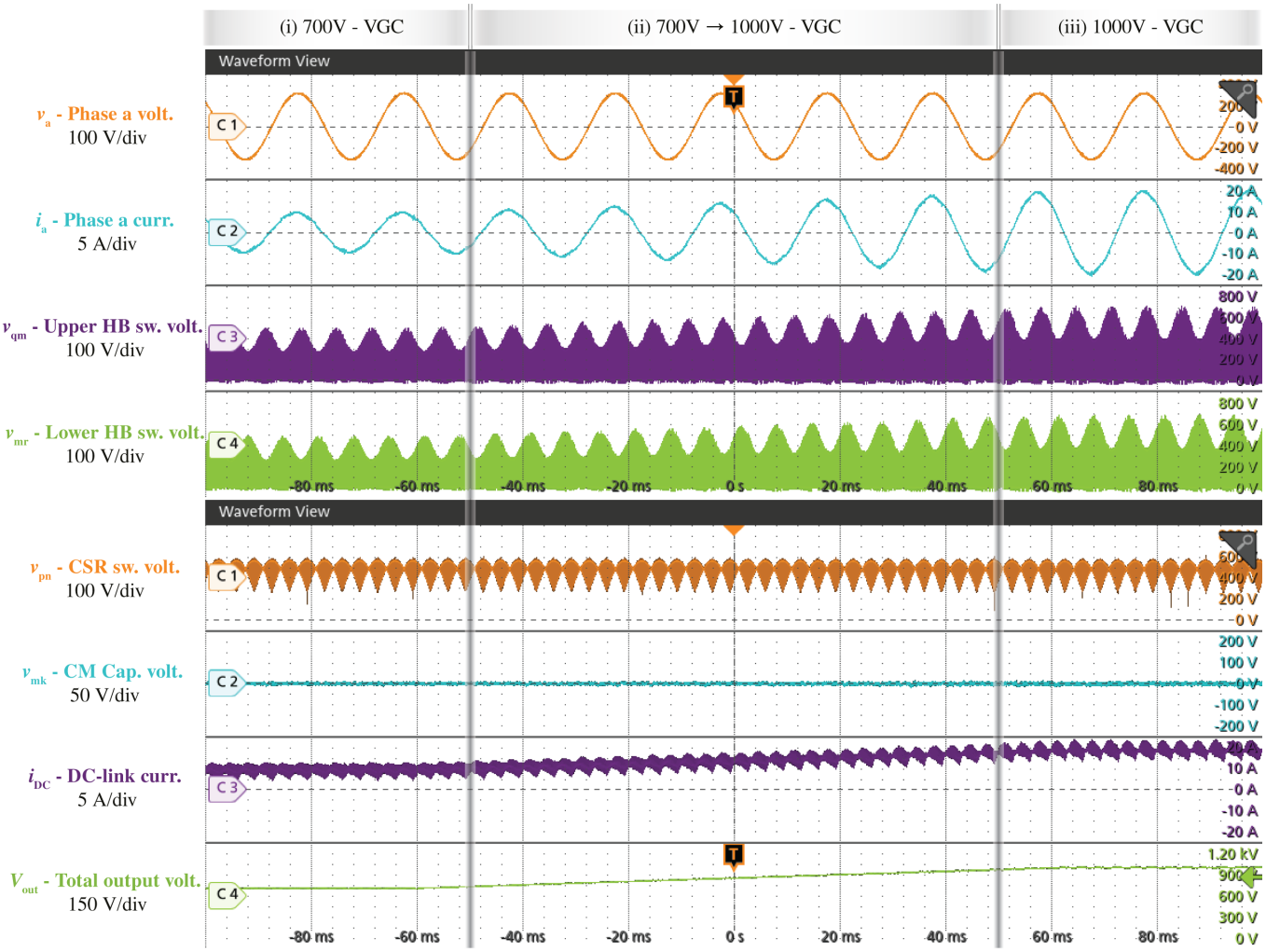

Fig. 12: Experimental waveforms of the converter with VGC enabled, which suppresses the LF component of the CM voltage v_{mk} almost completely (see also **Fig. 13**). Again (see **Fig. 11**), using a resistive load of 110 Ω and varying the output voltage, different operating points between $V_{\mathrm{out}} = 700\,\mathrm{V}$, $P_{\mathrm{out}} = 4.5\,\mathrm{kW}$ and $V_{\mathrm{out}} = 1000\,\mathrm{V}$, $P_{\mathrm{out}} = 9.1\,\mathrm{kW}$ are covered. Note that the CSR-stage still operates with 2/3-PWM (boost-mode) and also note the expected opposed fluctuation of the two output capacitor voltages, which is visible in the envelopes of the DC/DC-stage HB's switched voltages, v_{qm} and v_{mr}.

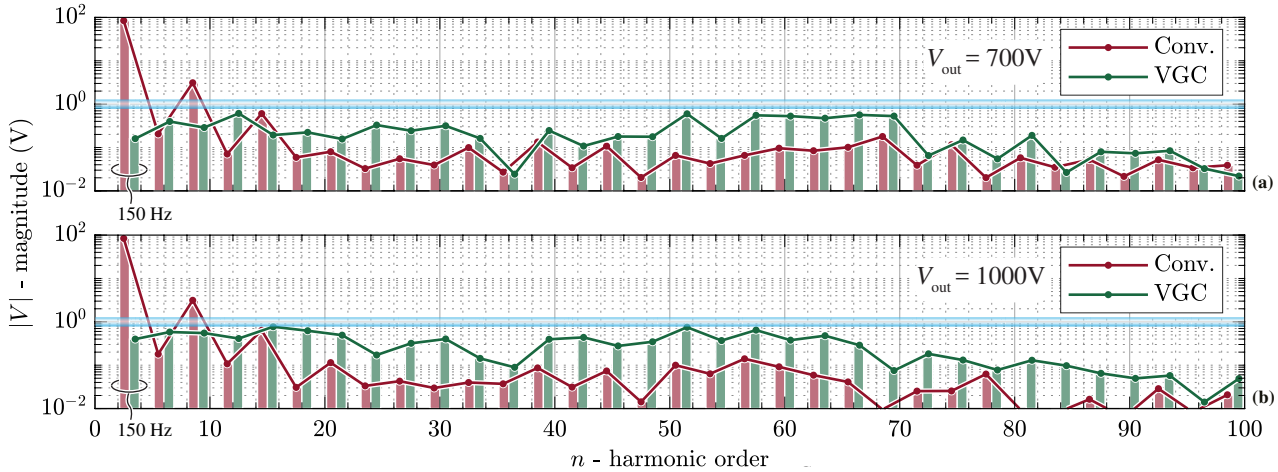

Fig. 13: Comparison of the harmonic spectra calculated from measured v_{mk} when operating without (**Fig. 11**) and with (**Fig. 12**) the proposed VGC at **(a)** $V_{\mathrm{out}} = 700\,\mathrm{V}$, $P_{\mathrm{out}} = 4.5\,\mathrm{kW}$ and **(b)** $V_{\mathrm{out}} = 1000\,\mathrm{V}$, $P_{\mathrm{out}} = 9.1\,\mathrm{kW}$; in all cases from a 50 Hz mains. Note that VGC successfully suppresses LF CM voltage harmonics, i.e., especially the third-harmonic component is reduced from 80 V without VGC to less than 1 V with VGC.

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Fig. 14: Experimental waveforms of the converter with GCC enabled and using a TN grounding system configuration (direct low-impedance connection of the three-phase source's star-point and the converter's PE, i.e., $R_N = R_G = 0\,\Omega$ in **Fig. 3**). Again, using a resistive load of $110\,\Omega$ and varying the output voltage, different operating points between $V_{out} = 700\,V$, $P_{out} = 4.5\,kW$ and $V_{out} = 1000\,V$, $P_{out} = 9.1\,kW$ are covered. Note the expected similarity of all waveforms to those obtained with VGC in **Fig. 12**. GCC achieves an RMS ground current of less than $5\,mA$ ($40\,Hz$ to $1\,kHz$) as confirmed by a *Fluke 368 FC* leakage current clamp meter.

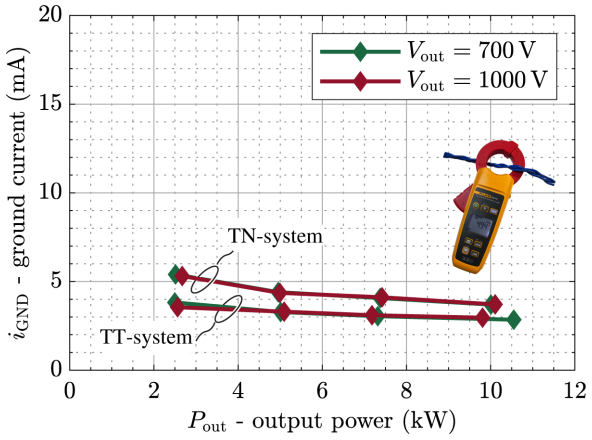

Fig. 15: Ground current i_{GND} measured with a leakage current clamp meter *Fluke 368 FC* [39] for operation with two different output voltages and various power levels from 25 % to 100 % of rated load. For both grounding schemes (TT and TN), the measured ground current remains far below RCD trip levels of $30\,mA$.

ripples, are generated.[2] (ii) The CSR-stage always operates with 2/3-PWM and hence generates identical switching losses. (iii) Even though the switched voltages of the DC/DC-stage ($V_{out,p}$ and $V_{out,n}$) are varying with $150\,Hz$ if GCC is used, the total output V_{out} stays constant. The switching losses of SiC MOSFETs can be modeled as [20]

$$E_{sw} = (k_1 I_{sw}^2 + k_2 I_{sw} + k_3) V_{sw} + (C_{oss,Q}) V_{sw}^2. \qquad (11)$$

Therefore, considering the *sum* of the upper and lower DC/DC-stage HB's switching losses, the loss contribution resulting from voltage/current overlap (the first term in (11)) does not depend on the ratio $V_{out,p}/V_{out,n}$ due to the linear dependency on the switched voltage V_{sw}. In contrast, the capacitive loss term shows a quadratic dependency on the switched voltage V_{sw} and hence slightly increased losses are expected if GCC

[2]This applies to the boost-mode operation considered here; note that in the buck-mode, a slightly higher (yet still minor) impact of VGC/GCC on the converter efficiency would be expected as the DC/DC-stage cannot be clamped and because of the necessary increase of the DC-link current by about 5 %.

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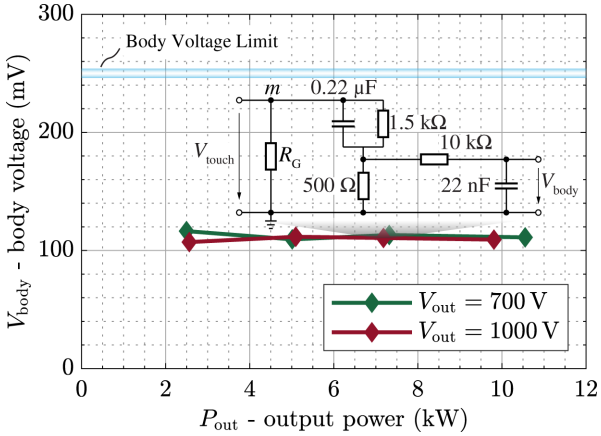

Fig. 16: Body voltage V_{body} obtained by processing the measured touch voltage V_{touch} with the transfer function of the human body impedance network according to UL 2202. The converter operates with the proposed GCC at $V_{out} = 700\,V$ and $V_{out} = 1000\,V$, considering different output power levels. In all cases, the measured body voltages of around $110\,mV$ are well below the safe level of $250\,mV$ defined in UL 2202 [2].

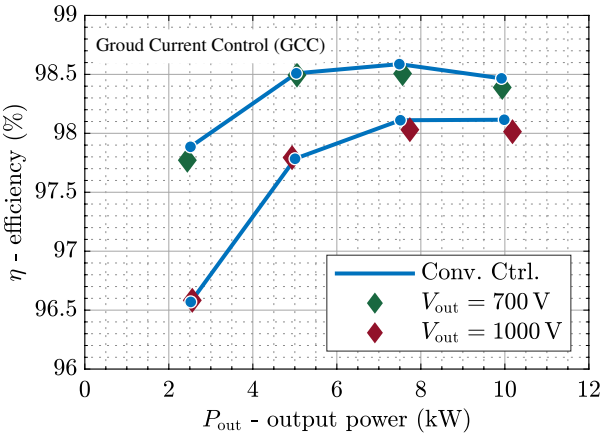

Fig. 17: Measured (Yokogawa WT3000) efficiencies of the $10\,kW$ hardware demonstrator (see **Fig. 10**) with $V_{out} = 700\,V$ and $V_{out} = 1000\,V$ (i.e., boost-mode) and for various output power levels. Enabling GCC has almost no impact on the efficiency; and with or without GCC a high peak efficiency of about $98.5\,\%$ is achieved.

is used. The impact on the overall system efficiency, however, remains very limited as the measurement results demonstrate. All in all, the built $10\,kW$ hardware demonstrator achieves high efficiencies over a wide operating range, reaching a peak efficiency of about $98.5\,\%$ at $V_{out} = 700\,V$ and rated load.

V. Conclusion

Targeting non-isolated EV chargers supporting a wide output voltage range of $300\,V$ to $1000\,V$, this paper proposes virtual grounding control (VGC) for a three-phase (3-Φ) buck-boost (bB) current DC-link AC/DC converter that consists of a buck-type current-source rectifier (CSR) stage and a boost-type three-level DC/DC-stage. Whereas HF CM conducted emissions are limited by the EMI filter, LF CM voltage components inherently resulting from the CSR-stage modulation can be compensated by the DC/DC-stage. This enables VGC to control the LF CM voltage between the DC-output midpoint and an artificial star-point of the three-phase mains (formed by the CSR-stage's input capacitors) to zero, i.e., establishes a virtual connection. Furthermore, the proposed ground current control (GCC) allows a direct connection of the DC output midpoint to protective earth (PE), see the dashed lines in **Fig. 3**, by regulating the measured LF CM ground current (i.e., the sum of the three mains phase currents) to near zero and hence prevents nuisance tripping of mandatory RCDs. Both, VGC and GCC are experimentally verified with a $10\,kW$ hardware demonstrator considering TT and TN grid grounding systems. With a directly grounded DC output midpoint, the measured LF CM ground leakage current is less than $6\,mA$ rms for all considered cases, i.e., significantly below the typical $30\,mA$ trip level of RCDs. Similarly, considering the human-body impedance network defined in UL 2202 (touch current test), the resulting test voltage of $110\,mV$ is clearly below the most stringent limit ($250\,mV$) of the standard. GCC is found to have only a minor impact on the efficiency, with the compact ($6.4\,kW/dm^3$ or $107.5\,W/in^3$) demonstrator reaching a peak efficiency of $98.5\,\%$.

Appendix

The resilient operation of the analyzed 3-Φ bB current DC-link PFC rectifier (see **Fig. 3**) under irregular mains conditions has been already comprehensively verified in [35], but without the proposed VGC/GCC. Therefore, this Appendix briefly demonstrates that the proposed VGC can cope with irregular mains conditions, e.g., asymmetric mains voltage amplitudes ($\pm 10\%$) [3] and mains voltages with low-frequency harmonic distortions [44].

Under such irregular 3-Φ mains conditions, the artificial star-point k of the three-phase mains formed by the CSR-stage's input capacitors (see **Fig. 3**) does not always stay at the same potential as PE. Thus, to tolerate irregular mains conditions, the ground voltage $\bar{v}_{mPE}$ used for VGC must be directly measured between the output midpoint m and the PE conductor. Even though we use VGC as an example here, note that again all considerations made are likewise applicable for GCC; for GCC, the measurement of the ground current (i.e., as the sum of the 3-Φ currents) remains the same as for operation with symmetric 3-Φ mains.

Fig. 18 verifies the resilient operation of the proposed VGC under asymmetric 3-Φ mains conditions (voltage amplitudes $+10\%$ in phase a and -10% in phase b [3]. The DC-link current i_{DC} follows the upper envelope of the 3-Φ current absolute values to still ensure 2/3-PWM. The CM voltage v_{mPE} is distorted but still can be compensated to zero after activating the proposed VGC. Note that the lower envelope of $v_{qm,bias}$ and the upper envelope of v_{mr} indicate the time-varying output capacitor voltages $V_{out,p}$ and $V_{out,n}$, while the sum of both, i.e., the output voltage V_{out}, remains almost constant.

Fig. 19 presents the operation of the proposed VGC when several voltage harmonics, e.g., 12% of 5th, 10% of 7th, and 7% of 11th, are added on top of the 3-Φ sinusoidal mains voltages [44]. Note that 2/3-PWM can still be maintained. Importantly, the CM voltage regulation performance is not affected by the mains voltage distortions. Even though harmonics besides the already existing $150\,Hz$ component (see

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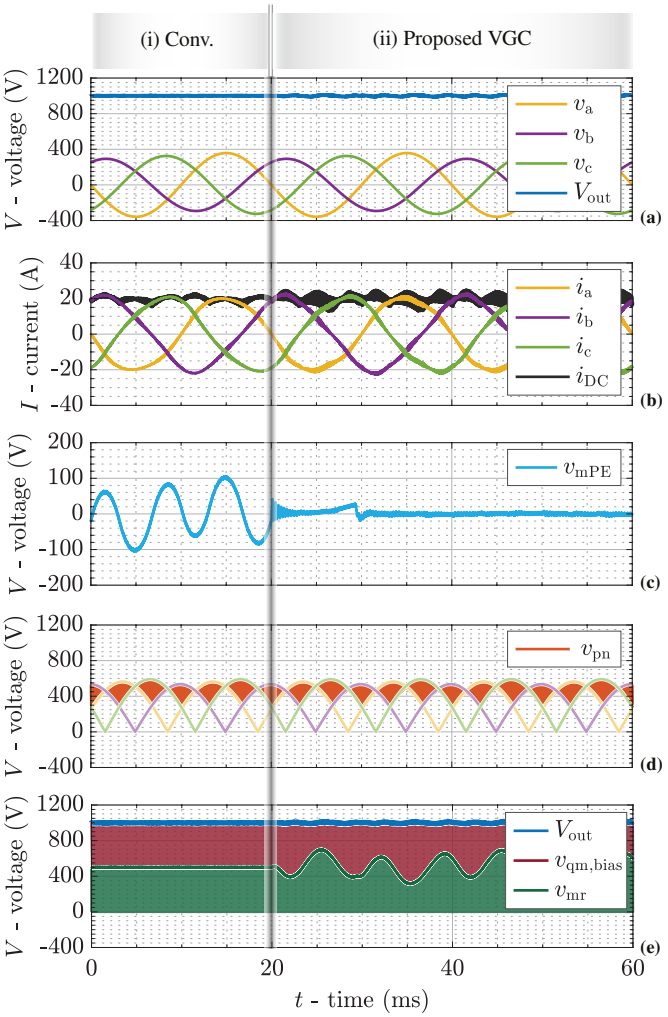

Fig. 18: Simulated key waveforms for operation in the boost-mode under asymmetric 3-Φ mains voltage amplitudes, e.g., $+10\%$ in phase a and -10% in phase b, **(i)** regulated by conventional synergetic control without VGC and **(ii)** with the proposed VGC, where $V_{out} = 1000\,\mathrm{V}$ and $P_{out} = 10\,\mathrm{kW}$.

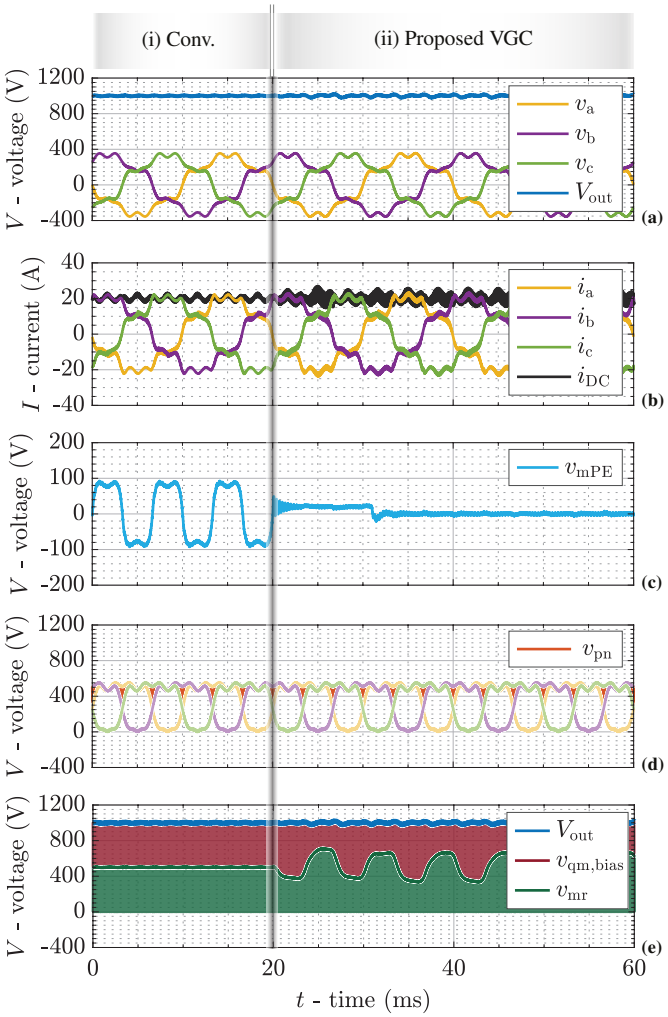

Fig. 19: Simulated key waveforms for operation in the boost-mode with distorted mains voltages (i.e., the 3-Φ mains voltages contain 12% of 5th, 10% of 7th, and 7% of 11th harmonics [44]), **(i)** regulated by conventional synergetic control without VGC and **(ii)** with the proposed VGC, where $V_{out} = 1000\,\mathrm{V}$ and $P_{out} = 10\,\mathrm{kW}$.

Fig. 5) appear in the two output capacitor voltages $V_{out,p}$ and $V_{out,n}$, again the sum of both, i.e., the output voltage V_{out}, remains almost constant.

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