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Novel Three-Phase Electronic Transformer

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Novel Three-Phase Electronic Transformer

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Abstract—Electronic transformers enable galvanic isolation and voltage level adaption at high frequency and thus the magnetic core volume and weight can be reduced substantially compared to traditional transformers operating at the grid frequency. This paper introduces a novel phase-modular single-stage three-phase electronic transformer (3Φ -ET) which advantageously enables the use of standard power transistors with unipolar voltage blocking capability. The output frequency is identical to the grid input frequency and the bidirectional power flow can be adjusted by means of a simple dual-active-bridge-(DAB)-type modulation which results in inherently sinusoidal grid currents. The 3Φ -ET is thoroughly described and experimental waveforms with a 6 kW prototype system operated in a 400V (rms, line-line) three-phase grid provide a proof of concept and verify the theoretical considerations.

Index Terms—Three-phase, ac-ac, high-frequency isolated, bidirectional, converter, electronic transformer, SST, DAB.

I. INTRODUCTION

Transformers are a key component for electric energy distribution and realize voltage level adaption and galvanic isolation in the grid. However, the magnetic cores of line-frequency transformers (LFTs) are bulky and heavy due to the large voltage-time area (VTA) applied to the transformer windings, thus promoting interest in solid-state transformer (SST) concepts with medium-/high-frequency transformers (MFTs / HFTs) promising substantial weight and volume gains as well as additional functionality such as fault handling and voltage regulation [1,2]. A single-stage single-phase ac-ac SST was first proposed in the late sixties [3] (building on the older concept of a thyatron-based "dc transformer" [4]) and employed power switches with bipolar voltage blocking capability¹ and a center-tapped HFT. Output voltage control was enabled by a simple carrier

¹Standard power transistors such as MOSFETs with a body diode are capable of conducting current in both (positive and negative) directions but cannot block both voltage polarities, i.e., have unipolar voltage blocking capability and can only control the current flow in one direction. In contrast power switches with bipolar voltage blocking capability (today typically realized as an inverse-series connection of two MOSFETs and in future using two-gate monolithic ac-switches) can block both voltage polarities and can control the current flow in both directions.

phase-shift strategy and experimental verification was later obtained in [5]. As the output frequency f_{AC} was tied to the input frequency f_{ac} and could not be adjusted, the system was also referred to as an "electronic transformer". This single-phase ac-ac SST concept was also adapted to form a three-phase SST in [6] and realized as a three-stage SST with an additional folder ($ac \rightarrow |ac|$) and unfold ($|ac| \rightarrow ac$) converter stage [7,8] in order to allow the use of standard power transistors with unipolar voltage blocking capability. Ever since, countless SST concepts with [9]–[14] and without [10,15]–[18] the capability of adjusting the output frequency with respect to the grid input frequency were proposed with a categorization provided in [1,2].

This paper introduces the novel three-phase electronic transformer (3Φ -ET; i.e., with $f_{AC} = f_{ac}$) depicted in **Fig. 1** with a simple dual-active-bridge-(DAB)-type modulation resulting in naturally sinusoidal grid currents. Compared to state-of-the-art systems with the same functionality, the 3Φ -ET rectifies several conceptual short-comings: Such SSTs are typically realized as either a) a single-stage system employing power switches with bipolar voltage blocking capability [3,5,6,19], or b) a multi-stage system with standard power transistor [7,8]. In contrast, the 3Φ -ET enables single-stage HF energy conversion and the use of standard power transistors with unipolar voltage blocking capability. Advantageously the power transistors of the 3Φ -ET are arranged in a half-bridge configuration (i.e., with a short and clearly defined commutation path enabling high switching speeds with moderate switch-node overvoltages) similar to the non-isolated ac front-ends in [20]–[22] and the SSTs in [15,23]. In contrast to [15], where a complex resonant circuit is required due to the weak transformer coupling present in the considered wireless power transfer application, the 3Φ -ET employs a standard HFT (with high coupling) enabling power-flow control by means of a simple DAB-type modulation. Further, the 3Φ -ET HFT shows improved utilization compared to the center-tapped HFTs in [3,5,6,16] where transient switch-node overvoltages may result due to the HFT leakage inductance.

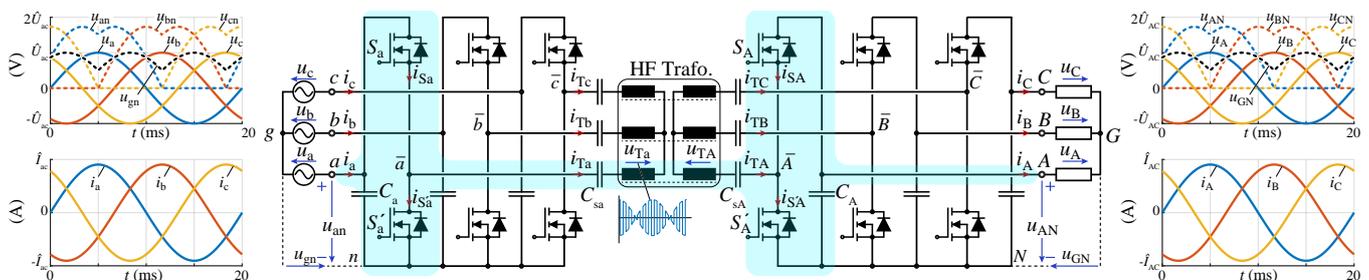


Fig. 1. Main power circuit and input / output terminal voltage / current waveforms of the proposed three-phase electronic transformer (3Φ -ET): Note that both, the input u_{an}, u_{bn}, u_{cn} and output stage voltages u_{AN}, u_{BN}, u_{CN} are strictly positive (unipolar) as they comprise a time-varying CM offset voltage on top of the sinusoidal grid voltages u_a, u_b, u_c (with a frequency f_{ac}) and u_A, u_B, u_C (with a frequency constrained to $f_{AC} = f_{ac}$), respectively. The DAB-type modulation of the input- and output-side converter switching stages results in inherently sinusoidal input i_a, i_b, i_c and output currents i_A, i_B, i_C .

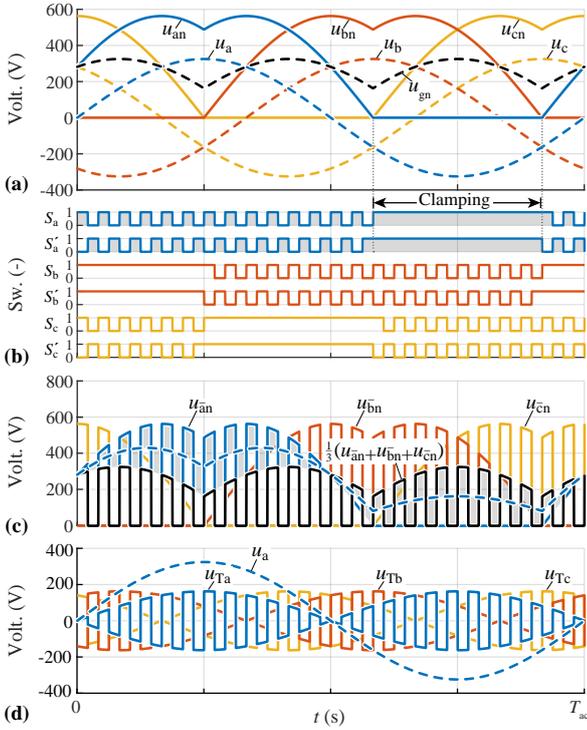


Fig. 2. Main waveforms of the 3Φ-ET primary-side converter stage during one grid period $T_{ac} = 1/f_{ac}$: (a) sinusoidal grid voltages u_a, u_b, u_c and strictly positive (unipolar) converter input voltages u_{an}, u_{bn}, u_{cn} comprising a CM offset voltage u_{gn} , (b) switching signals (for illustration purposes a low switching frequency $f_s = 24f_{ac}$ is selected), (c) switch-node voltages $u_{\bar{a}n}, u_{\bar{b}n}, u_{\bar{c}n}$ and the resulting CM voltage component equal to $\frac{1}{3}(u_{\bar{a}n} + u_{\bar{b}n} + u_{\bar{c}n})$ (the resulting LF and HF DM voltage in phase a is highlighted), and (d) resulting HF transformer voltages u_{Ta}, u_{Tb}, u_{Tc} .

II. CONVERTER BASICS

In this section, first, the operating principle, the modulation and the grid current formation of the proposed 3Φ-ET (see Fig 1) is discussed and, second, its power transfer characteristic is derived. Further, operation in an asymmetric three-phase grid is investigated and the impact of the input-output voltage amplitude ratio on the transistor stresses is assessed.

A. Modulation and Grid Current Formation

The power transistors of the primary-side converter stage require strictly positive input voltages u_{an}, u_{bn}, u_{cn} which is realized by introducing a common-mode (CM) offset voltage u_{gn} between the grid star point g and the input-stage reference potential n on top of the LF differential-mode (DM) grid input voltages u_a, u_b, u_c as illustrated in Fig. 2a for a grid period $T_{ac} = 1/f_{ac} = 20$ ms and a line-to-neutral amplitude $\hat{U}_{ac} = 325$ V. The half-bridges operate with a constant pulse-width modulation (PWM) duty-cycle of 50% (see Fig. 2b). Further, the phase with the instantaneously lowest grid phase voltage turns on simultaneously the high- and low-side transistor during one third of the grid period T_{ac} . In doing so, the input-stage reference potential n is always clamped to the most negative grid phase voltage and advantageously the CM offset voltage u_{gn} is strictly defined (i.e., u_{gn} cannot drift to higher voltage values, which would potentially result in critically high transistor blocking voltages) and the switching losses are reduced compared

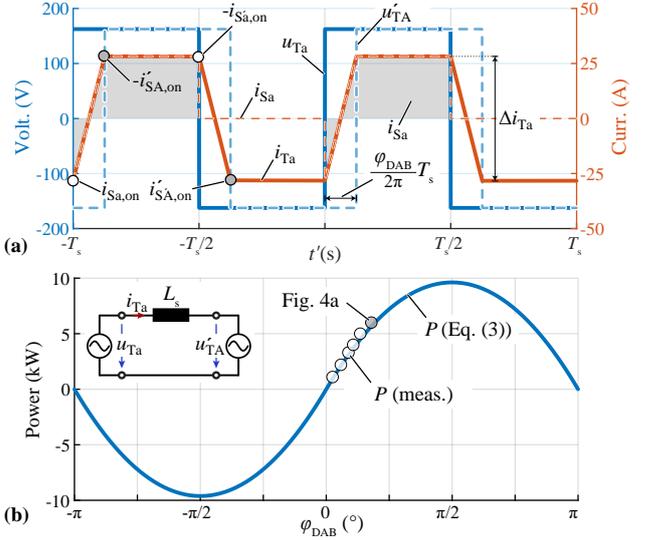


Fig. 3. (a) Primary-side-related single-phase equivalent circuit of phase a of the 3Φ-ET in Fig. 1 and relevant voltage and current waveforms during two switching periods for $t' = t - T_{ac}/4$. The difference of the transformer voltages u_{Ta}, u'_{Ta} is applied across the transformer leakage inductance L_s resulting in a trapezoidal transformer current i_{Ta} with the corresponding primary-side high-side transistor current i_{sa} (see Fig. 2) highlighted on top. The primary-side $i_{sa,on}, i'_{sa,on}$ and the primary-side-related secondary-side transistor turn-on currents $i_{SA,on}, i'_{SA,on}$ are indicated with circles and the transistor current directions in Fig. 1 are defined such that positive and negative turn-on currents correspond to hard- and soft-switching transitions, respectively. (b) Three-phase power flow P as a function of the PWM carrier phase-shift φ_{DAB} according to (3) with the maximum power flow resulting for $\varphi_{DAB} = \pm\pi/2$. The measured power flow of the system prototype in Sec. III is represented by scatter points which closely match the theoretical prediction.

to a modulation concept where all three half-bridges are continuously switched at HF.

The resulting switch-node voltages $u_{\bar{a}n}, u_{\bar{b}n}, u_{\bar{c}n}$ are presented in Fig. 2c and comprise CM and DM components at both, LF and HF. As in [23] the CM offset voltage u_{gn} is translated by the synchronous PWM switching pattern into a corresponding HF CM switch-node voltage which cannot drive any current in the open-starpoint transformer windings and is thus irrelevant for the power transfer. As the switch-node voltages comprise both, an HF and an LF DM voltage component, series capacitors C_{sa}, C_{sb}, C_{sc} are introduced to block the LF voltage component and/or to avoid saturation of the compact HFT. The series capacitors are sized based on the transformer leakage inductance L_s such that the series capacitor impedance is dominant at the grid frequency (i.e., $Z_{Cs}(f_{ac}) \gg Z_{Ls}(f_{ac})$) and blocks the LF voltage component, and negligible at the switching frequency f_s (i.e., $Z_{Cs}(f_s) \ll Z_{Ls}(f_s)$) to ensure an inductive HF power transfer. Accordingly, the resulting transformer voltages u_{Ta}, u_{Tb}, u_{Tc} in Fig. 2d toggle between \pm half of the respective grid input voltages, i.e., are grid-voltage amplitude-modulated.

B. Phase-Shift Power Flow Control

The primary-side-related single-phase equivalent circuit of phase a of the 3Φ-ET is presented in Fig 3. The difference of the primary-side u_{Ta} and the primary-side-

related secondary-side transformer voltage u'_{TA} is applied to the transformer leakage inductance L_s . For a high switching frequency $f_s \gg f_{ac}$ the grid voltages are approximately constant during one switching period $T_s = 1/f_s$ as highlighted for $t = T_{ac}/4$ in **Fig 3a** and thus the equivalent circuit resembles a dc-dc DAB converter [24]. Accordingly, the power flow can be regulated by means of a DAB-type modulation [3,24] where the secondary-side converter stage operates identical to the primary-side stage and employs a PWM carrier phase-shift $\varphi_{DAB} \in [-\pi, \pi]$. For the sake of simplicity a transformer turns ratio $n_1 : n_2 = 1 : 1$ (i.e., $u'_{TA} = u_{TA}$) and identical input and output grid voltage amplitudes (i.e., $\hat{U}_{ac} = \hat{U}_{AC}$ and $|u_{TA}| = |u_{TA}|$) are assumed for the following derivations. For the duration of the phase-shift interval $\frac{\varphi_{DAB}}{2\pi} T_s$ the primary- and secondary-side transformer voltages show opposing signs resulting in a peak-to-peak transformer current variation

$$\Delta I_{Ta}(t) = \frac{u_a(t) T_s}{2} \frac{\varphi_{DAB}}{L_s \pi} \propto u_a(t), \quad (1)$$

which is proportional to the instantaneous value of the grid voltage u_a . Subsequently, the transformer voltages u_{Ta} and u'_{TA} cancel out each other and the transformer current i_{Ta} remains constant for the remainder of the half-switching period $T_s/2$ resulting in the characteristic trapezoidal current shape.

Similar to a dc-dc DAB converter the phase-shift interval does not contribute to the active power transfer and the transformer current i_{Ta} is rectified by the input-stage high-side transistor S_a (see **Fig. 1, Fig. 3a**). The resulting LF grid current i_a is (when neglecting the LF charging current of the input stage capacitor C_a) equal to the high-side transistor switching frequency local-average current $\bar{i}_{Sa}(t)$ and i_a can be approximated as

$$i_a(t) \approx \bar{i}_{Sa}(t) = \frac{1}{2} \frac{\Delta I_{Ta}(t)}{2} \left(1 - \frac{\varphi_{DAB}}{\pi}\right) \propto u_a(t). \quad (2)$$

Thus, a constant PWM carrier phase-shift φ_{DAB} results in a naturally sinusoidal grid current i_a in phase with the grid voltage u_a . It is important to highlight that (2) only holds if $f_{AC} = f_{ac}$ and therefore the output frequency cannot be adjusted. However, it is worth noting that the converter output stage could be reconfigured as shown in [23] to generate an isolated dc-bus voltage instead of an isolated three-phase voltage system.

The grid current amplitude \hat{I}_{ac} and the three-phase power flow P from the input to the output is adjusted by means of the phase-shift φ_{DAB} , where $\varphi_{DAB} > 0$ corresponds to $P > 0$ and vice versa. The three-phase power flow P can be calculated considering (2) for $t = T_{ac}/4$ where $u_a = \hat{U}_{ac}$ and $i_a = \hat{I}_{ac}$ resulting to

$$P = \frac{3}{2} \hat{U}_{ac} \hat{I}_{ac} = \frac{3}{16} \hat{U}_{ac}^2 \frac{T_s}{L_s} \frac{\varphi_{DAB}}{\pi} \left(1 - \frac{\varphi_{DAB}}{\pi}\right). \quad (3)$$

The power characteristics $P(\varphi_{DAB})$ is depicted in **Fig. 3** and the maximum power flow results for $\varphi_{DAB} = \pm\pi/2$. Note that – similar to a dc-dc DAB converter – the marginal power increase $dP/d\varphi_{DAB}$ decreases towards $\varphi_{DAB} = \pm\pi/2$ and results in high transformer current stresses such that typically nominal-power phase-shift values φ_{DAB} of $\pi/6$ to $\pi/4$ are selected. As any DAB-type converter, the 3 Φ -ET shows

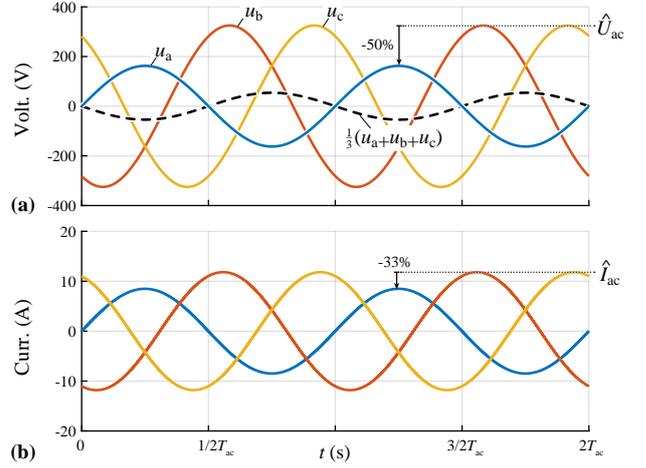


Fig. 4. Simulated 3 Φ -ET waveforms considering the specifications of the experimental prototype system in **Sec. III** for an unbalanced grid where the input voltage of phase a shows only half the line-to-neutral amplitude of phases b and c : (a) grid input voltages u_a, u_b, u_c and the CM voltage component, and (b) grid input currents i_a, i_b, i_c which sum to zero in the open grid starpoint g .

buck-boost capability and the power transfer characteristics for a generic input-output voltage amplitude ratio $\hat{U}_{AC}/\hat{U}_{ac}$ and transformer turns ratio $n_1 : n_2$ can be derived following the same calculation steps as

$$P = \frac{3}{16} \hat{U}_{ac} \left(\hat{U}_{AC} \frac{n_1}{n_2}\right) \frac{T_s}{L_s} \frac{\varphi_{DAB}}{\pi} \left(1 - \frac{\varphi_{DAB}}{\pi}\right). \quad (4)$$

C. Operation in Unbalanced Grids

Thus far, an ideally symmetric three-phase grid was assumed at the input of the 3 Φ -ET. However, in reality grid asymmetries may occur and this section therefore qualitatively assesses the impact on the converter operation. **Fig. 4** depicts simulated 3 Φ -ET waveforms (PLECS) where the input voltage of phase a shows only half the line-to-neutral amplitude of phases b and c (i.e., $\max(u_a) = k \cdot \hat{U}_{ac}$ with $k = 0.5$). Note that this imbalance causes the grid voltages to comprise a CM voltage component $1/3(1-k)\hat{U}_{ac}$ with respect to the grid starpoint g which cannot drive any current in the open-starpoint system such that the resulting current in phase a is impacted by the DM imbalance voltage component $2/3(1-k)\hat{U}_{ac}$ only, and is thus reduced by $\approx 33\%$. As can be observed in **Fig. 4b** the grid currents remain sinusoidal and are slightly phase-shifted with respect to the corresponding grid voltages such that the currents sum to zero in the grid starpoint g . Naturally sinusoidal grid currents are maintained and therefore the 3 Φ -ET can also safely operate in unbalanced-grid conditions.

D. Transistor Turn-on Currents and Voltages

The transistor turn-on currents and voltages have a great impact on the converter switching losses and the phase a transistor currents $i_{Sa,on}, i'_{Sa,on}$ and $i_{SA,on}, i'_{SA,on}$ in **Fig. 1** are defined such that positive and negative turn-on currents corresponds to hard- and soft-switching transitions, respectively. The resulting transistor turn-on currents within a switching period T_s are indicated in **Fig. 3a** and correspond to full soft switching operation.

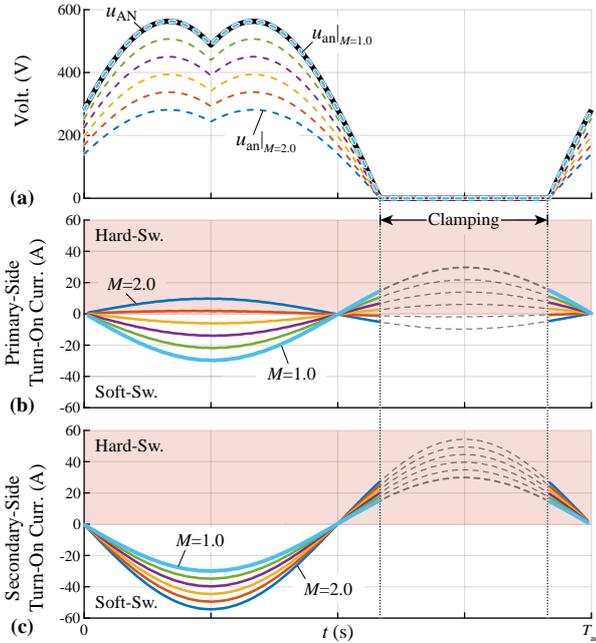


Fig. 5. Impact of the input-output voltage amplitude ratio $M = \hat{U}_{AC}/\hat{U}_{ac}$ (for a constant output voltage amplitude $\hat{U}_{AC} = 325$ V and a PWM carrier phase-shift $\varphi_{DAB} = \pi/6$) on the transistor turn-on currents of phase a during one grid period T_{ac} considering the specifications of the experimental prototype system in **Sec. III** with a unity transformer turns ratio: (a) Converter input u_{an} and output voltage u_{AN} , (b) primary-side transistor turn-on currents $i_{S_{a,on}} = i'_{S'_{a,on}}$, and (c) secondary-side transistor turn-on currents $i_{S_{a,on}} = i'_{S'_{a,on}}$. Note that the transistor current directions in **Fig. 1** are defined such that positive and negative turn-on currents correspond to hard- and soft-switching transitions, respectively.

Fig. 5 further provides a detailed analysis on the impact of the input-output voltage amplitude ratio, i.e.,

$$M = \hat{U}_{AC}/\hat{U}_{ac}, \quad (5)$$

on the transistor turn-on currents of phase a during one grid period T_{ac} . Here, the output voltage amplitude $\hat{U}_{AC} = 325$ V is kept constant and, starting from $M = 1.0$, the input amplitude \hat{U}_{ac} is gradually reduced. The specifications of the experimental prototype system in **Sec. III** (with a unity transformer turns ratio) are considered and the PWM carrier phase-shift $\varphi_{DAB} = \pi/6$ is kept constant such that lower values of M correspond to lower three-phase output power values P according to (4).

As can be observed in **Fig. 5b,c** the primary-side and the secondary-side turn-on currents are identical for $M = 1.0$ and full soft switching results in the positive grid half period. In contrast, hard-switching transitions occur in the negative grid half period. However, as all transistors of phase a cease switching during the $T_{ac}/3$ clamping interval (and do not cause any switching losses), the hard-switching time in the negative grid half period is limited to $T_{ac}/6$ where advantageously the hard-turn-on currents and the switched voltages (defined by the input- u_{an} and the output-stage voltage u_{AN} highlighted in **Fig. 5a**) are low compared to the corresponding values in the positive grid half period.

With decreasing input amplitudes \hat{U}_{ac} (and thus $M > 1.0$), the primary- and secondary-side turn-on currents are no longer identical: The primary-side turn-on currents in **Fig. 5b** decrease in amplitude during the positive grid

TABLE I: PROTOTYPE SPECIFICATIONS.

| Designator | Description | Value |
|-----------------|----------------------------------|-----------------|
| U_{ac} | Grid voltage (rms, line-neutral) | 230/115 V |
| f_{ac} | Grid frequency | 50 Hz |
| P_{ac} | Nominal system power | 3×2 kW |
| I_{ac} | Nominal grid current (rms) | 8.7 A |
| f_s | Switching frequency | 72 kHz |
| φ_{DAB} | Nominal DAB phase-shift | $\pi/6$ |
| $n_1:n_2$ | Transformer turns ratio | 1:1 |
| L_s | Transformer leakage ind. | 7.2 μ H |
| C_s | Series capacitor | 6.8 μ F |

half period and reverse sign for $M > 1.6$ such that hard-switching transitions with elevated switching losses result. Conversely, the secondary-side turn-on currents in **Fig. 5c** are pushed to more negative values and soft switching during the positive grid half period is maintained in this converter stage. Note that the same trend occurs for $M < 1.0$ and thus the 3Φ -ET is – similar to a dc-dc DAB converter – preferably operated with limited step-up or -down ratios $M \in [0.7, 1.6]$, and ideally large conversion ratios are realized by means of a suitable transformer turns ratio $n_1 : n_2$.

III. EXPERIMENTAL VERIFICATION

To verify the operating principle of the proposed 3Φ -ET, most importantly the naturally sinusoidal grid currents and the DAB-type power transfer characteristics, a 6 kW proof-of-concept hardware demonstrator according to the specifications in **Tab. I** is constructed. Aiming at operation in the European 400 V_{rms} three-phase mains, a power transistor blocking voltage requirement $\sqrt{3}\hat{U}_{ac} = 565$ V is considered and thus 900 V SiC MOSFETs from Cree (C3M0010090K) with sufficient blocking voltage margin are employed. Advantageously, the half-bridge arrangement of the power transistors allows to use the same layout considerations as for a dc-dc DAB converter [24]. A switching frequency $f_s = 72$ kHz is selected such that advantageously the second switching-frequency harmonics are not yet in the regulated electromagnetic interference (EMI) band starting at 150 kHz. Note that the aim of this paper is to verify the operating principle of the 3Φ -ET and thus only the core converter depicted in **Fig. 1** is built where the input capacitors (C_a in phase a) serve as the first EMI filter elements. Additional HF attenuation is required to comply with the relevant EMI emission standards and the authors refer to Ref. [25] for the design of the additional grid-side filter stages.

The transformer is realized with three two-port single-phase HFTs connected to a common starpoint for both the primary- and secondary-side converter stage and it is important to highlight that alternatively also a monolithic three-phase HFT could be employed. Each phase transformer is designed such that its leakage inductance results to $L_s = 7.2 \mu$ H resulting in a $P = 6$ kW power transfer according to (3) for the nominal PWM carrier phase-shift $\varphi_{DAB} = \pi/6$.

The system is operated with a resistive three-phase load connected to the output terminals and **Fig. 6a** shows experimental nominal-power operation waveforms for identical input-output grid voltage levels ($\hat{U}_{ac} = \hat{U}_{AC}$; $M = 1.0$) and a sinusoidal grid current i_a in phase with the respective

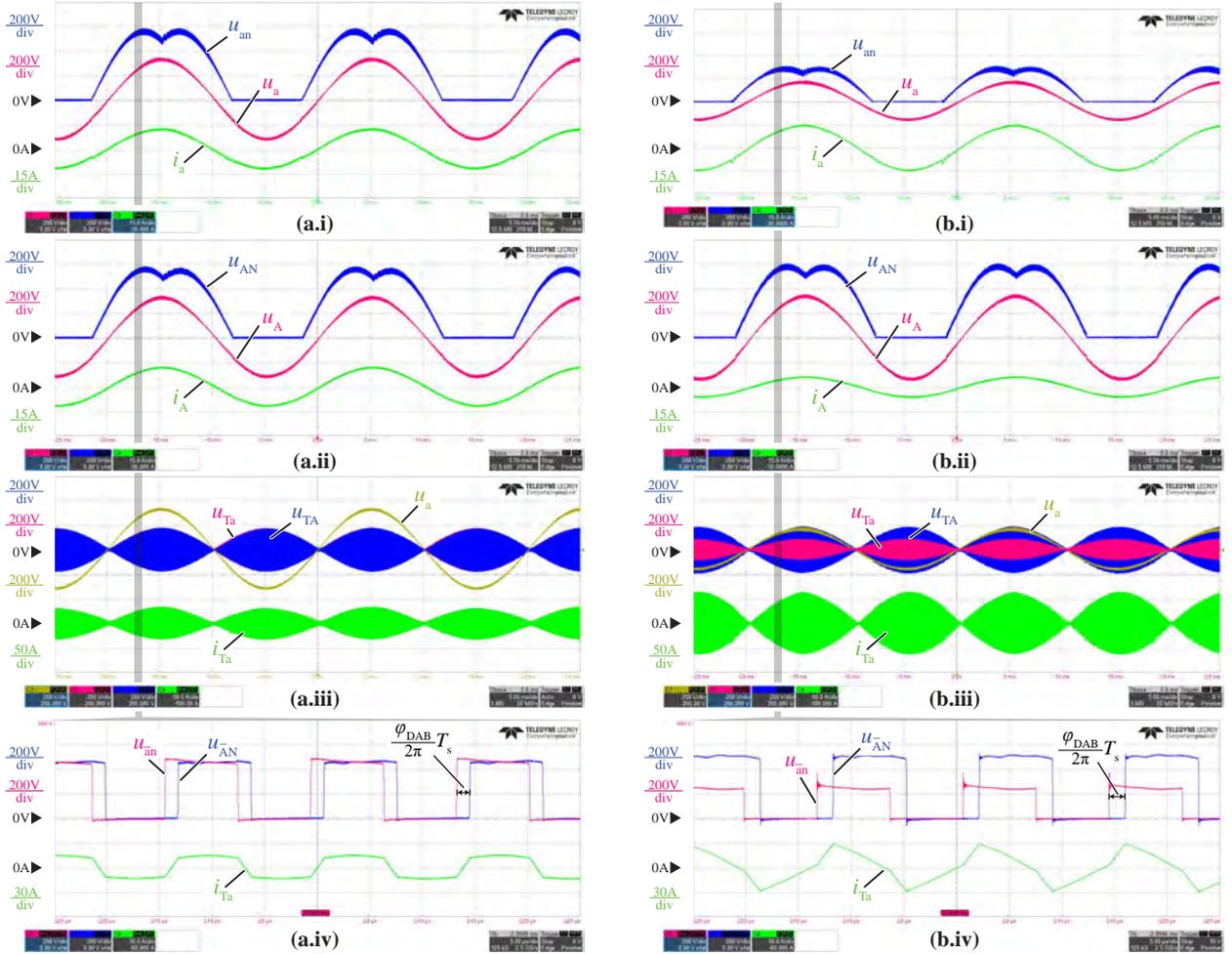


Fig. 6. Experimental waveforms for the considered specifications in **Tab. I** with an output voltage of 230 V (rms, line-neutral) generated from an input voltage of (a) 230 V and (b) 115 V: (x.i) converter primary-side phase a grid u_a and input capacitor voltage u_{an} , and sinusoidal input current i_a , (x.ii) converter secondary-side phase A grid u_A and output capacitor voltage u_{AN} , and sinusoidal output current i_A . (x.iii) phase a grid input u_a voltage, transformer primary- u_{TA} and secondary-side voltage u_{TA} , and the corresponding transformer i_{TA} within one grid period T_{ac} , and (x.iv) zoom in on the switching-frequency waveforms of (c) for a grid angle $\omega_{act} \approx 60^\circ$ (with reference to the zero crossing of u_a)

grid voltage u_a can be observed. The clamping of the instantaneously most negative grid phase is determined by means of a phase-locked loop and does not cause any transient overvoltages. The measured three-phase power flow P for several values of φ_{DAB} is represented by scatter points in **Fig. 3** which closely match the theoretical prediction from (3) with small deviations explained by the impact of the deadtime and the non-zero switching-frequency impedance of the series capacitors. Further, a zoom-in on the primary-side switch-node voltages is provided, where the PWM carrier phase-shift and the resulting characteristic trapezoidal transformer current i_{TA} (resulting in fully soft-switched operation) can be observed.

As any DAB-type converter, the system shows buck-boost capability and **Fig. 6b** further presents experimental waveforms for half-nominal power operation with an output voltage of $U_{AC} = 230 \text{ V}_{\text{rms}}$ (line-neutral) generated from an input voltage of $U_{ac} = 115 \text{ V}_{\text{rms}}$ only ($M = 2.0$). As predicted in **Sec. II-D** the converter primary-side stage loses soft-switching for the high step-up ratio $M = 2.0$ and a hard-switching transition with high du/dt and associated switch-node voltage ringing can be observed in **Fig. 6b.iv**.

Further, the primary-side and secondary-side transformer voltages do no longer cancel out each other after the phase-shift interval and thus higher transformer current variations and conduction stresses result. Thus, for an application where the nominal operating point requires a step-up ratio $M = 2.0$ selecting a transformer turns ratio $n_1 : n_2 = 1 : 2$ allows to optimize the 3 Φ -ET performance. Alternatively, a reconfigurable transformer with a tap changer allowing to, e.g., adjust the primary-side turns number enables high-performance operation in a wide input-output voltage range [26].

IV. CONCLUSION

Solid-state / electronic transformers enable galvanic isolation and voltage level adaption at HF and thus the magnetic core volume and weight can be reduced substantially compared to traditional transformers operating at the grid frequency. This paper introduces a novel phase-modular single-stage three-phase electronic transformer (3 Φ -ET) which advantageously enables the use of standard power transistors with unipolar voltage blocking capability in a half-bridge configuration. The 3 Φ -ET operates with a simple carrier

phase-shift / DAB-type modulation with natural sinusoidal grid currents and bidirectional power flow. The 3Φ -ET modulation and power transfer characteristics are systematically derived and experimentally verified by means of a 6kW prototype system operating with a wide input voltage range.

Future research may focus on aspects of the practical realization of an industrial 3Φ -ET system such as design guidelines and/or the identification of optimal converter designs by means of a comprehensive multi-objective optimization, as well as a comparison to the performance limits of alternative topology concepts. As the operation of the 3Φ -ET phase modules is very similar to a standard dc-dc DAB converter (with high reported efficiency and power density values of $\approx 98\%$ and up to $10\text{kW}/\text{dm}^3$, respectively [27,28]) similar performance metrics can be expected for the 3Φ -ET, where the twice-grid-frequency power variation in each module may lead to a slight performance derating compared to a dc-dc DAB converter.

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