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***Abstract*—Fast charging of electric vehicles (EVs) requires isolated AC/DC converters with a wide output voltage range of 200 V to 1000 V. Combining a three-level Vienna Rectifier (VR) with four isolated Dual-Active-Bridge DC/DC Converter (DABC) modules and latest-generation 600 V GaN technology enables very high switching frequencies of 560 kHz for the VR and up to 330 kHz for the DABCs. Hence, in this paper an ultra-compact realization of a 10 kW EV charger module with a power density of 9 kW/dm^3 (about 150 W/in^3), not including the coldplate, is presented. In this context, a simplified DABC modulation method and straightforward yet accurate (confirmed by experiments) loss models for the DABCs and the VR are introduced, which facilitate a thorough investigation of the optimum synergetic operation of the two stages: For the considered converter, changing the VR operating mode from conventional 3/3-PWM (where the two stages operate rather independently and hence all three VR bridge-legs operate with PWM) to 1/3-PWM (where the DABCs shape the voltage of the shared intermediate DC-link such that always only one of the VR's three bridge-legs must operate with PWM) results in an advantageous efficiency improvement of up to about 2% over a large part of the output voltage and power range, and in a peak efficiency of more than 97%. Further, the synergetic operation of the two-stage system (VR and DABCs) is experimentally verified for the first time, confirming the modeling results and the efficiency advantage of 1/3-PWM (i.e., 95.4% vs. 95.1% at the rated load of 10 kW and with 500 V output voltage). Conducted EMI pre-compliance measurements indicate that the change of the operating strategy from 3/3-PWM to 1/3-PWM only requires minor changes of the EMI filter design.**

I. Introduction

OVER the past decade, electric vehicle (EV) sales have grown significantly [1]. For example, since 2019, the share of EVs among global car sales has risen by a factor of four to almost 10% in 2021 [2]. This trend can be expected to continue, given worldwide government policies that subsidize the adoption of electric mobility (e.g., the U.S. government targets a 50% EV market share by 2030 [3]). With the increasing fleet of EVs, a corresponding need to scale the charging infrastructure emerges. Certain market studies estimate that in the U.S. alone, 1.2 million public and 28 million private EV chargers will be required by 2030 [4].

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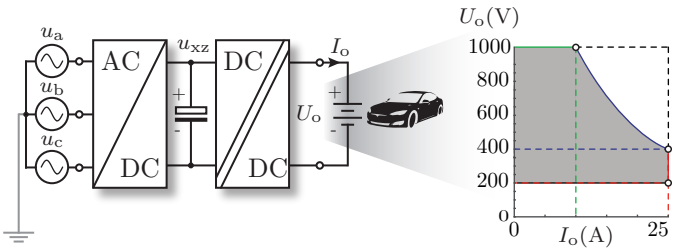

Fig. 1. Block diagram of a typical two-stage EV charger with a three-phase AC/DC PFC rectifier front-end and a downstream isolated DC/DC converter, and the output voltage, U_o, and output current, I_o, range of the considered 10 kW system.

The general functionality of an EV charger is to transfer power from a single- or three-phase AC mains to the EV battery, which has DC voltage ratings of typically 400 V or, especially if higher charging powers are desired [5], 800 V. Depending on where they are installed, EV battery chargers can be classified as either on-board or off-board chargers [6]. On-board chargers feature an AC input, and standards such as IEC 62196 or SAE J1772 define charging power levels in the range of 3 kW to 22 kW, depending also on whether a single- or three-phase mains is available. Fast charging of comparably large EV batteries requires much higher power ratings, however, which are realized with stationary charging stations and a DC interface to the EV. Then, for example, the CHAdeMo standard allows power levels of up to 400 kW at 1000 V DC [7], [8] (note that even higher voltage and current ratings of up to 1250 V DC and 3000 A are envisioned for the future [9], e.g., targeting electric trucks). To ensure compatibility with a wide range of EV batteries, such stationary fast-charging stations should feature a wide output voltage range of typically 200 V to 1000 V. **Fig. 1** shows the output voltage, current, and power ranges of the exemplary three-phase 10 kW charger that we consider in this paper. The unit could be employed as an on-board charger, where the achieved high compactness is beneficial, or several units could be operated in parallel to realize a high-power fast-charging station.

Fig. 1 further shows the typical block diagram of an EV charger: there is a power-factor-correcting (PFC) AC/DC rectifier stage, an intermediate DC bus, and an isolated DC/DC converter [7], [8], [10] that provides galvanic separation to ensure user safety and contributes to covering the wide output

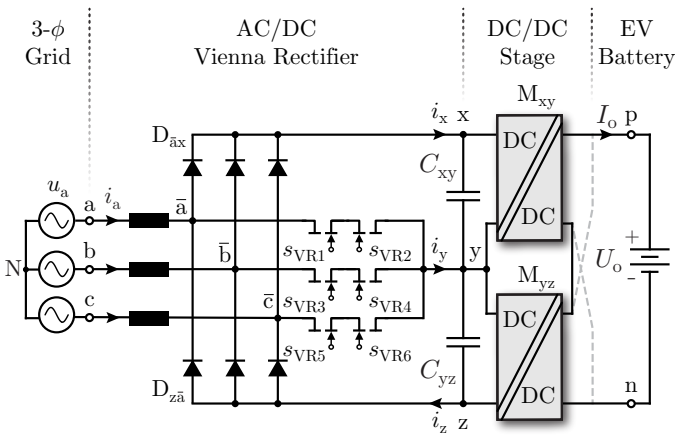

Fig. 2. Conceptual power circuit of the considered EV charger, where the AC/DC PFC rectifier is realized as a Vienna Rectifier (VR) and two isolated DC/DC converter stages, realized as Dual Active Bridge Converters (DABCs), are employed. As indicated by the dashed lines, the DABC modules' outputs could be reconfigured into a parallel connection to increase the available output current and hence power at low output voltages.

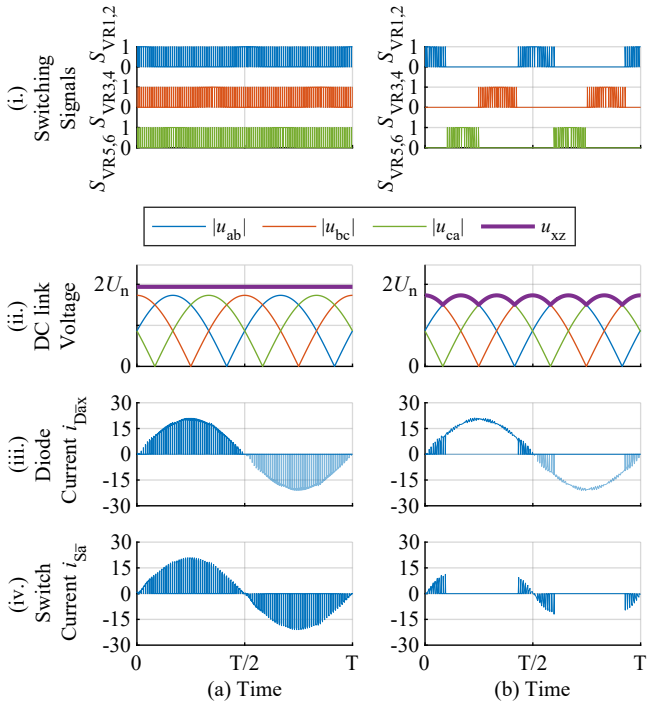

Fig. 3. Simulated waveforms of the VR operating with **(a)** 3/3-PWM and **(b)** 1/3-PWM (note the six-pulse shape of the intermediate DC-link voltage u_{xz}, which is controlled by the DC/DC converters to impress currents in two of the mains phases). **(i)** Switch gate signals, **(ii)** DC-link voltage u_{xz}, **(iii)** diode current of phase a, **(iv)** switch current of phase a

voltage range [11] (this is necessary as, e.g., a typical boost-type PFC rectifier operating from a 400 V line-to-line mains can not generate a DC voltage below about 650 V if some control margin is taken into account [12]). Even though non-isolated EV chargers are being considered as an alternative that could possibly facilitate higher efficiency and compactness [13], the two-stage approach with galvanic separation still is the most widely employed solution, not least because of electrical safety considerations.

Literature discusses a wide variety of converter topologies for the realization of the AC/DC PFC rectifier and the isolated DC/DC converter stages of EV chargers [7], [8], [10]. Aiming for a very compact realization, we select a Vienna Rectifier (VR) [14] front-end (see **Fig. 2**), which advantageously can be realized using latest-generation 600 V GaN transistors and 1200 V SiC diodes. The thus enabled high switching frequency and the three-level characteristic of the VR facilitate a very compact realization of the boost inductors and the EMI filter stages. Note that bidirectional power flow could be achieved by replacing the diodes with transistors. The split intermediate DC-link of the VR is then used as input for the subsequent stage realizing the galvanic separation with two stacked DC/DC converter modules, which therefore also can be realized with 600 V GaN technology. Again, many different realization options exist (e.g., phase-shifted full bridges, LLC or CLLC resonant converters, etc. [8]), but Dual-Active-Bridge Converters (DABCs), advantageously, have the ability to operate with a wide range of voltage conversion ratios [11] and provide very high control dynamics.

For simplicity reasons, the rectifier and the DC/DC converter stage are often operated rather independently, as typically the intermediate DC-link is realized with large electrolytic capacitors that serve to decouple the control of both stages. Thus the voltage u_{xz} (see **Fig. 2**) is usually constant for a given operating point. The PFC rectifier stage ensures sinusoidal input currents and at the same time regulates u_{xz} to a fixed voltage $u_{xz} = U_{xz}$. In particular, this implies that all three bridge-legs of the three-phase AC/DC front-end must continuously operate with PWM (3/3-PWM; for the sake of clarity discontinuous modulation schemes [15] are not considered in this paper) as indicated in **Fig. 3a**. The DC/DC converter stage then draws power from the intermediate DC-link capacitor and delivers the power to the output port of the converter, while regulating the output voltage, U_o, to the desired value. In order to reduce the required range of the DC/DC stage's voltage transfer ratios (which typically leads to more favorable design trade-offs), it is advantageous to adapt U_{xz} depending on the output voltage. The upper limit for U_{xz} is given by the permissible blocking voltage of the power semiconductors and the selected DC-link capacitors, and the lower limit follows from the grid voltage (i.e., the peak line-to-line voltage plus a certain margin; for a 400 V grid, $U_{xz} \geq 640$ V follows [12]). Of course, for each operating point (i.e., combination of output voltage and output power), there is an optimum value of U_{xz} that minimizes the combined losses of the VR and the DC/DC converter stage, as will be addressed in detail later.

It seems now sensible to think of ways in which the operation of the two converter stages could be further integrated, such that ultimately minimum overall losses could be achieved. A first such option [16]–[19] (based on [20]) reduces the functionality of the AC/DC front-end to that of a three-phase unfolder; there is no high-frequency (HF) switching of the VR semiconductors and consequently near-zero switching losses. The two DC/DC converters then generate time-varying voltages u_{xy} and u_{yz} and thus ultimately ensure sinusoidal grid currents *and* regulate the output voltage. Whereas these solutions advantageously

completely avoid HF switching of the VR unfolder and do not require AC-side boost inductors, the intermediate DC bus voltages u_{xy} and u_{yz} are varying widely, and, in particular, reach 0 V three times per grid period—and thus so does the power processed by each of the two DC/DC converters, i.e., their utilization is relatively low. Furthermore, the blocking voltage stress on the power transistors increases and a blocking capability of 600 V would no longer provide sufficient margin.

For arbitrary three-phase boost-type rectifier front-ends (not only for VRs), it is well known that discontinuous PWM (DPWM) methods [21], [22] require HF switching of each bridge-leg only during 2/3 of the mains period, lowering switching losses accordingly. Furthermore, the intermediate DC voltage U_{xz} could be lowered to the minimum possible but still constant value, i.e., the peak value of the line-to-line voltages [12]. However, for the considered three-level VR front-end, such DPWM schemes result in a relatively large midpoint current, i_y [23]. Thus, either bulky electrolytic capacitors would be required, or the two DC/DC converters would need to compensate a relatively large power mismatch.

Instead, by using the DC/DC converter to shape u_{xz} into the six-pulse envelope of the line-to-line voltage absolute values, i.e., $u_{xz} = \max(|u_a|, |u_b|, |u_c|)$ as indicated in **Fig. 3b**,[1] the currents in the two phases with the highest and the lowest instantaneous voltage, respectively, can be controlled as the corresponding diodes are conducting (or, in bidirectional realizations, the corresponding anti-parallel transistors are permanently conducting). Accordingly, only the third phase current needs to be shaped by PWM of the corresponding AC/DC-stage bridge-leg. Advantageously, this phase (for PFC operation with near unity power factor) always carries the current with the lowest absolute value. Thus, each front-end bridge-leg only operates with PWM during 1/3 of the mains period (1/3-PWM) where also the switched currents are low [24], [25]. Therefore, 1/3-PWM significantly reduces the switching losses of the AC/DC rectifier stage. Originally proposed in 2005, [24], [25], the concept has been further analyzed in [26], [27], and [28] has pointed out the close relationship to the integrated active filter (IAF) [29] topology. Furthermore, [12] provides a detailed comparison with 2/3-PWM (DPWM), and [30], [31] analyze the behavior under irregular grid conditions, [32] employs a delta-switch front-end converter, and [33] details a generalized carrier-based modulation implementation. Whereas the former references all discuss non-isolated systems, i.e., with non-isolated DC/DC converter stages, the same advantageous reduction of the front-end stage's switching losses can be achieved with isolated DC/DC stages shaping the intermediate DC-link voltage u_{xy} accordingly [34]–[36].

Finally, 1/3-PWM can also be implemented in three-level AC/DC rectifier stages whose split intermediate DC-link is connected to two stacked isolated DC/DC converters, as initially mentioned in [34] using a three-level NPC front-end and three-phase PWM-operated DC/DC converters. The direct precursor to the analysis presented in the following is [37], which details the 1/3-PWM concept for an EV charger module consisting of a VR and two generic DC/DC converter stages. As an aside, note that also non-isolated DC/DC converters could be employed. In that case, only the ratio of the required output voltage to the grid line-to-line voltage amplitude decides whether the DC/DC stage must operate; if it does, it is always advantageous to operate it in a way that allows 1/3-PWM for the rectifier stage, i.e., for each operating point there is a clearly defined optimum operating mode of the two converter stages [38], [39]. This is

[1]Note that this is essentially an approximation that neglects the (mains-frequency) voltage drop across the boost inductors, which, however, is very low especially if high VR switching frequencies and hence small boost inductors with a low inductance value are used.

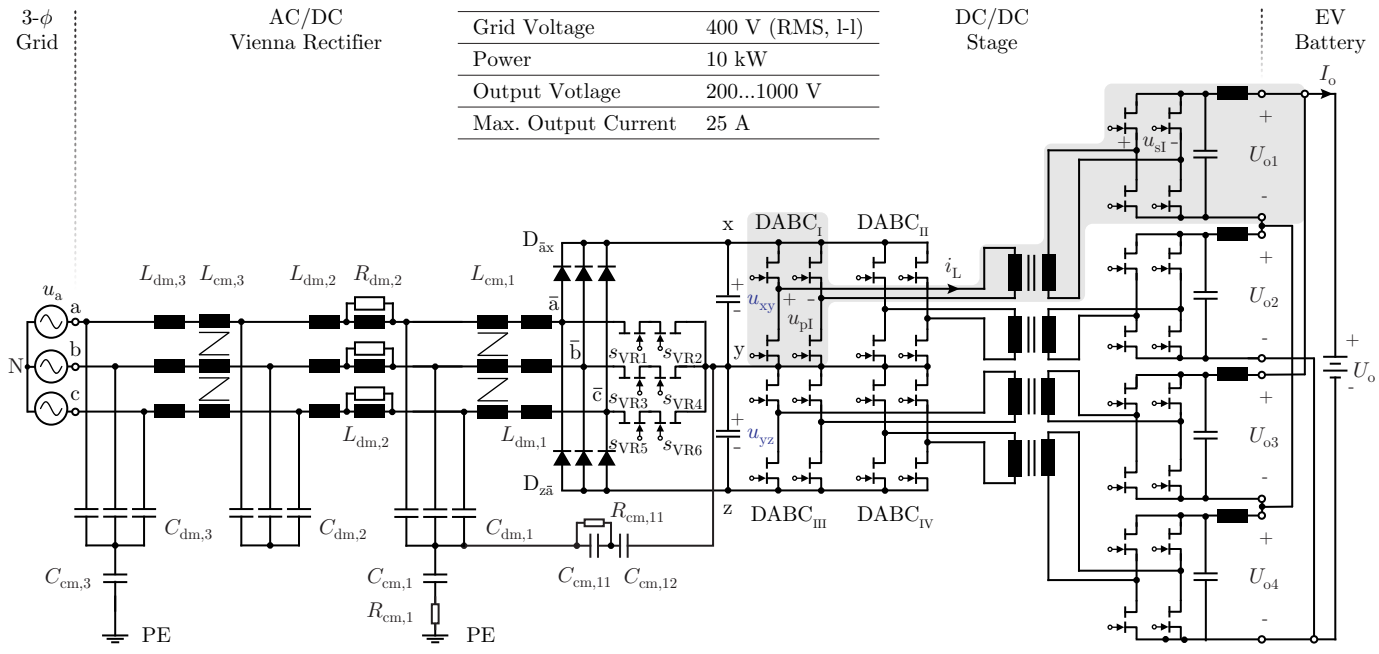

Fig. 4. Full schematics of the considered two-stage EV charger hardware prototype, including an EMI filter, the VR front-end, and four DABC modules.

different in the cases considered in [37] and here, where the isolated DC/DC converter stage necessarily *always* operates and hence a system-level efficiency analysis must be employed to identify the optimum operating mode for a given operating point. However, [37] did not include a quantitative analysis of the optimum operating mode selection (3/3-PWM, 1/3-PWM) considering the VR front-end *and* the DC/DC converters, nor an experimental analysis.

Therefore, the optimal operation and experimental verification of a 1/3-PWM VR in combination with isolated DC/DC converter stages is analyzed in this paper, considering an exemplary three-phase 10 kW ultra-compact EV charger module with a wide output voltage range of 200 V to 1000 V. As a detailed overview of the considered system is needed for the discussions in later parts of the paper (whose focus, after all, is not on the hardware design but on the different operating modes of a given hardware), we choose the somewhat unorthodox approach of first introducing some details of the realized 10 kW two-stage hardware demonstrator in **Section II**. Then, based on straightforward but sufficiently accurate loss models (confirmed by experiments) for the GaN-based VR introduced in **Section III** and for the DAB DC/DC converter modules in **Section IV**, we provide a comprehensive performance evaluation of the two-stage system in **Section V**. For each operating point, the analysis quantifies the achievable system-level efficiency improvement (if any) for a change of the operating strategy from the baseline 3/3-PWM to 1/3-PWM. Then, **Section VI** discusses control implementation details of the two-stage system and provides experimental verification for typical operating points, including also a brief discussion of the EMI performance, which confirms that a change of the operating strategy from 3/3-PWM to 1/3-PWM has no significant impact on the EMI filter design.

II. Demonstrator System Overview

Whereas a theoretical analysis of the VR loss reduction achieved by 1/3-PWM compared to 3/3-PWM can be carried out by assuming arbitrary (ideal) DC/DC converters (see [37] and a brief summary in **Section III**), this perspective is incomplete as the losses of actual DC/DC converters depend on the operating point and in particular on u_{xz}. Therefore, specific realizations of the VR front-end *and* the DC/DC converter stages must be considered to analyze the system-level optimum operating modes over the output voltage and power ranges.

Fig. 4 shows the power circuit schematic, including an EMI filter for compliance with CISPR 11 Class A, of the thus considered 10 kW two-stage EV charger system, an early prototype version of which has been mentioned in [40]. Note that each of the two DC/DC converters is realized with *two* DABCs, each rated at 2.5 kW. This, first, facilitates an ultra-flat realization and increases the DABC transformer surface area that can be attached to the coldplate, and, second, would enable improved part-load efficiency by only operating two instead of all four DABCs. Note further that the DABC modules are configured in a cross-wise input-parallel, output-series (IPOS, e.g., DABC_I and DABC_II) and input-series, output-parallel (ISOP; e.g., DABC_I and DABC_III) structure, thus utilizing the known natural balancing properties of IPOS and ISOP arrangements [41] to ensure balanced intermediate DC-link voltages.

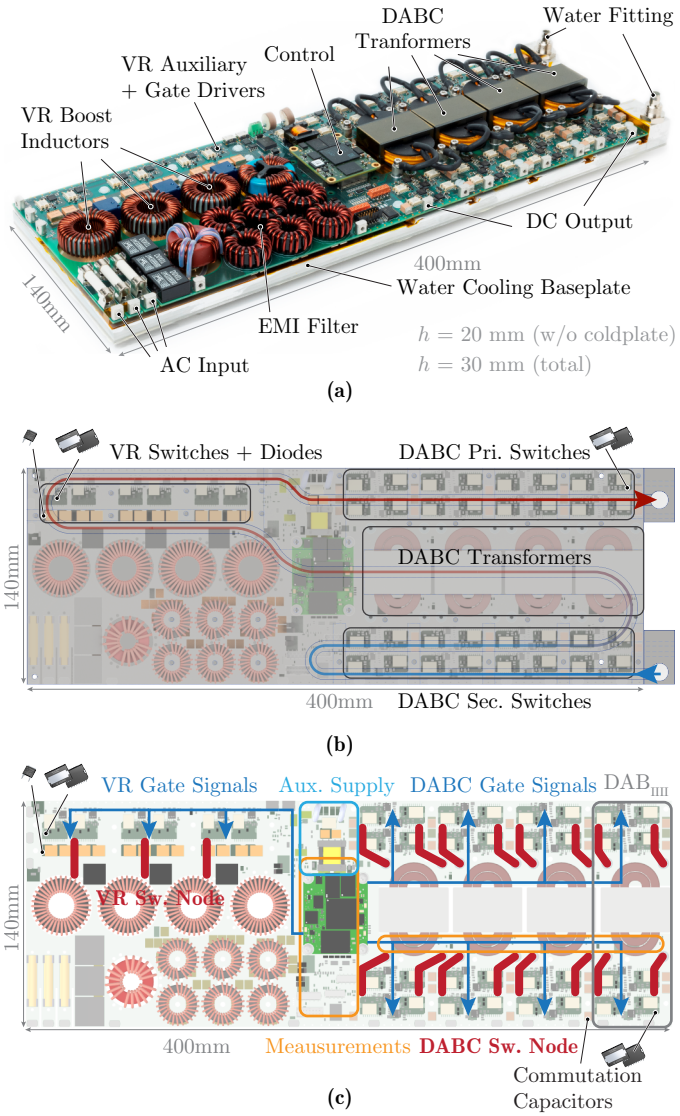

Fig. 5. (a) Photograph of the considered realized 10 kW three-phase two-stage VR and DABC hardware prototype. The overall dimensions of 400 mm × 140 mm × 20 mm (not including the non-optimized coldplate) yield a power density of around 9 kW/dm^3 or about 150 W/in^3. **(b)** Coldplate with the 7 mm × 4.3 mm water channel passing underneath the 38 GaN switches, the 12 SiC Schottky diodes, and the 4 DABC transformers. **(c)** Overview of key aspects of the PCB layout; the whole converter is realized on a single PCB.

Fig. 5 shows a photo of the realized system, and **Tab. I** summarizes its main components. The high switching frequency ($f_{\text{sw,VR}}$ = 560 kHz) of the VR and the ultra-flat realization (overall dimensions of 400 mm × 140 mm × 20 mm, not including the coldplate) result in a comparably high power density of around 9 kW/dm^3 (or about 150 W/in^3). The system is liquid-cooled and the non-optimized and thus 10 mm thick coldplate[2] increases the volume by about 30%, corresponding to a power density reduction to about 6 kW/dm^3 (or 98 W/in^3). As shown in **Fig. 5b**, the water channel is shaped to cool all the

[2]As shown in [42], the thickness of the coldplate could be be cut in half, i.e., reduced to about 5 mm without impairing the cooling properties.

TABLE I
MAIN COMPONENTS OF THE 10 KW EV CHARGER MODULE (SEE **FIG. 4**).

Parameter	Value
EMI Filter	
Boost Ind. $L_{dm,1}$	36 µH, Magnetics Molypermalloy Powder (MPP), 55550 core, 36 turns, 1.4 mm wire
CM Ind. $L_{cm,1}$	320 µH, TDK N87, R34 (B64290L0058X087), 12 turns per winding, 1.4 mm wire
DM Cap. $C_{dm,1}$	560 nF (10x56 nF X2 rated)
CM Cap. $C_{cm,1}$	18.8 nF (4x4.7 nF Y2 rated)
CM Resistor $R_{cm,1}$	22 Ω
CM Cap. $C_{cm,11}$	220 nF
CM Resistor. $R_{cm,11}$	47 Ω
CM Cap. $C_{cm,12}$	220 nF
DM Ind. $L_{dm,2}$	16.5 µH, Kool Mµ MAX Toroids (79351), 18 turns, 1.8 mm wire
DM Resistor. $R_{dm,2}$	47 Ω
DM Cap. $C_{dm,2}$	336 nF (6x56 nF X2 rated)
CM Ind. $L_{cm,2}$	560 µH, VAC Nanocrystalline VITROPERM cores T60006-L2025-W380, 6 turns per winding, 1.8 mm wire
DM Ind. $L_{dm,3}$	6.8 µH, shielded wirewound inductor (Würth 7443556680)
DM Cap. $C_{dm,3}$	224 nF (4x56 nF X2 rated)
CM Cap. $C_{cm,3}$	9.4 nF (2x4.7 nF Y2 rated)
Vienna Rectifier Stage	
Boost Ind. L	36 µH, Magnetics Molypermalloy Powder (MPP), 55550 core, 36 turns, 1.4 mm wire
Switches	600 V, 70 $m\Omega_{max}$ / 55 $m\Omega_{typ}$ CoolGaN™ IGOT60R070D1
Diodes	1200 V SiC Schottky CoolSiC™ IDM10G120C5 (2 in parallel)
Gate Drivers	EiceDRIVER™ 1EDF5673K
Sw. Freq. $f_{sw,VR}$	560 kHz
DC Cap. C_{xy}, C_{xy}	28 µF
Dual Active Bridge Converter Stage	
Switches (Pri. & Sec.)	600 V, 42 $m\Omega_{max}$ / 37 $m\Omega_{typ}$ CoolGaN™ IGOT60R042D1
Gate Drivers	EiceDRIVER™ 1EDF5673K
Transformer	ELP43/10/28 core, N97 ferrite, no air-gap, 16 turns prim., 1200x40 µm litz, 10 turns sec., 1200x40 µm litz, L_σ = 13 µH, L_m = 300 µH
Sw. Freq. $f_{sw,DABC}$	180-330 kHz

38 GaN switches, the 12 SiC Schottky diodes, and the 4 DABC transformers. Further, **Fig. 5c** gives an overview on some key aspects of the PCB layout, which otherwise follows state-of-the art best practices, e.g., regarding the design of GaN transistors' commutation loops, etc. Note that, except for a small credit-card-sized control board carrying a Xilinx Zynq-7000 SoC, the converter is realized on a single 8-layer PCB. Therefore, care has to be taken to prevent noise emissions from the power stages from disturbing measurements and logic circuitry. Placing the controller in the center of the converter facilitates routing the gate signals (blue arrows) without any overlap with noisy switch-node planes (red). The analog circuitry of the VR measurements is also placed in the relatively quiet center of the PCB, whereas the DABC measurements are beneath the transformer winding; a shielding layer in the PCB (top layer connected to logic ground) prevents noise issues. Furthermore, the PCB features cutouts for the boost inductors and the transformers, which facilitates the ultra-flat realization.

In the following, the operating modes and especially the loss models for the VR (**Section III**) and the DABC (**Section IV**) stages will be introduced, which then allow a quantitative comparison of the efficiency that the two-stage system achieves when it operates with 3/3-PWM or 1/3-PWM (**Section V**).

III. VIENNA RECTIFIER STAGE

As discussed in the introduction, there are two interesting options for how to operate a boost-type AC/DC PFC rectifier, specifically a VR, in a two-stage system. First, if standard 3/3-PWM is used, the intermediate DC-link voltage U_{xz} is kept at a constant value (for a given output voltage and power; different constant values may be favorable for different operating points) in the range of typically 640 V to 800 V (400 V grid, 1200 V diodes). However, as mentioned above, the downstream DC/DC converters can contribute to the rectifier's task of shaping the grid currents by pre-shaping the intermediate DC-link voltage u_{xz} into the six-pulse shape given by $u_{xz} = \max(u_a, u_b, u_c)$ (1/3-PWM), which then implies that, advantageously, at all times only one of the rectifier's bridge-legs is operating with PWM; see also **Fig. 3**. Note that to do so (i.e., to achieve sufficiently high control dynamics), the intermediate DC-link capacitors, C_{xy} and C_{yz} must be relatively small (specifically, 28 µF is used in the considered system).

A detailed comparative analysis of the VR semiconductor stresses and losses occurring with 3/3-PWM and 1/3-PWM is given in [37]. For the sake of brevity, we summarize the key results in **Tab. II**, where $f_{sw,VR}$ is the switching frequency, I_{avg} and $\hat{I}$ are the average and peak value of the sinusoidal input currents, respectively ($I_{avg} = 2/\pi \cdot \hat{I}$), M is the modulation index, and $\hat{U}$ is the peak value of the grid (input) phase voltages. Note that for 3/3-PWM, space-vector PWM (SVPWM), i.e., a common-mode (CM) third-harmonic injection of $u_{CM} = (u_{max} + u_{min})/2$ is assumed, whereby u_{max} and u_{min} are the maximum and minimum instantaneous phase voltage, respectively. The same CM voltage also appears for 1/3-PWM as a consequence of always two phases being clamped. The switching losses are considered with a linear model, $P_{sw} = P_{sw,0} + P_{sw,1}$, where $P_{sw,0}$ represents the current-independent capacitive switching loss contributions and $P_{sw,1}$ the dependency on the switched current. Compared to 3/3-PWM, 1/3-PWM reduces the switching losses by more than 66%, as at all times only the bride-leg corresponding to the phase with the lowest (absolute value) current operates with PWM. For the same reason, also the conduction losses of the transistors decrease significantly while the diode currents only increase slightly.

A. VR Loss Model

The paper's goal of providing a system-level comparative analysis of the EV charger operation with 3/3-PWM and 1/3-PWM requires a straightforward yet accurate loss model of the VR, which considers the main loss components (i.e., conduction and switching losses of the 600 V, 70 mΩ GaN transistors and the 1200 V SiC diodes, and the EMI filter losses; please refer to **Table I** for a detailed component list).

The conduction losses of all semiconductors follow directly from the per-device average and RMS currents given in **Tab. II**

TABLE II
COMPARISON OF THE VR SEMICONDUCTOR STRESSES RESULTING WITH 3/3-PWM AND 1/3-PWM, FOR UNITY POWER FACTOR OPERATION.

Parameter		Equation		Difference	Condition
		3/3-PWM	1/3-PWM		
Switching Losses P_{sw}	$P_{sw,0}$	$k_{sw,0} \cdot f_{sw,VR}$	$\frac{k_{sw,0}}{3} \cdot f_{sw,VR}$	−66%	/
	$P_{sw,1}$	$k_{sw,1} \cdot I_{avg} \cdot f_{sw,VR}$	$\left(1 - \frac{\sqrt{3}}{2}\right) k_{sw,1} \cdot I_{avg} \cdot f_{sw,VR}$	−86%	/
Switch RMS Current $I_{S,RMS}$		$\frac{\hat{I}}{\sqrt{\pi}} \sqrt{\frac{\pi}{2} + \frac{5\sqrt{3}-16M-8}{12}}$	$\frac{\hat{I}}{\sqrt{\pi}} \sqrt{\frac{\pi}{6} + 2\sqrt{3} \ln\left(\frac{\sqrt{3}}{2}\right)}$	−69.4%	
Diode RMS Current $I_{D,RMS}$		$\frac{\hat{I}}{\sqrt{\pi}} \sqrt{\left(\frac{1}{3} - \frac{3\sqrt{3}}{16}\right)(2M+1) + \frac{18M-1}{16\sqrt{3}}}$	$\frac{\hat{I}}{\sqrt{\pi}} \sqrt{\frac{\pi}{6} + \frac{\sqrt{3}}{8} \ln\left(\frac{256}{81}\right)}$	+9%	$U_{xz} = 640\,V$, $\hat{U} = 325\,V$ $M = \frac{\hat{U}}{(U_{xz}/2)} = 1.015$
Diode Average Current $I_{D,avg}$		$\hat{I}\frac{M}{4}$	$\hat{I}\frac{\sqrt{3}\ln(3)}{2\pi}$	+19.1%	

and the respective on-state characteristics from the datasheets. An electro-thermal model is used to account for the temperature-dependency of the conduction losses using a linear approximation of the on-state resistance's dependency on the junction temperature as $R_{on}(T_j) \approx 70\,m\Omega + 0.36\,m\Omega/K \cdot (T_j[°C] - 25\,°C)$ (note that the maximum specified nominal on-state resistance at room temperature, i.e., 70 mΩ, is used to ensure a conservative design). Furthermore, a (measured) thermal resistance from transistor junction to the cooling liquid of $R_{th,j-w} = 2.5\,K/W$ and an average liquid temperature of 35 °C are considered (note that the temperature difference between liquid inlet and outlet is less than 6 K and hence neglected).

Similarly, the switching losses can again be calculated with the equations from **Tab. II**, but it is interesting to briefly consider how the switching loss model parameters $k_{sw,0}$ and $k_{sw,1}$ are obtained. Even though full (calorimetrically) measured loss maps for the employed GaN transistors are available [43], these pertain to symmetric half-bridges and not to the (relevant hard-switching) commutations against a 1200 V SiC Schottky diode as occurring in the considered VR. To account for this, and especially also for the second diode that is not actively involved in a commutation but, being connected to the switch node, contributes to the capacitive switching losses, we calculate $k_{sw,0}$ from the involved voltage-dependent device capacitances (and the parasitic switch-node capacitance resulting from the PCB layout) as described in [44]. Note that $k_{sw,0}$ thus depends on the voltage u_{xy} (with 1/3-PWM, this value would be even time-variant, but, for simplicity, we use a constant value of $\overline{u}_{xz} = 537\,V$, i.e., the time average of u_{xz}, to calculate $k_{sw,0}$). On the other hand, the current-dependency of the switching losses is assumed to be dominated by the transistor's characteristic and hence $k_{sw,1}$ from the mentioned loss maps [43] is used.

Finally, the main loss contributions of the compact EMI filter (given the 560 kHz switching frequency) are the conduction losses of all inductive components, which can be modeled by a 70 mΩ series resistance for each phase; core losses of the magnetic components are neglected.[3]

B. Experimental Verification

To verify the aforementioned loss models, the VR stage is commissioned and operated with 3/3-PWM and with a (for testing purposes) reduced switching frequency of 400 kHz. **Fig. 6a** compares the calculated (using the model from above) and measured efficiencies of the VR stage and provides a (calculated) loss breakdown. Even though the loss model is quite straightforward, it achieves a reasonably good accuracy. **Fig. 6b** shows the calculated efficiency curve and loss breakdown of the VR stage operating with 1/3-PWM.[4] The significant reduction of switching losses improves the efficiency by almost one percentage point at nominal and even more at lower output power; this effect will be even more pronounced at the final switching frequency of 560 kHz.

IV. DABC MODULES WITH WIDE OUTPUT VOLTAGE RANGE

From a VR perspective alone, operation with 1/3-PWM seems clearly favorable. However, the question to be answered later in **Section V** is at what cost in terms of possibly increased DABC losses the VR's efficiency gain comes. Therefore, this section discusses, similarly, the operating modes and loss model of the DABC modules.

The DABC [45] is a versatile isolated DC/DC converter topology that achieves tightly controlled bidirectional power flow and hence can operate with widely varying voltage transfer ratios [11], [46]. Essentially, two full bridges actively apply voltages to the primary and the secondary side (i.e., u_p and u_s as shown in **Fig. 4** for $DABC_I$) of a magnetic assembly (including a transformer with its stray inductance, and possibly—not used here—a dedicated series inductor) to shape the current in the (stray) inductance. Whereas in the simplest case, both bridges operate with full duty cycle and hence the phase shift,

[3] For the operating conditions of **Fig. 6a**, calculations based on manufacturer data indicate less than 0.6 W of core losses per boost inductor; the other magnetic components of the EMI filter are expected to show lower core losses as they carry already much lower high-frequency ripple currents. At rated output power, core losses thus account for less than 1% of the total losses.

[4] Note that it is not possible to measure the efficiency of the VR operating with 1/3-PWM without also running the DC/DC converters to shape u_{xz}. The corresponding measurements of the two-stage system are presented later in **Section VI**.

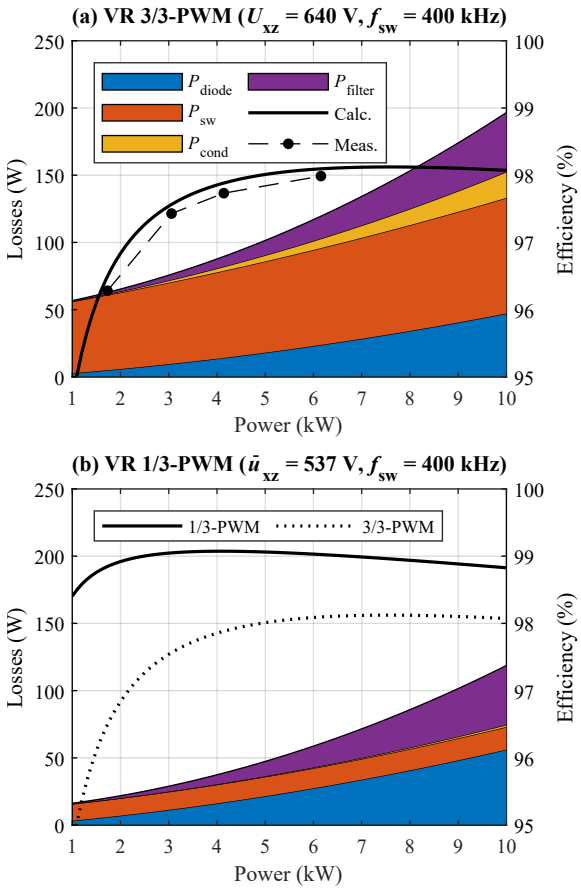

Fig. 6. Calculated efficiencies and loss breakdowns of the VR operated **(a)** with 3/3-PWM (U_{xz} = 640 V), including measured (Yokogawa WT-1804E) efficiencies for verification, and **(b)** with 1/3-PWM, which achieves a significant reduction of the switching losses. Note that this comparison considers a switching frequency of 400 kHz, i.e., lower than the 560 kHz used in the final prototype.

TABLE III
KEY SPECIFICATIONS OF A SINGLE DC/DC DABC MODULE.

Parameter	Value
Input Voltage U_{in} (i.e., u_{xy} or u_{yz})	240 V…400 V
Output Voltage U_{out}	100 V…500 V
Nominal Power P_{out}	2.5 kW
Maximum Output Current $I_{out,max}$	12.5 A

ϕ, between the primary-side and secondary-side square voltages is adjusted to realize a desired power flow [45], further degrees of freedom exist, which can be leveraged to achieve certain optimality criteria. Specifically, these are the duty cycles D_1 of the primary-side and D_2 of the secondary-side full-bridges, and the switching frequency, $f_{sw,DABC}$, see **Fig. 7a**. For example, [46], [47] provides closed-form solutions to calculate the set of modulation parameters that results in minimum RMS current and hence minimum conduction losses for a given operating point, which is defined by the tuple $(U_{in}, U_{out}, P_{out})$, i.e., the input and output voltages, and the desired power transfer. However, switching losses cannot be neglected either, i.e., it is advantageous to select modulation patterns that also achieve soft-switching for all transitions (or at least for as many transitions as possible).

A. Simplified Modulation Scheme

Aiming for a simplified modulation method that features continuous modulation parameters in case of changing operating points (advantageous for the implementation), limits RMS currents, and achieves mostly soft switching, one degree of freedom is fixed. Specifically, the duty cycle of the bridge operating from the lower DC voltage (referred to the same side of the transformer, e.g., the comparison is between U_{in} and nU_{out}) is clamped to the maximum of $D = 0.5$ (note that $D = T_{pulse}/T_{sw}$, i.e., $D = 0.5$ results in a symmetric square wave). Therefore, $D_1 = 0.5$ in boost ($nU_{out} > U_{in}$) operation and $D_2 = 0.5$ in buck ($nU_{out} < U_{in}$) operation, where n denotes the transformer turns ratio. This constraint reduces the possible twelve basic voltage patterns (i.e., sequences of switching transitions of the two bridges) that can be generated by two full-bridges [46], [47] to the only two sensible choices shown in **Fig. 7ab**.

With the phase-shift, ϕ, used as a control input for the power flow, two degrees of freedom that must be determined otherwise remain (one duty cycle and the switching frequency). In addition to aiming for minimum RMS currents, advantageously also as many of the switching transitions as possible should be soft, i.e., zero-voltage switching (ZVS) transitions. This means that the switched transistor currents should have the correct sign and should be high enough to charge/discharge the parasitic output capacitances C_{oss} of the transistors within the interlock delay time interval [48]. For the selected switching patterns, there are two switching transitions where it is inherently more difficult to realize these ZVS conditions, namely t_2 and t_3 in the boost mode and t_1 and t_3 in the buck mode (see **Fig. 7ab**). Considering the boost mode, the corresponding switched currents are

$$i_{L,t2,boost} = \frac{\frac{1}{f_{sw,DABC}} nU_{out}(U_{out}n - U_{in})D_2^2 + PL_s}{2U_{out}D_2nL_s}, \quad (1)$$

$$i_{L,t3,boost} = \frac{1}{2L_s f_{sw,DABC}} \left(\frac{1}{2}U_{in} - nD_2U_{out}\right), \quad (2)$$

where U_{in} and U_{out} denote the input and output voltages of a single DABC module (see **Table III**) and no magnetization current is considered. Note that all current values are referred to the primary side, even though the first of these transitions actually happens in the secondary-side bridge with a correspondingly scaled (by the turns ratio n) current of the opposite sign (if the positive current direction is in all cases defined as out of the bride-leg's switch node).

Ideally, in each case both of these currents should equal a certain minimum current, $I_{ZVS} > 0$, that ensures full ZVS transitions. Thus, the two remaining degrees of freedom of the modulation pattern should be selected accordingly to ensure $i_{L,t2,boost} = -I_{ZVS}$ and $i_{L,t3,boost} = I_{ZVS}$. Note that the correct sign depends on whether the transition occurs on the primary or on the secondary side (see above) as well as on the direction of the switching transition (positive-to-negative or negative-to-positive voltage). From these conditions, the remaining duty

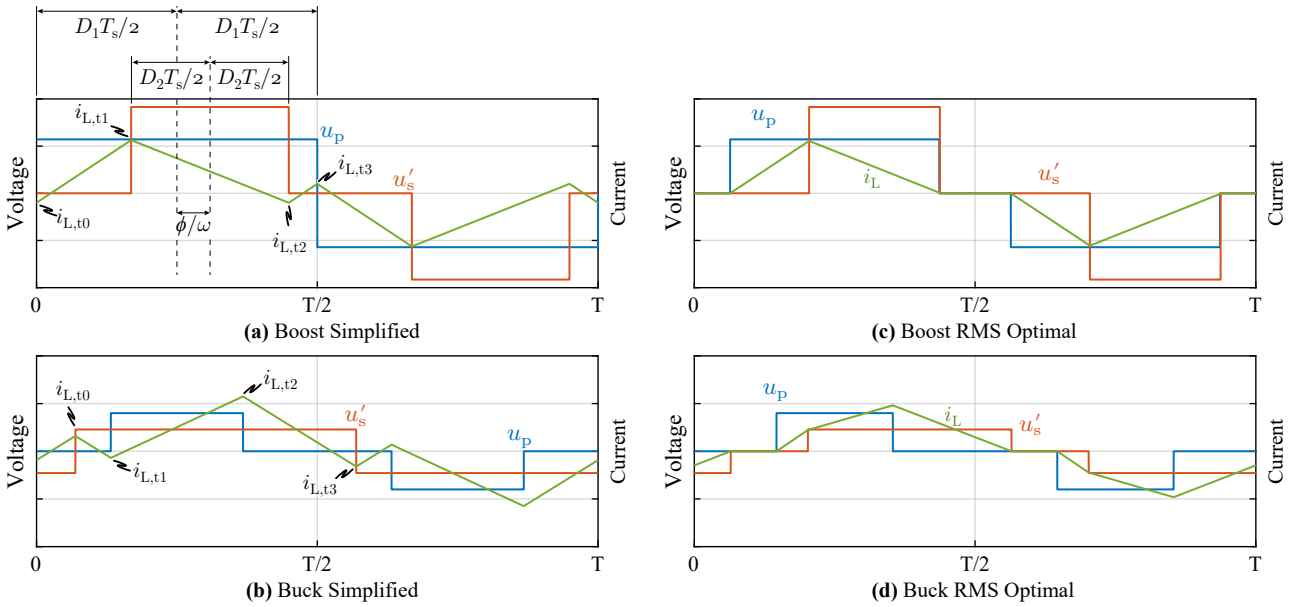

Fig. 7. Conceptual DABC waveforms (voltage patterns) for **(a,b)** selected simplified modulation with one duty cycle clamped to 0.5, and **(c,d)** the modulation scheme resulting in minimum transformer RMS current [46], [47].

cycle (D_2 in the boost mode) follows as

$$D_2 = \frac{-4 f_{\mathrm{sw,DABC}} I_{\mathrm{ZVS}} L + U_{\mathrm{in}}}{2 U_{\mathrm{out}} n}, \tag{3}$$

and the switching frequency is given by (4). Similar considerations can be made for the buck mode to find the conditions $i_{\mathrm{L,t1,buck}} = -I_{\mathrm{ZVS}}$ and $i_{\mathrm{L,t3,buck}} = -I_{\mathrm{ZVS}}$. Taking into account the symmetry of the voltage sequences (see **Fig. 7ab**) identical equations for D_1 and $f_{\mathrm{sw,DABC}}$ as (4) and (3) result, where, however, nU_{out} and U_{in} need to be exchanged. By doing so, (3) is valid for D_1 (remember that $D_2 = 0.5$ in the buck mode).

Considering three exemplary input voltages, **Fig. 8a** gives an overview of the resulting modulation parameters' dependency on the output voltage, for the nominal output power of 2.5 kW (note that at low output voltages, the maximum output current of 12.5 A limits the power as indicated in **Fig. 8c**).[5] Furthermore, **Fig. 8b** shows the four (per half period) switched current values (I_{sw1} and I_{sw2} are for the primary-side bridge, I_{sw3} and I_{sw4} are for the secondary-side bridge), where a negative value indicates hard switching. Note that for each operating point at most one switching transition (per half period) occurs without ZVS, specifically at low output voltages. There, a further reduction of $f_{\mathrm{sw,DABC}}$ below 180 kHz would be needed to ensure ZVS, which is not possible without increasing the losses of (and eventually saturating) the transformer core. Finally, **Fig. 8c** indicates the transformer RMS current and compares it against that achieved by the RMS-optimal modulation method from [46], [47] (see **Fig. 7cd** for the conceptual waveforms obtained with that modulation method). Clearly, the employed simplified modulation scheme results in only slightly higher RMS current stress, but ensures ZVS for most switching transitions.

[5]Note that for now each operating point's phase shift ϕ is calculated numerically such that the desired power transfer results; in the final realization, ϕ is calculated by the DABC voltage controller (see **Section VI-A**).

B. DABC Loss Model

Again, a straightforward yet sufficiently accurate loss model of the DABC modules is needed. Note that in contrast to the VR, the DABC modules employ low-ohmic 600 V, 42 mΩ GaN transistors on both, the primary and the secondary side. Please refer to **Tab. I** for a detailed list of components.

To accurately predict the component stresses of a DABC module, first an accurate representation of the transformer current waveform must be obtained, because a rather small change of a few amperes in one of the switched currents can decide on whether the transition occurs with ZVS or not, Obviously, this can quickly lead to large loss calculation errors. Furthermore, due to the small series inductance ($L_\sigma = 13\,\mu$H), the transformer current waveform is sensitive to non-idealities that must be expected in a real converter. Therefore, unlike as for the VR, we do not employ a purely analytical model. Instead, the implemented numerical waveform generator thus first takes into account the (current-dependent) effects of all resistances in the current path as well as the transformer's magnetizing inductance according to [49]. Then, also the voltage-time-area contributions appearing during the interlock delay time of 50 ns are considered, which can be estimated based on the GaN transistors' output capacitances C_{oss} and the direction

$$f_{\mathrm{sw,DABC}} = \frac{U_{\mathrm{in}}^2 \left(U_{\mathrm{in}} - nU_{\mathrm{out}}\right)}{2\left(2I_{\mathrm{ZVS}}U_{\mathrm{in}}^2 - 3I_{\mathrm{ZVS}}U_{\mathrm{in}}nU_{\mathrm{out}} - PnU_{\mathrm{out}} - \sqrt{I_{\mathrm{ZVS}}^2 U_{\mathrm{in}}^2 nU_{\mathrm{out}}^2 - 4I_{\mathrm{ZVS}}P\,U_{\mathrm{in}}^2 nU_{\mathrm{out}} + 6I_{\mathrm{ZVS}}PU_{\mathrm{in}}n^2U_{\mathrm{out}}^2 + P^2nU_{\mathrm{out}}^2}\right)L_{\mathrm{s}}} \tag{4}$$

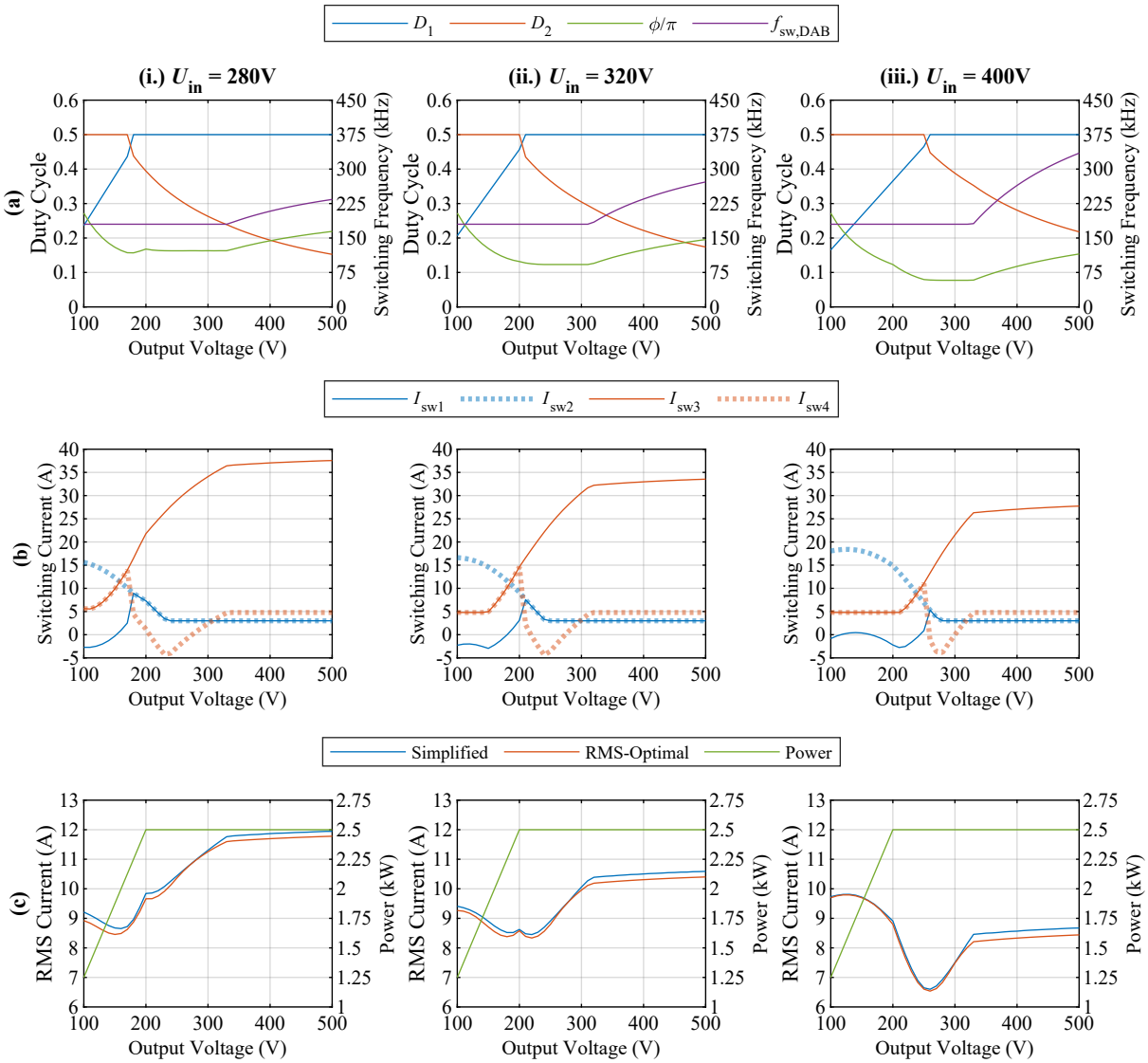

Fig. 8. **(a)** DABC control parameters (duty cycles D_1, D_2, normalized phase shift ϕ/π, and switching frequency $f_{sw,DABC}$) obtained with the proposed simplified modulation scheme; note that one duty cycle is always clamped to 0.5. Nominal power (or, for low output voltages, the maximum power compatible with the output current limit of 12.5 A, see (c)), and three different input voltages are considered in (i), (ii), and (iii), respectively. **(b)** Switched currents (I_{sw1} and I_{sw2} are in the primary-side bridge, I_{sw3} and I_{sw4} in the secondary-side bridge) within one half period; positive values indicate ZVS transitions. **(c)** RMS transformer currents of the proposed simplified and the RMS-optimal modulation scheme from [46], [47].

and the magnitude of the switched current. Given the current-dependency of these effects, a few iterations of the waveform generator routine are needed for the waveform to converge to its final shape.

With the transformer current waveform known, it is then straightforward to extract the transistor currents and the corresponding conduction losses, whereby again a temperature-dependent on-state resistance characteristic of the 600 V, 42 mΩ GaN transistors is considered, i.e., $R_{on}(T_j) \approx 42\,\text{m}\Omega + 0.28\,\text{m}\Omega/\text{K}\cdot(T_j[^\circ\text{C}] - 25\,^\circ\text{C})$. The thermal model uses $R_{th,j-w} = 2.3\,\text{K/W}$ to account for the lower on-state resistance and hence larger chip area. The switching losses incurred by each transition are obtained from the switched current (direction, magnitude) and published (calorimetrically) measured loss maps for hard-switched and soft-switched transitions [50]. However, special attention has to be paid to cases where the switched current is positive yet not high enough to achieve full soft-switching. Then, partial hard-switching with correspondingly higher losses occurs [48]. Time-domain simulations of the switching transitions, considering the non-linear device capacitances, are used to obtain the residual switched voltages and the expected partial ZVS losses [48] for low-current ZVS transitions. The loss maps are then modified accordingly in the relevant region, i.e., for soft-switching currents < 2.5 A, using quadratic fits similar to [51].

Finally, the transformer winding losses are calculated using the measured frequency-dependent AC resistance of a prototype transformer as well as the current waveform with all its harmonics. The core losses are estimated using the datasheet loss maps for N97 ferrite material, assuming a core temperature of 100 °C.

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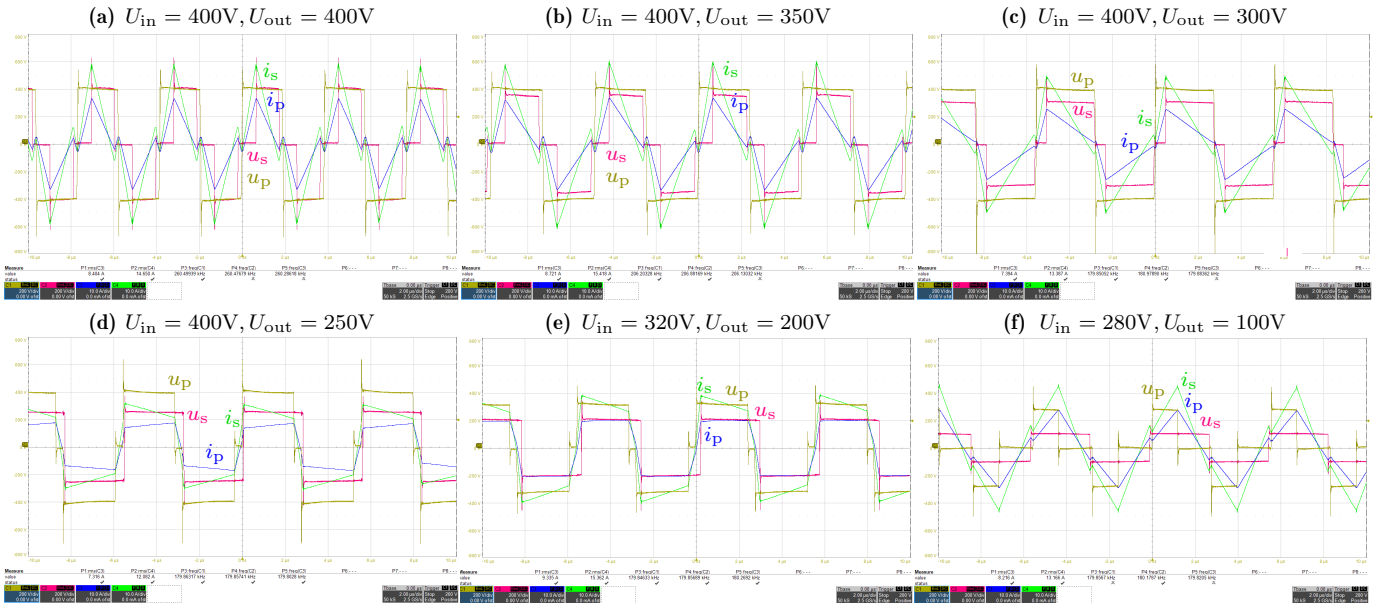

Fig. 9. Measured waveforms of a DABC module operating at rated load of 2.5 kW (except for the case with an output voltage of 100 V, where the 12.5 A maximum output current limits the power to 1.25 kW, see also **Fig. 10**) and with various input/output voltage combinations. u_p, u_s, i_p and i_s are the primary-side and secondary-side transformer voltages and the primary-side and secondary-side transformer currents, respectively.

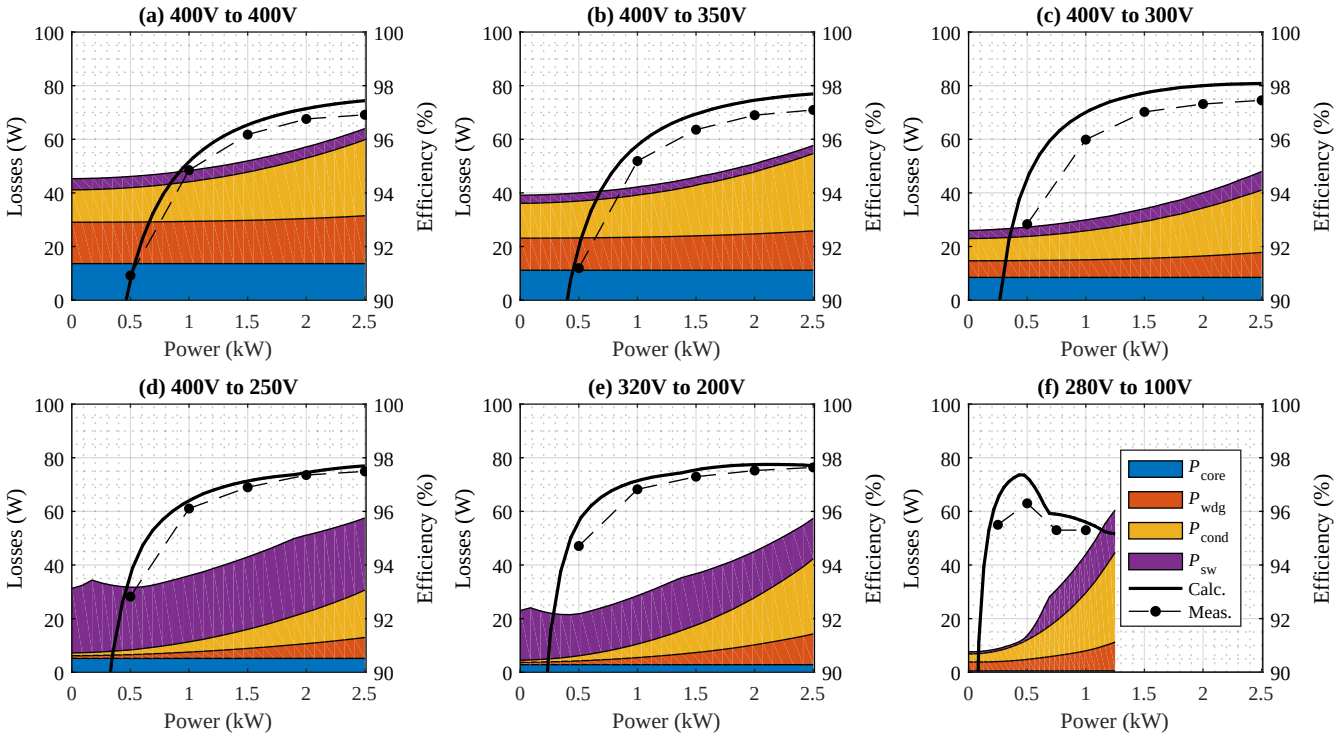

Fig. 10. Measured and calculated DABC module efficiencies for various operating points, and calculated loss breakdowns. Note that the output current limit (12.5 A, single module) limits the power to 1.25 kW when operating with an output voltage of 100 V only.

C. Experimental Verification

Fig. 9 shows measured voltage and current waveforms of a DABC module for six different operating points (remember that each DABC module connects to only one half of the split VR DC-link, see **Fig. 4**, hence the maximum input voltage is U_{in} = 400 V for the maximum U_{xz} = 800 V and, similarly, the output voltage is, e.g., U_{out} = 400 V for a system output voltage of U_o = 800 V). The implemented simplified modulation scheme results, as expected, in one duty cycle always being equal to 0.5. **Fig. 10** shows the measured (Yokogawa WT-3000) efficiencies of the DABC module, again for six different operating points. The comparison with the calculated efficiency curves shows good accuracy. Furthermore, the calculated loss breakdowns are shown, which illustrate that for different operating points,

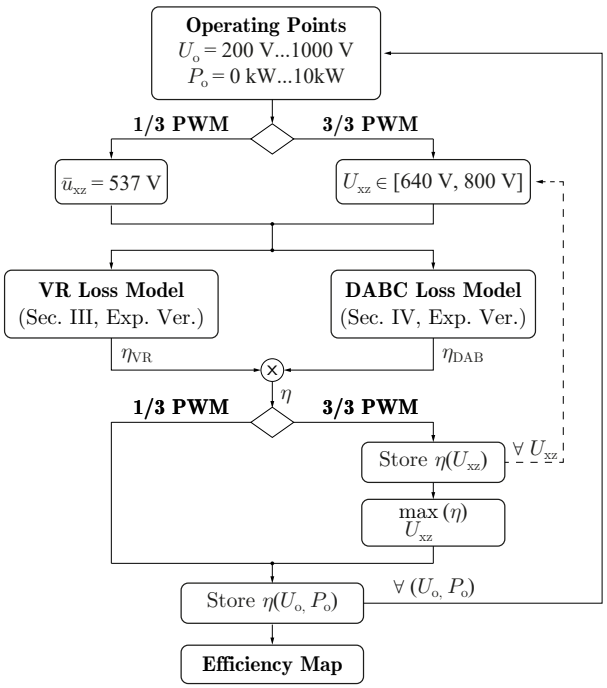

Fig. 11. Flowchart illustrating the procedure used for obtaining the efficiency maps shown in **Fig. 12**. For 3/3-PWM, either a fixed U_{xz} for all operating points can be used, or, alternatively and as indicated by the dashed line, for each operating point an optimized U_{xz} that results in highest overall efficiency can be used. In contrast, for 1/3-PWM, u_{xz} shows a time-varying six-pulse shape regardless of the operating point, and the corresponding average value $\bar{u}_{xz}$ is used for the calculations. Note further that the loss models of the VR and of the DABC have been introduced and experimentally verified individually in **Section III** and **Section IV**, respectively.

different loss components dominate, e.g., conduction losses for the case shown in **Fig. 9a** and (partial) hard-switching losses for the case of **Fig. 9d**; note that this is consistent with the theoretically calculated switched currents for this operating point, some of which are borderline negative, see **Fig. 8b.iii**. Note further that all four DABC modules have been tested and shown similar performance.

V. Optimum Operation of the Two-Stage System

In the previous two sections, the detailed loss modeling of the VR stage and the DABC modules have been discussed, and the accuracy of the relatively straightforward models has been demonstrated by close agreement of calculated and measured efficiencies. In a next step, the introduced loss models can thus be used to assess the different options of how to operate the full, two-stage EV charger demonstrator comprising a VR stage and four DABC modules (see **Fig. 5**). This is done by calculating efficiency maps, i.e., efficiencies for a grid of operating points defined by the tuples (U_o, P_o) in the ranges given in **Fig. 4**, and considering different operating regimes. **Fig. 11** provides an overview of this process, which is detailed in the following together with the results.

A. Operation with 3/3-PWM

A first basic option is to select a single, *constant* value for U_{xz} that is kept regardless of the operating point. The VR then operates with 3/3-PWM, regulates U_{xz} to a constant value, and the DABCs provide isolation and scale the voltage as required by the load. **Fig. 12a** and **Fig. 12b** show the resulting efficiency maps for the considered output power and output voltage ranges for U_{xz} = 640 V and U_{xz} = 800 V, respectively. Clearly, the region of maximum efficiency shifts between the two cases. Therefore, it is beneficial to consider adapting the intermediate DC-link voltage U_{xz} depending on the operating point, such that minimum overall losses (i.e., sum of VR and DABC losses) result.

Fig. 12c shows the corresponding optimal selection of U_{xz} in the range of 640 V to 840 V (the lower limit ensures sufficient control margin for a 400 V grid, and the upper ensures compatibility with the employed 1200 V diodes and 600 V GaN transistors, the latter being exposed to $U_{xz}/2$ only). **Fig. 12d** shows the corresponding efficiency map for optimally selected U_{xz} values and **Fig. 12e** illustrates the improvement (in percentage points, p.p.) over the case with an operation-point-independent U_{xz} = 800 V shown in **Fig. 12a**. Especially at lower output voltage, it pays to select a low U_{xz} value, too, which enables the DABCs to operate closer to their natural voltage transfer ratio ($n = 16/10$). Correspondingly, U_{xz} should increase with the output voltage, but only up to a point ($U_o \approx 600$ V). For even higher output voltages, a slight reduction of U_{xz} lowers the VR switching losses more than it increases the DABC losses. The changing VR loss share shown in **Fig. 13a** illustrates this point.

B. Operation with 1/3-PWM

So far, adaptive but, for a given operating point, still *constant* intermediate DC-link voltages U_{xz} and hence 3/3-PWM of the VR have been considered. However, as discussed earlier, the DABC modules can be utilized to shape the intermediate DC-link voltage into a time-varying six-pulse shape to facilitate 1/3-PWM operation of the VR with the associated significant reduction of switching losses (note the lower VR loss share in **Fig. 13b**). **Fig. 12f** shows the corresponding efficiency map, whereby the losses have been calculated approximating the time-varying voltage u_{xz} by its average value $\bar{u}_{xz}$ = 537 V. **Fig. 12g** then shows the efficiency change (in percentage points, p.p.) between 1/3-PWM and 3/3-PWM (with adaptive U_{xz}). Especially for lower output voltages and lower power levels, a significant efficiency increase of up to 2% results; this is not only because of the switching loss saving of the VR stage, but also because the lower u_{xz} in 1/3-PWM allows the DABC modules to operate closer to the natural voltage transfer ratio. At high output voltages and higher power levels, switching to 1/3-PWM is not always beneficial, as on the system level the VR loss reduction might be overcompensated by increasing DABC losses.

C. Optimal Combined 1/3-PWM and 3/3-PWM

Finally, **Fig. 12h** shows the efficiency map that can be achieved by the optimal combination of 1/3-PWM and 3/3-PWM. The thick dashed line delineates the region where 1/3-PWM should be used (i.e., where 1/3-PWM gives higher system-level efficiency than 3/3-PWM). **Fig. 13c** shows the

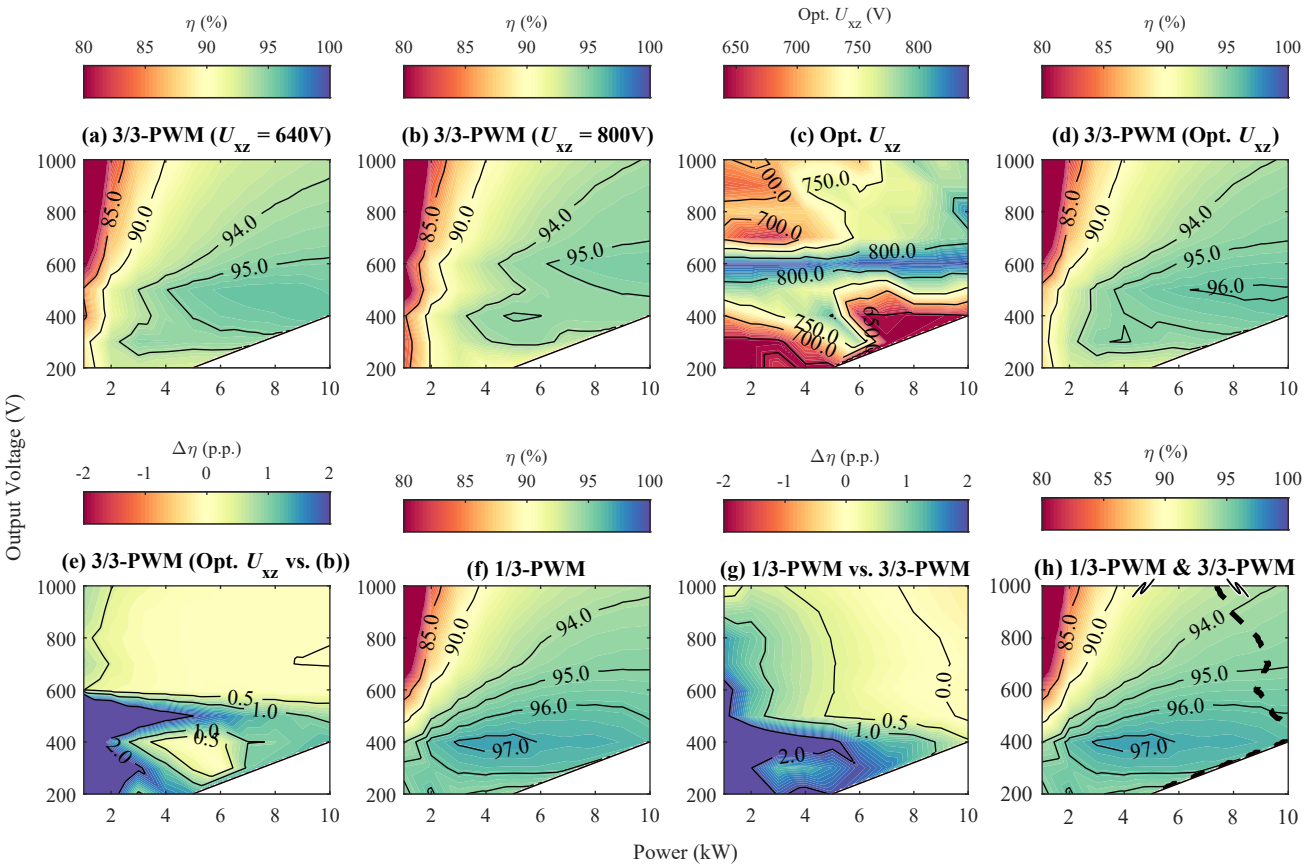

Fig. 12. Efficiency of the two-stage system operated with 3/3-PWM and **(a)** constant U_{xz} = 640 V or **(b)** U_{xz} = 800 V. Advantageously, however, U_{xz} is adapted with the operating points as shown in **(c)** to achieve the best possible (with 3/3-PWM) overall efficiency shown in **(d)**; **(e)** shows the improvement compared to (b) in percentage points (p.p.). **(f)** shows the efficiency when operating with 1/3-PWM and **(g)** gives the improvement compared to (d), i.e., 3/3-PWM with adaptive U_{xz}. Finally, **(h)** shows the best overall efficiency obtained when both, 3/3-PWM and 1/3-PWM are considered; the area where 1/3-PWM should be selected is highlighted. Note that the maximum output current of 25 A limits the power for low output voltages.

corresponding VR loss share. The sharp step change at the boundary exists because even though the efficiency of the total system does change only very slightly (see **Fig. 12h**), the loss contributions of the VR and the DABCs change significantly when switching from 1/3-PWM to 3/3-PWM.

Note that in terms of efficiency (gains), see **Fig. 12g**, for the given system it might as well be a good engineering decision to *always* operate with 1/3-PWM, i.e., to forego certain minor loss savings in a rather small part of the operating range in favor of a simpler implementation. It is also essential to highlight that the results shown here are valid for our specific realization of the two converter stages. We reiterate that the system has been initially designed for 3/3-PWM operation; by changing the operating regime, a significant efficiency improvement can be achieved. In general, note that the boundary between 1/3-PWM and 3/3-PWM, and the overall efficiency map, depend (amongst other parameters), on the DABC modules' natural voltage transfer ratio and hence on the selected transformer turns ratio. Such degrees of freedom, and the possibility to employ 3/3-PWM and 1/3-PWM, should be considered for a new converter design, whereby a mission profile (weighted efficiency) could be used to identify, e.g., the optimum natural voltage transfer ratios of the DABC modules (i.e., the transformer turns ratio).

D. Output Series/Parallel Reconfiguration

In the standard prototype configuration (see **Fig. 4**), the total output voltage is shared by a series connection of two DABC modules. However, at lower output voltages it would be beneficial to reconfigure the DABC modules such that all four would be connected in parallel. Clearly, the maximum output voltage is then limited to 500 V. However, advantageously, the maximum output current increases to $4 \cdot 12.5\,\text{A} = 50\,\text{A}$, which implies that nominal power can be supplied even at only 200 V output voltage. Thus, **Fig. 14** shows the efficiency map considering all degrees of freedom (i.e., 3/3-PWM, 1/3-PWM, parallel reconfiguration of DABC outputs) to optimize the efficiency for each operating point. As an aside, note that this reconfiguration of the DABC outputs essentially has a similar effect as changing the transformer turns ratio: it shifts the area of maximum efficiency. Finally, note further that the availability of four DABC modules could also be utilized to improve the part-load efficiency by only operating two instead of four modules. This, however, is not investigated further here.

VI. Hardware Verification

The two-stage demonstrator introduced in **Section II** and analyzed throughout the paper has originally been designed for

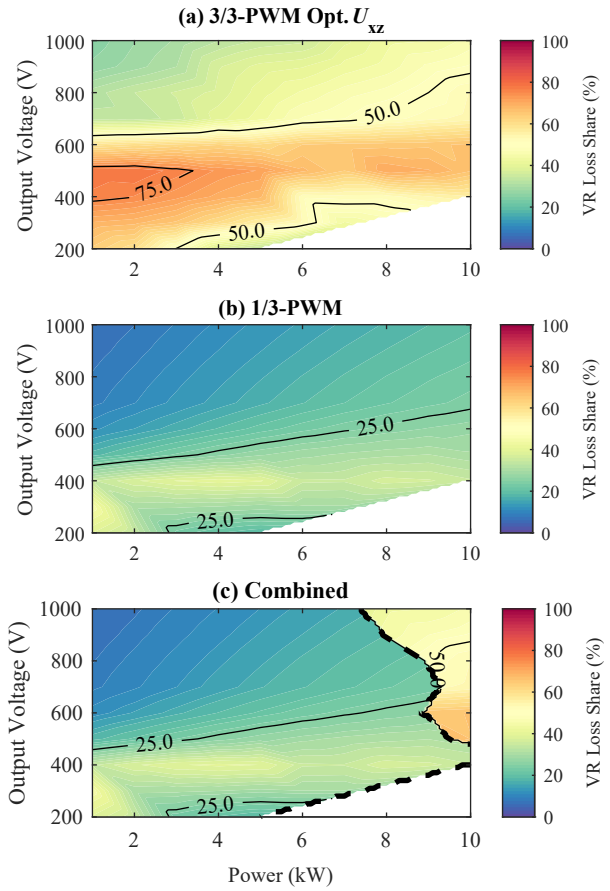

Fig. 13. Distribution of losses between the VR and the DABCs for operation with **(a)** 3/3-PWM (with optimum DC-link voltage), **(b)** 1/3-PWM, and **(c)** optimum combination of the two modes. Note that the maximum output current of 25 A limits the power for low output voltages.

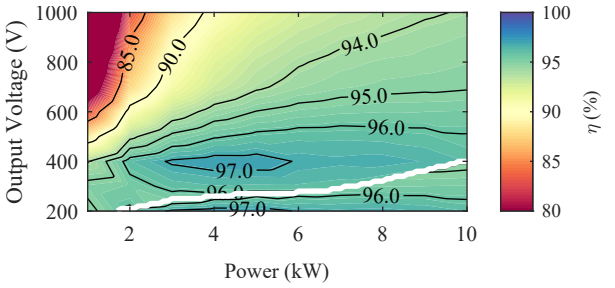

Fig. 14. Extension of the operating range by reconfiguring the four DABC modules (all four in parallel for output voltages lower than the white line indicates). The efficiency map considers the best combination of modulation (3/3-PWM and 1/3-PWM) and DABC module configuration for each operating point.

operation with 3/3-PWM. After briefly discussing some control implementation aspects, we then provide a comparison of grid current total harmonic distortion (THD), system efficiency, and EMI performance for operation with 3/3-PWM and with 1/3-PWM, which is the main subject of this paper.

A. Control System and Implementation

The control of the two-stage system is implemented on a Zynq-7000 SoC, which features a dual-core ARM central processing unit (CPU) and an integrated FPGA fabric. Advantageously, this allows to implement certain time-critical functions in the FPGA and more advanced algorithms in the CPU, as indicated in the overview control diagram shown in **Fig. 15**. Even though a smooth transition from 1/3-PWM to 3/3-PWM is possible [37], it is not strictly needed: as discussed in the previous **Section V**, due to the DAB's capability to step down or step up u_{xz} to the desired output voltage U_o, the selection of 1/3-PWM or 3/3-PWM is purely determined by efficiency considerations.[6] Therefore, the control implementation can be (externally) reconfigured between 3/3-PWM and 1/3-PWM operation; this is indicated by the two signal selectors in **Fig. 15**.

We will now briefly explain the main functional blocks of that control diagram, proceeding from left to right. First, the outer VR control loop regulates the intermediate DC-link voltage U_{xz} if 3/3-PWM is used; the DABCs then regulate, fully decoupled, the output voltage U_o. In contrast, if 1/3-PWM is used, the outer VR control loop regulates the output voltage. In both cases, a mains power reference (P^*_{33} or P^*_{13}) results. Together with the three measured (via two line-to-line voltage sensors, u_{ab} and u_{bc}) grid phase voltages, u_{abc}, the phase current references, i^*_{abc}, are then calculated. For 1/3-PWM, a common-mode voltage injection of $u_{CM} = 1/2 \cdot (u_{max} + u_{min})$ must be used, where u_{max} and u_{min} are the maximum and the minimum of the measured instantaneous phase voltages, respectively. As the duty cycles are calculated (in the FPGA, see below) by essentially dividing the phase voltage references by the actual intermediate DC-link voltage, u_{xz}, which, for 1/3-PWM, follows $u_{xz} = \max(u_{max}, |u_{min}|)$, this ensures automatically that the two respective phases are clamped (the duty cycles become 1 and 0, respectively). For 3/3-PWM, the common-mode voltage injection, u_{CM}, is a degree of freedom and various options do exist [52]; advantageously, the method from [23] could ensure zero midpoint current. However, in the following, the same CM voltage injection as for 1/3-PWM is employed, which is equivalent to employing standard space-vector PWM (SVPWM). As the required bandwidth is relatively low, these calculations are implemented in the CPU and executed with an update rate of $f_{vc} = f_{cc}/50 = 22\,\text{kHz}$, where f_{cc} will be explained immediately.

On the other hand, given the VR's rather high switching frequency of $f_{sw,VR} = 560\,\text{kHz}$ and the thus small boost inductors ($L = 30\,\mu\text{H}$) the grid current controllers are implemented in the FPGA to realize dual-update mode, i.e., a control loop execution frequency of $f_{cc} = 2f_{sw,VR} = 1.12\,\text{MHz}$. The controller outputs plus the feed-forward terms (i.e., the phase voltages including the CM injection) are then used to generate the VR reference voltages, u^*_{Babc}. Finally, using the

[6]This is in contrast to non-isolated two-stage systems such as analyzed in [12], [28], [38], [39], where the non-isolated DC/DC stage provides only buck *or* boost functionality, i.e., for certain output voltages, the front-end can not operate with 1/3-PWM (e.g., if a boost-type rectifier is combined with a buck-type DC/DC converter, $u_{xz} \geq U_o$ must hold at all times and hence 1/3-PWM is not possible for high output voltages.)

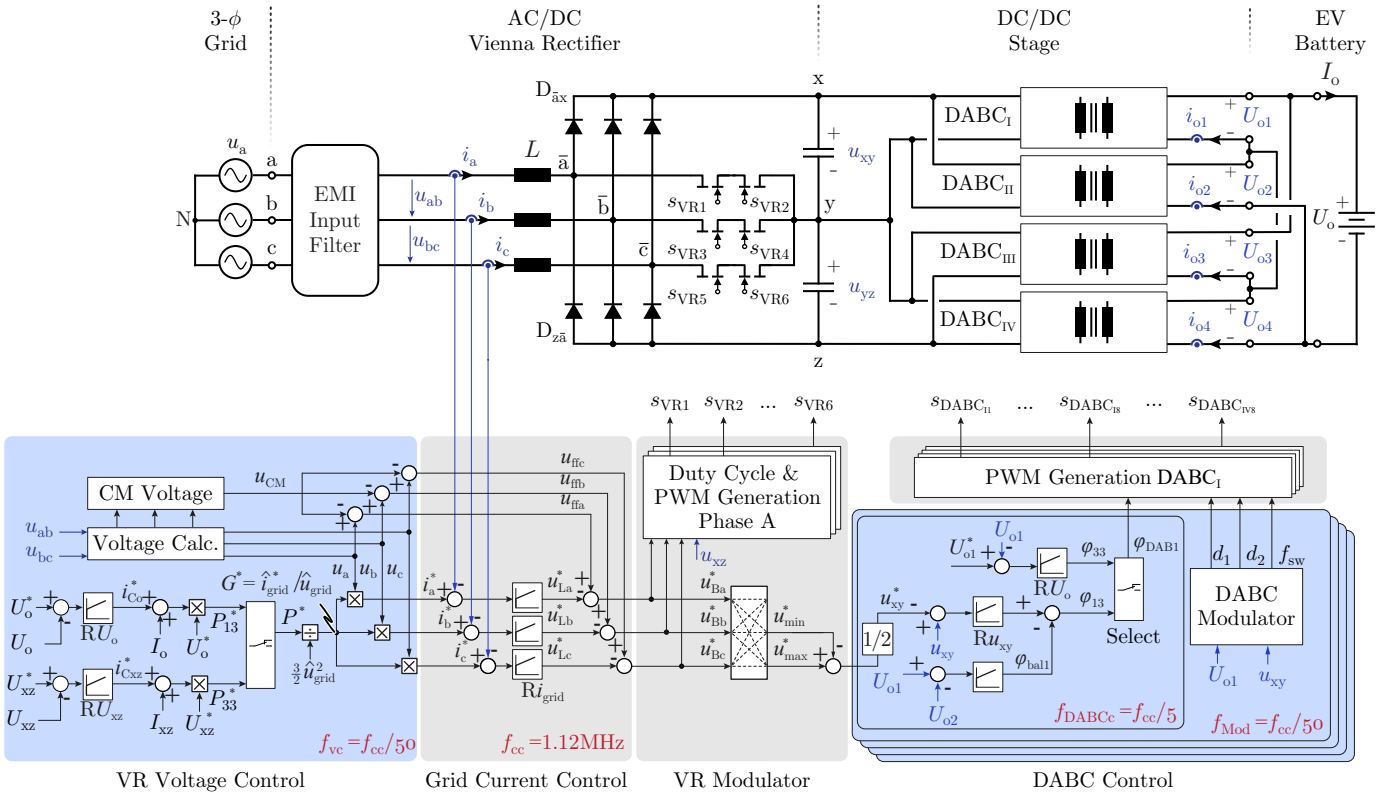

Fig. 15. Control diagram of the two-stage VR and DABC EV charger, which facilitates operation with either 3/3-PWM or 1/3-PWM. The functions with a blue background are implemented in the Zynq-7000 SoC's CPU whereas the functions with a gray background are implemented in the FPGA fabric. Please refer to the text for a description of the functional blocks.

measured DC-link voltage u_{xz}, the duty cycles are calculated[7] and ultimately the modulator generates the VR gate signals. Note that the FPGA clock frequency of 100 MHz results in limited yet sufficient quantization resolution (between 7 bit and 8 bit).

Further, the reference value for the intermediate DC-link voltage, u^*_{xz}, follows from the VR phase reference voltages and is fed to the DABC controllers, where, if 1/3-PWM operation is enabled, it is used as a control reference. Actually, two and two DABC modules regulate $u^*_{xy} = u^*_{xz}/2$ and $u^*_{yz} = u^*_{xz}/2$, respectively, and thereby ensure balanced intermediate DC-link halves (in addition to the shaping of u_{xz} as required by 1/3-PWM). Furthermore, since the VR can only control the total output voltage, an additional balancing controller is needed to ensure $U_{o1} = U_{o2} = U_{o3} = U_{o4}$. These controllers define the required power transfers of the DABC modules and hence the phase shifts $\phi_{DAB1,2,3,4}$. Because the required control bandwidth to shape u_{xz} is rather high (roughly 3 kHz in the current implementation), these controllers are executed in a CPU task with an update rate of $f_{DABCc} = f_{cc}/5 = 220$ kHz. On the other hand, the modulation parameters, i.e., the duty cycles D_1 and D_2 and the switching frequency $f_{sw,DABC}$, are calculated based on measured voltage values (see **Section IV**) in a slower task updating at again $f_{Mod} = f_{cc}/50 = 22$ kHz. Finally, the DABC PWM modulators are implemented in the FPGA.

[7]To avoid the costly division in the FPGA, the actual implementation correspondingly uses an approximation and scales the feed-forward terms u_{ffa}, u_{ffb}, and u_{ffc} with $1/u_{xz}$ in the CPU before passing them to the FPGA; a corresponding re-scaling of $u^*_{max} - u^*_{min}$ after being passed from the FPGA to the DABC control in the CPU is thus needed. This approach is feasible because of the small low-frequency voltage drops across the boost inductors (which are small given the high switching frequency) mentioned earlier, i.e., small values of u^*_{Labc}.

B. *Waveforms and THD Measurements*

Using the control structure discussed in the last subsection, the EV charger is operated with both 3/3-PWM and 1/3-PWM at the rated power of 10 kW and with an output voltage of $U_o = 500$ V. For 3/3-PWM, the total intermediate DC-link voltage is selected as $U_{xz} = 640$ V, i.e., the lowest possible value for 3/3-PWM which is hence closest ot $\bar{u}_{xz} = 537$ V resulting for 1/3-PWM. **Fig. 16** shows the measured waveforms of the three-phase mains currents, the intermediate DC-link voltages u_{xy} and u_{yz} (with $u_{xy} + u_{yz} = u_{xz}$), and the split output DC voltages $U_{o1} = U_{o3}$ and $U_{o2} = U_{o4}$ (remember that $U_{o1} + U_{o2} = U_o$). The split DC voltages on either side of the DABC modules are balanced well.

In 1/3-PWM mode, the three-phase mains currents show some low-frequency distortions around the peak values. This is a consequence of the limited control bandwidth of the DABCs, which thus cannot exactly reproduce the six-pulse waveform of u^*_{xz} around the polarity change of the dv/dt in the valleys. Nevertheless, with a DABC control execution frequency of 220 kHz, operation with 1/3-PWM (where two of the three phase currents follow from the u_{xz} impressed by the DABCs and

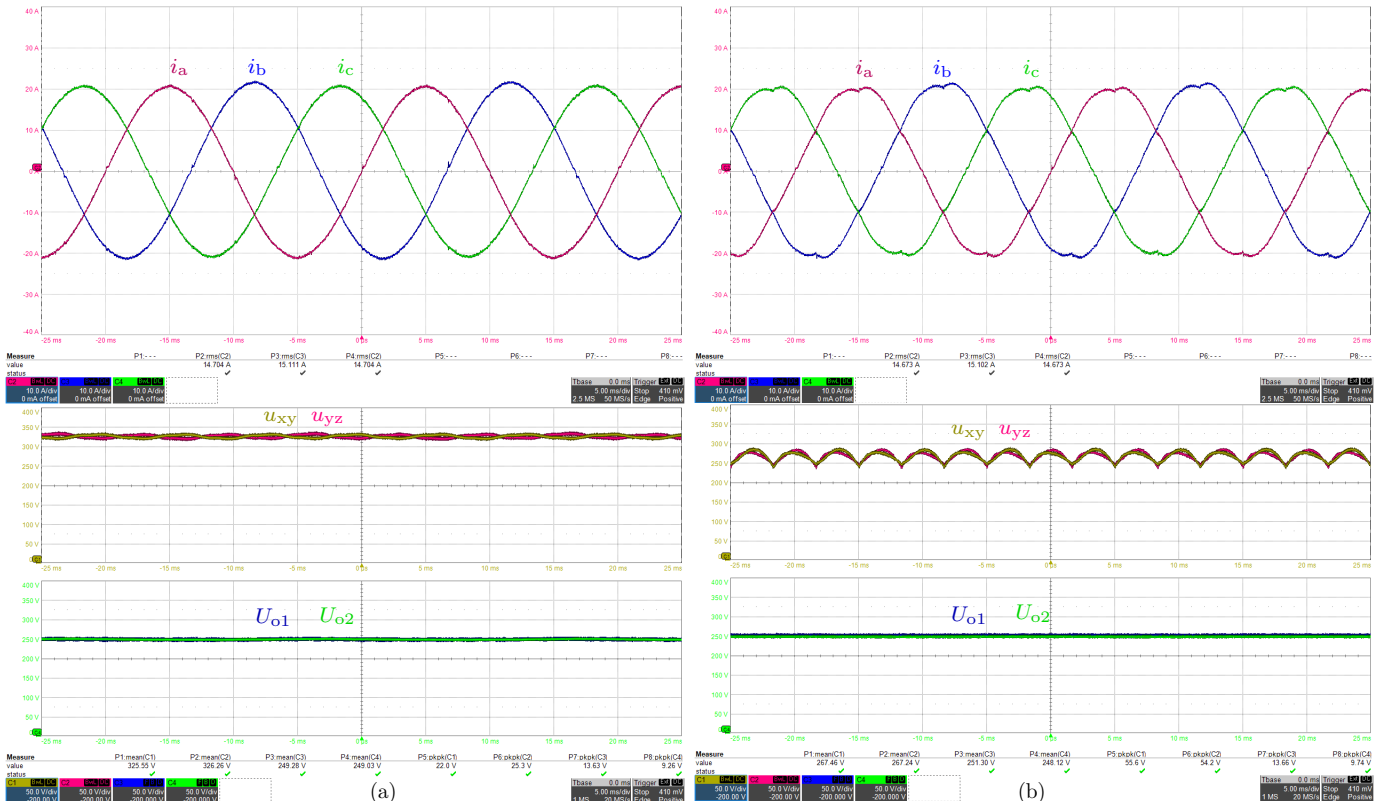

Fig. 16. Measured grid currents (i_a, i_b, i_c), intermediate DC-link voltages (u_{xy}, u_{yz} with $u_{xz} = u_{xy} + u_{yz}$), and output voltages (U_{o1}, U_{o2}) for $U_o = U_{o1} + U_{o2} = 500\,\text{V}$ and 10 kW rated output power; in **(a)** with 3/3-PWM ($U_{xz} = 640\,\text{V}$) and in **(b)** with 1/3-PWM.

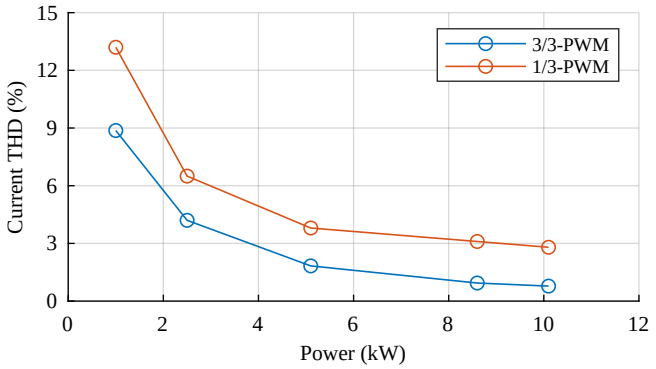

Fig. 17. Measured mains current THD (Yokogawa WT-1804E) for 3/3-PWM (with $U_{xz} = 640\,\text{V}$) and 1/3-PWM, respectively, in dependence of the output power and with an output voltage of $U_o = 500\,\text{V}$.

the VR directly controls only the remaining one) still achieves a total harmonic distortion (THD) of the mains currents of about 3% at rated power, see **Fig. 17**. This is higher compared to the about 1% resulting for 3/3-PWM (where the VR directly controls all three phase currents) but, given the efficiency improvement achieved with 1/3-PWM, seems a reasonable price to pay. Note that due to the high VR switching frequency, a turn-off delay compensation must be implemented to achieve these THD values; this is detailed in the **Appendix**.

C. Efficiency Measurements

Fig. 18a shows the calculated and measured (Yokogawa WT-1804E) efficiency characteristics of the two-stage system operating with 3/3-PWM ($U_{xz} = 640\,\text{V}$) and with 1/3-PWM, respectively, and an output voltage of $U_o = 500\,\text{V}$. The calculation results contain an additional offset of 16 W to account for the control hardware (Zynq-7000 SoC, gate drives, etc.). Similarly, **Fig. 18bc** show the calculated loss distributions between the stages as well as the measured total losses, demonstrating again a good accuracy of the relatively straightforward loss models for the VR and the DABCs introduced in **Section III** and **Section IV**, respectively. Clearly, at the considered exemplary operating points, operating with 1/3-PWM significantly reduces the VR losses at the expense of a moderate increase of the DABC losses only, as also visible in the full efficiency maps shown earlier in **Fig. 12**, which have been obtained using the individually verified loss models of the VR and the DABCs.

D. Comparative Conducted EMI Pre-Compliance Tests

Finally, it is an interesting question whether changing the operating mode of the two-stage system from 3/3-PWM (for which the system has been designed) to 1/3-PWM (which, advantageously, gives higher efficiency) affects the EMI noise emissions to an extent that would require modifications of the EMI filter design. Therefore, *comparative* pre-compliance EMI measurements have been carried out. To emulate worst-case grounding conditions, the DC output midpoint is connected to earth. The coldplate, on the other hand, is tied to the

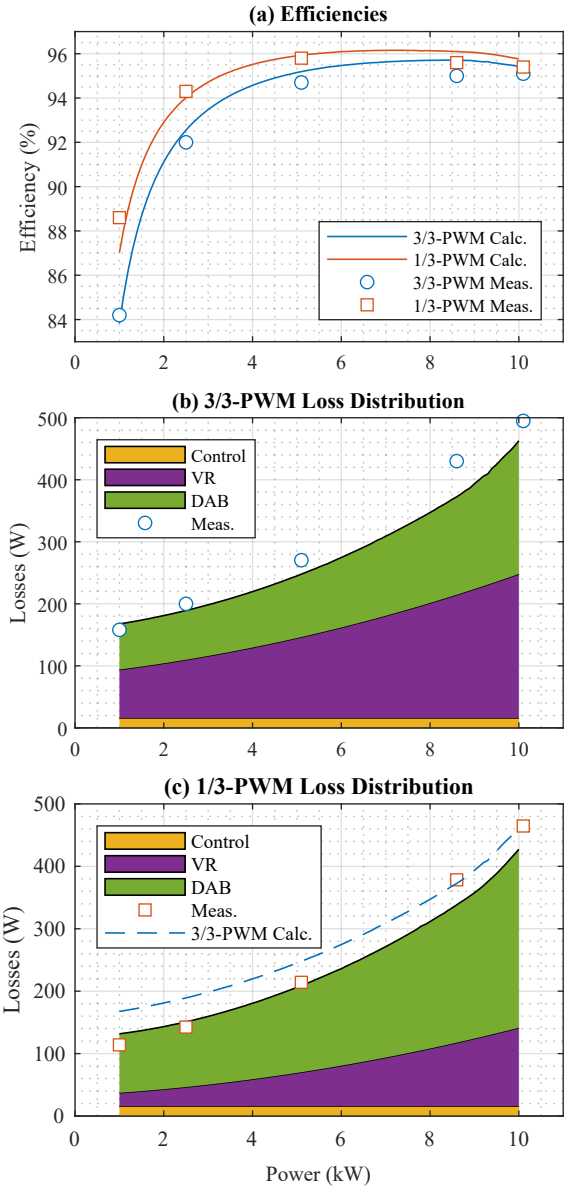

Fig. 18. **(a)** Calculated and measured (Yokogawa WT-1804E) efficiencies of the two-stage system with U_o = 500 V and operation with 3/3-PWM (U_{xz} = 640 V) and 1/3-PWM, respectively. **(b)** and **(c)** show the measured total losses and the (calculated) loss distributions between the VR and the DABCs for operation with 3/3-PWM and 1/3-PWM, respectively.

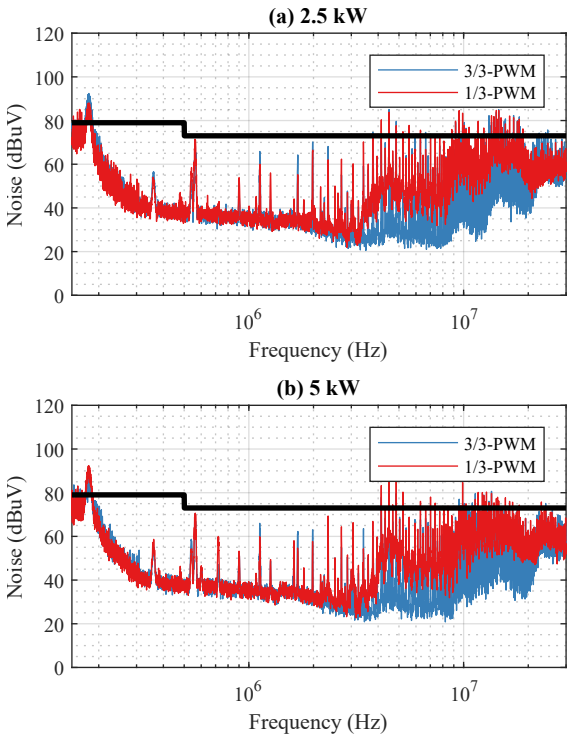

Fig. 19. Conducted EMI noise emission spectra of the two-stage demonstrator system for operation with 3/3-PWM (U_{xz} = 640 V) and 1/3-PWM, an output voltage of U_o = 500 V, and with **(a)** 2.5 kW output power and **(b)** 5 kW output power. A Rhode & Schwarz ESH2-Z5 three-phase LISN and a Rhode & Schwarz ESPI3 test receiver (setings: PK detector with 9 kHz resolution bandwidth (RBW), 1 ms measurement time, 0.1 % step size) have been used. The solid black line indicates the CISPR 11 Class A limit.

intermediate DC-link midpoint; deionized water is used as a coolant.

Fig. 19ab show the measured conducted EMI emissions for 2.5 kW and 5 kW output power, and with 500 V output voltage. For all measurements, an external CM choke has been placed at the mains input (3 × 5 turns on a VAC W517-51 core resulting in 140 µH CM inductance at 500 kHz; this CM impedance could be realized in a much smaller form factor for integration into the converter). On the other hand, no housing has been placed, which would help to reduce the noise emissions in the high-frequency range. Note that for both, operation with 3/3-PWM and with 1/3-PWM, the DABCs are expected to show at least some switching transitions without ZVS (see **Fig. 8**) and thus the selected operating point constitutes a worst-case for dv/dt-imposed emissions in the upper frequency range. The observed difference between 3/3-PWM and 1/3-PWM for frequencies above 5 MHz could well be explained by the circuit's non-idealities and component tolerances, which might allow for partial ZVS in case of 3/3-PWM.

Even though around 180 kHz, there is a minor violation of the CISPR 11 Class A limit[8], the main point of these results is *comparative* in nature: the noise emissions resulting for 3/3-PWM and 1/3-PWM operation are very similar. Hence, a system designed for 3/3-PWM can operate with 1/3-PWM without a redesign of the EMI filter.

VII. Conclusions

The paper first presents a 10 kW two-stage EV charger with a wide output voltage range of 200 V to 1000 V, which combines a three-level Vienna Rectifier (VR) AC/DC stage and four Dual Active Bridge Converter (DABC) modules. This, advantageously, enables a realization with latest-generation 600 V GaN technology and enables very high switching frequencies of 560 kHz for the VR and of up to 330 kHz for the DABCs, resulting thus in a flat, ultra-compact design with a power density of around 9 kW/dm^3 (about 150 W/in^3),

[8]This is because the DABC operating frequency has been lowered slightly compared to the switching frequency targeted in the original design; it could be addressed in a next design iteration by selecting a slightly lower EMI filter cutoff frequency and likely be implemented without a significant impact on the EMI filter volume.

not including the coldplate. Although, conventionally, the two stages would operate largely independently and hence the VR would switch all three bridge-legs with high-frequency PWM (3/3-PWM), alternative synergetic operation concepts are known. Specifically, the DABCs can be used to shape the shared intermediate DC-link voltage such that always only *one* of the VR's three bridge-legs must operate with PWM (1/3-PWM). Whereas it is directly possible (and has been done before) to evaluate the according loss savings of the VR *alone*, a system-level analysis including *both* converter stages has been missing so far. As the optimum operating mode selection (i.e., 3/3-PWM or 1/3-PWM) depends on the operating-point-dependent loss contributions of both stages, such an analysis can necessarily only be carried out for a specific system realization. Therefore, in this paper a built 10 kW charger is considered and straightforward but accurate and experimentally verified loss models are introduced for the VR and the DABCs (for which, in addition, a simplified modulation scheme is proposed). These then enable a comprehensive analysis of the optimum synergetic operation. Changing the operating mode from 3/3-PWM to 1/3-PWM gives efficiency improvements of up to about 2% for a large share of the operating points (power, output voltage). This is confirmed by running the two-stage system with 3/3-PWM and with 1/3-PWM for an output voltage of 500 V, whereby the full-load efficiency improves from 95.1% to 95.4%, respectively. Whereas a minor degradation of the mains current total harmonic distortion for 1/3-PWM must be accepted, conducted EMI pre-compliance tests confirm that changing from 3/3-PWM to 1/3-PWM operation does not necessitate significant changes of the EMI filter design. All in all, three-level VR front-ends and (cascaded) DABC isolation stages that are both realized with latest-generation 600 V GaN power transistors, and the advantageous synergetic operation of the two stages, are both very promising concepts for future highly efficient and ultra-compact EV charging solutions.

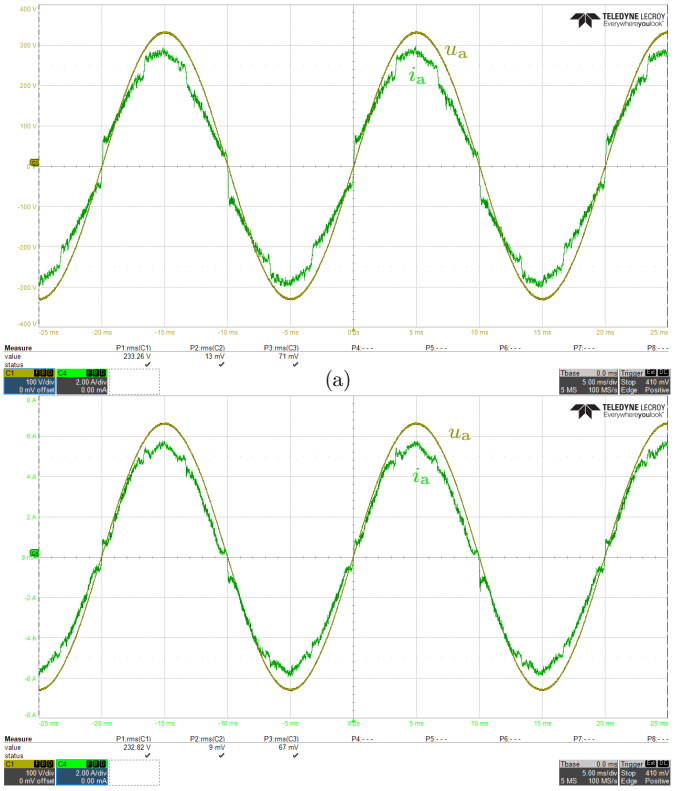

Fig. 20. Measured mains phase currents with 3/3-PWM and 2.5 kW output power, in **(a)** without and in **(b)** with the turn-off delay compensation activated.

TABLE IV
IMPROVEMENT OF MAINS CURRENT THD BY TURN-OFF DELAY COMPENSATION.

Power	Modulation	Uncompensated	Compensated
2.5 kW	3/3 PWM	7.3 %	4.2 % (-3.1 %)
	1/3 PWM	9.0 %	6.5 % (-2.5 %)
5 kW	3/3 PWM	4.2 %	3.8 % (-0.4 %)
	1/3 PWM	2.9 %	1.8 % (-1.1 %)

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APPENDIX
VR TURN-OFF DELAY COMPENSATION

Two of the main challenges of operating the VR with a high switching frequency of 560 kHz are the practical implementation of the current control and the modulation. The need for a fast current control loop requires an FPGA-based implementation as discussed in **Section VI**. However, the turn-off delay caused by the GaN transistor's parasitic capacitances, C_{oss}, has to be compensated for, particularly for duty cycles close to unity, to limit low-frequency current distortions.

As discussed in [53] for silicon superjunction (Si-SJ) MOSFETs, the challenge at higher switching frequencies (e.g., 560 kHz as opposed to 100 kHz) is that the *effective* duty cycle (i.e., the voltage-time area that is actually applied at the VR bridge-leg switch node) is distorted by the turn-on, and, particularly, the turn-off delays of the power semiconductors (in addition to the propagation delays of the gate drive and control signal isolation stages). This ultimately leads to an increase of the mains current THD. The turn-on of wide-bandgap (WBG) devices, assuming that the gate is driven by a strong gate driver and the gate loop PCB layout is adequate, can, in a first step, be assumed to have a much smaller effect than the device's turn-off process (considering also the missing turn-on of a complementary transistor in case of current commutation to a diode path). This is because the turn-off delay depends on the charge stored in the parasitic output capacitance, and, in particular, also on the switched current, i.e., it varies over the grid period as the phase current does.

Although for the same $R_{\mathrm{ds,on}}$, GaN devices feature a much more linear output capacitance and smaller output charge than their Si-SJ counterparts [54], [55], it is still necessary to adjust the duty cycles of the VR to compensate for the above-mentioned current-dependency of the turn-off delay and the thus introduced voltage-time area error. In the case at hand this is achieved by shortening the on-time of the switches by

$$t_{\mathrm{comp},i} = \min\left(50\,\mathrm{ns}, 50\,\mathrm{nsA}^2 \cdot i_i^{-2}\right), \tag{5}$$

where t_{comp} is the on-time compensation in nanoseconds, and i_i is the (measured) input current of phase i. As in [53], the equation parameters are obtained empirically.

Fig. 20 depicts measured mains current waveforms without and with turn-off delay compensation, which clearly show the reduction of the low-frequency distortions. This is reflected by a corresponding improvement in the mains current THD, as listed in **Tab. IV**. Note that the compensation is advantageous for both, operation with 3/3-PWM and with 1/3-PWM.

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