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Optimal Synergetic Control of Three-Phase/Level Boost-Buck Voltage DC-Link AC/DC Converter for Very-Wide Output Voltage Range High-Efficiency EV Charger

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***Abstract*—Universal high-power three-phase mains interfaces for electric vehicle (EV) charging must provide a wide output voltage range (e.g., 200 V to 800 V) and thus provide buck and boost capability. An advantageous realization combining a three-level (3-L) T-type (Vienna) boost-type PFC voltage-source rectifier (VSR) with a 3-L buck-type DC/DC converter stage is presented in this paper. For high output voltages (boost-mode), the VSR-stage operates with 3/3-PWM, i.e., continuous PWM of all three phases to regulate the output voltage while the DC/DC-stage remains clamped to avoid switching losses. For low output voltages (buck-mode), the DC/DC-stage advantageously controls the DC-link voltage according to a time-varying reference value, which allows to sinusoidally shape the currents of two mains phases, such that the VSR-stage can operate with 1/3-PWM (only one of the three bridge-legs operates with PWM at any given time) with reduced switching losses. This paper proposes a novel 2/3-PWM scheme for the output voltage transition region, where output voltages are between the buck-mode and the boost-mode. This enables loss-optimum operation (i.e., the minimum number of the VSR-stage bridge-legs operating with PWM, and with the minimum possible DC-link voltage) for any output voltage. Furthermore, this paper introduces a new synergetic control concept that ensures seamless transitions between the loss-optimum operating modes. A comprehensive experimental verification, including pre-compliance EMI measurements, using a 10-kW hardware demonstrator with a power density of 5.4 kW/dm^3 (91 W/in^3), a peak efficiency of 98.8% at rated power and 560 V output voltage, and >98% efficiency for all operating points with >400 V output voltage and more than about 50% of rated power, confirms the theoretical analyses.**

***Index Terms*—Electric Vehicle Chargers, Three-Phase Boost-Buck Voltage DC-Link PFC Rectifier, Three-Phase Bidirectional Vienna Rectifier, Synergetic Control, One-Third Pulse-Width Modulation, Optimal Two-Third Pulse-Width Modulation.**

I. Introduction

More efficient and compact EV battery chargers are key enablers for the transition from fossil-fuel-based to carbon-free road transportation by electric vehicles (EVs). This transition is an important element for achieving the net-zero CO_2 emission target set forth in the Paris Agreement before 2050 [1]. Typical high-power EV chargers include, first, a three-phase (3-Φ) power-factor-correcting (PFC) AC/DC rectifier stage and a subsequent DC/DC converter stage with high-frequency (HF) isolation (see **Fig. 1a**). The isolation stage provides voltage adaption and galvanic isolation, i.e., a large common-mode

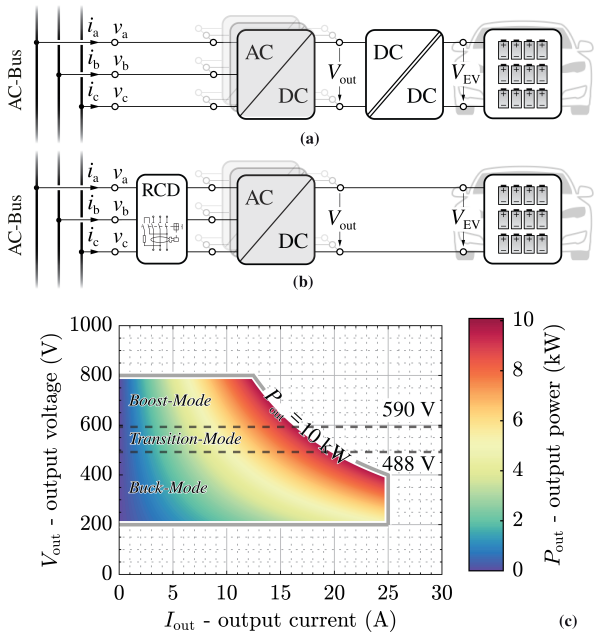

Fig. 1: (a) Typical two-stage EV charger architecture including a DC/DC stage with high-frequency (HF) isolation and constant voltage transfer ratio, i.e. a DC transformer (DCX, [4]–[6]). **(b)** Typical non-isolated EV charger architecture using residual current devices (RCDs) to ensure end-user safety. **(c)** Typical operating range of a 10 kW EV charger module [7], [8]; note the output current limit of $I_{out} = 25$ A.

(CM) impedance between the 3-Φ mains and the vehicle, which ensures electrical safety [2]. Recently, also extensive research has been carried out on non-isolated EV chargers (see **Fig. 1b**), where the ground leakage current is monitored by Residual Current Devices (RCDs) to guarantee end-user safety [3].

Universal DC fast chargers should support today's typical EV battery voltages of 200 V to 750 V [7]–[10]. To achieve high efficiency, often series resonant DC/DC converters with limited voltage regulation capability, i.e. DC transformers (DCX, [4], [5]) are employed [6]. Assuming a near-unity voltage conversion ratio, the AC/DC PFC rectifier front-end must cover a correspondingly wide output voltage range of 200 V to 800 V and/or the AC/DC front-end must incorporate buck-boost capability. The same is true for non-isolated

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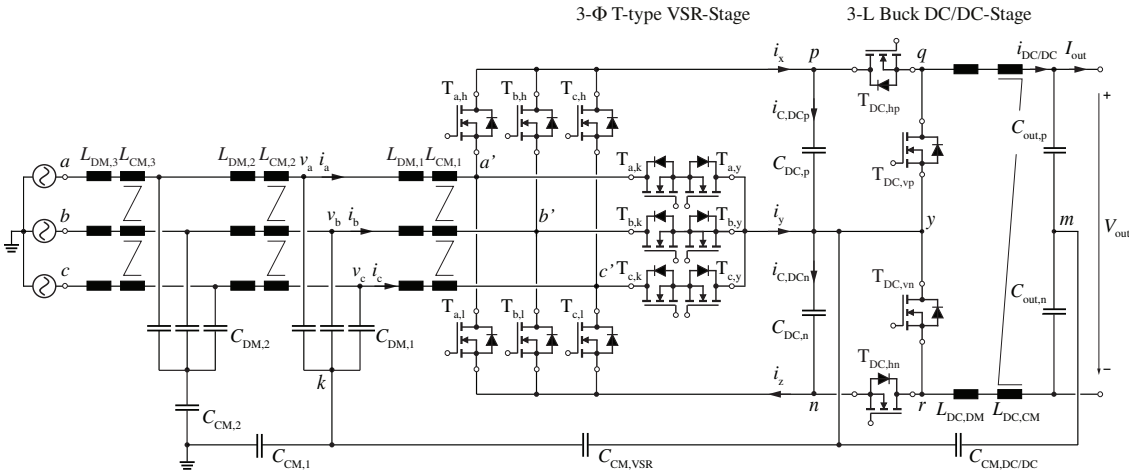

Fig. 2: Circuit schematic of the considered 10 kW three-phase (3-Φ) boost-buck (Bb) voltage DC-link PFC rectifier system including CM and DM EMI filter stage, which employs a 3-Φ three-level (3-L) T-type (Vienna) voltage source rectifier (VSR)-stage cascaded by a 3-L buck-type DC/DC-stage. To filter the common-mode (CM) noise at the DC-link and the DC output port, integrated CM filter capacitors, i.e, $C_{\text{CM,VSR}}$ and $C_{\text{CM,DC/DC}}$, are applied.

chargers. **Fig. 1c** shows the corresponding operating range of an exemplary 10 kW universal AC/DC EV charger module. Note that several such modules could be paralleled to realize higher output power levels, and that the concepts discussed throughout the article are likewise applicable to units with higher power ratings.

A three-level (3-L) realization of the 3-Φ AC/DC PFC rectifier stage facilitates small EMI filters and hence compact converter realizations [11]. In particular, the T-type (Vienna) voltage source rectifier (VSR)-stage [12], [13] is a widely used industry-standard solution [14]–[16]. To achieve boost-buck (Bb) functionality, the boost-type VSR-stage must be combined with a buck-type DC/DC stage (e.g., [17], [18]) as shown in **Fig. 2**, which again advantageously is realized as a 3-L structure to reduce the magnetics volume and to enable controllability of the VSR-stage DC-link midpoint potential.

The basic and/or conventional, decoupled operating regime of this two-stage system is as follows: For high output voltages (boost-mode), the VSR-stage switches all three bridge-legs with PWM (3/3-PWM) whereas the DC/DC-stage is clamped ($\text{T}_{\text{DC,hp}}$ and $\text{T}_{\text{DC,hn}}$ are always on), i.e., the VSR-stage directly controls the output voltage. Advantageously, the VSR-stage low-frequency (LF) common-mode (CM) voltage injection is selected as proposed in [19] to achieve zero local average (over a pulse period) mid-point current (ZMPC), i.e., $\bar{i}_y \approx 0$, which implies that two small DC-link capacitors are sufficient for high-frequency ripple filtering and that there is no need for large (electrolytic) capacitors as energy buffers.[1] As will be discussed later, such a decoupled operation requires a minimum DC-link voltage of $V_{\text{pn}} > 590\,\text{V}$ for a 400 V mains (if ZMPC is used), and typical DC-link voltage values would be $V_{\text{pn}} = 640\,\text{V}$ or $V_{\text{pn}} = 720\,\text{V}$, taking into account grid voltage fluctuations and some control margin. If the output voltage is lower, the DC/DC-stage must operate with PWM, too, to step-down the DC-link voltage accordingly.

However, recently extensive research has been conducted on a variable DC-link voltage modulation strategy, so-called 1/3-PWM[2]. Proposed in the early 2000 [26], [30], [31], for 2-L converters, the key idea is to utilize the DC/DC-stage for shaping the DC-link voltage such that two phases of the AC/DC rectifier can be clamped and only the remaining phase must operate with PWM; both stages together regulate the mains currents. This leads to a significant reduction of switching losses generated by the VSR-stage. 1/3-PWM has been analyzed mostly for 3-Φ two-stage systems with 2-L voltage DC-link front-ends [26]–[29], and [32]–[34] have described the operation of such systems, in the context of motor drive/photovoltaic inverter and EV charger applications, covering a wide output voltage range, i.e., with buck-boost functionality, emphasizing the advantages of 1/3-PWM for low output voltages and the seamless transition to 3/3-PWM for high output voltages.

For two-stage systems with 3-L AC/DC front-ends, there are even concepts that operate this front-end only as a mains-frequency commutated three-phase unfolder and use two DC/DC converters to shape the two DC-link voltages (i.e., v_{py} and v_{yn} in **Fig. 2**) such that ultimately sinusoidal grid currents result [35]–[37]. However, in this case, the two DC-link voltages vary widely and reach zero several times per mains period. Therefore, first, the two DC/DC stages are not utilized well as the power they process fluctuates correspondingly, and, second, they must provide boost and buck functionality. Therefore, this approach can not be adapted for the considered topology with a non-isolated buck-type DC/DC stage.

Alternatively, 1/3-PWM has also been suggested for 3-L NPC AC/DC front-ends combined with isolated DC/DC converters [38], or a combination of a 3-L ANPC front-end with a non-isolated 3-L DC/DC converter [39], and finally for a 3-L VSR-stage front-end with arbitrary (i.e., featuring buck

[1]Note that discontinuous PWM (DPWM) concepts [20]–[23] (which would allow one bridge-leg of the VSR-stage to be clamped) are not considered because these would lead to relatively high midpoint currents [19], [24], [25].

[2]Note that 1/3-PWM is sometimes also called space vector pulse-width amplitude modulation (SVPWAM) [26], 240CPWM [27], [28], or two-phase-clamped DPWM [29].

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and boost functionality and thus typically isolation) DC/DC converters in [8], which also shows the transition between 1/3-PWM and 3/3-PWM. However, all these studies are based on simulations only. A detailed analysis of the wide-output-voltage-range operation of the 3-Φ 3-L Bb voltage DC-link PFC rectifier system shown in **Fig. 2** is thus missing, especially considering the non-isolated buck-type DC/DC-stage where the input voltage can only be stepped down to a lower value but not also be boosted as would typically be feasible with isolated DC/DC-stages [8]. Note further that if isolated DC/DC converters (with buck-boost functionality enabling unconstrained selection of the DC-link voltage) are used, the decision on the optimum operating mode (i.e., 1/3-PWM or 3/3-PWM) is solely based on an optimization, e.g., for maximum efficiency. With non-isolated DC/DC buck converters as considered here, in contrast, for each output voltage a single loss-optimum operating mode with a defined DC-link voltage exists.

This paper therefore studies the loss-optimum operation of the converter shown in **Fig. 2**, considering the wide output voltage range of $200\,\mathrm{V}$ to $800\,\mathrm{V}$. Complementing a detailed discussion of the already mentioned 3/3-PWM (for the boost-mode) and 1/3-PWM (for the buck-mode), two new 2/3-PWM modulation methods for the transition-mode (see **Fig. 1c**) are proposed in **Section II**. Further, **Section III** introduces a synergetic control concept that ensures loss-optimum converter operation and seamless transitions between the three PWM variants. The proposed synergetic operating principle requires only three (out of five) half-bridges (HBs) to operate with PWM at any given point in time,[3] and the minimum possible DC-link voltage is used to ensure minimum switching losses. Furthermore, the DC-link capacitors are only needed for switching frequency ripple filtering but do not need to buffer low-frequency power fluctuations, which contributes to a compact realization. Thus, **Section IV** provides a detailed experimental verification, including efficiency and conducted EMI measurements, using a $10\,\mathrm{kW}$ hardware demonstrator with a peak efficiency of 98.8% at rated power and a power density of $5.4\,\mathrm{kW/L}$ ($91\,\mathrm{W/in^3}$), before **Section V** concludes the paper.

II. Operating Principle

The operating principle of the analyzed 3-Φ Bb voltage DC-link PFC rectifier system shown in **Fig. 2** is analyzed in this section, considering operation interfacing a $400\,\mathrm{V}$ mains with near-unity power factor. Advantageously, the following goals should be achieved for the full output voltage range of $200\,\mathrm{V}$ to $800\,\mathrm{V}$:

- A total of three HBs of the VSR-stage and the DC/DC-stage are operating with HF switching while the remaining two HBs are clamped, and the minimum possible DC-link voltage is used. This guarantees loss-optimum operation, i.e., minimum possible switching losses of the whole converter.
- LF currents in the DC-link capacitors are avoided and hence the DC-link capacitors are only needed to filter HF ripples; no bulky energy-buffering DC-link capacitors are needed. Note that 1/3-PWM in the buck-mode (see **Section II-B**) necessitates small DC-link capacitors to minimize the capacitive charging and discharging currents needed to control the DC-link voltage to the time-varying six-pulse shape.

Before discussing the most suitable operating modes for different output voltages, it is useful to first thoroughly explain and derive the range of the CM injection voltage v_{CM} that is available for the modulation of the VSR-stage. Considering Kirchhoff's Voltage Law and the VSR-stage front-end and $v_{\mathrm{CM}} = v_{\mathrm{ky}}$ (occurring across the CM filter capacitor $C_{\mathrm{CM,VSR}}$ as shown in **Fig. 2**, i.e., showing a continuous waveform) all three phases, at the same time, should follow $\bar{v}_{\mathrm{s'k}} + v_{\mathrm{CM}}$, with

$$-\frac{1}{2}V_{\mathrm{DC}} = V_{\mathrm{ny}} \leq \bar{v}_{\mathrm{s'k}} + v_{\mathrm{CM}} \leq V_{\mathrm{py}} = \frac{1}{2}V_{\mathrm{DC}}, \tag{1}$$

where $\mathrm{s} \in \{\mathrm{a}, \mathrm{b}, \mathrm{c}\}$ and $\bar{v}_{\mathrm{s'k}}$ is the local average DM voltage at the VSR-stage switching node; V_{DC} is the total DC-link voltage, i.e., $V_{\mathrm{DC}} = V_{\mathrm{py}} + V_{\mathrm{yn}}$. Then, assuming $v_{\mathrm{max}} = \max(\bar{v}_{\mathrm{s'k}})$ and $v_{\mathrm{min}} = \min(\bar{v}_{\mathrm{s'k}})$, the boundaries of v_{CM} can be derived as

$$-\frac{1}{2}V_{\mathrm{DC}} + |v_{\mathrm{min}}| \leq v_{\mathrm{CM}} \leq \frac{1}{2}V_{\mathrm{DC}} - v_{\mathrm{max}}, \tag{2}$$

which is as a general (time-varying) limitation of the injected CM voltage regardless of specific modulation schemes [23].[4]

A. Boost-Mode

If the output voltage is sufficiently (depending on the employed CM injection) higher than the peak value of the line-to-line voltages, the converter operates in the boost-mode: the VSR-stage uses 3/3-PWM, where all three HBs of the VSR-stage operate with HF PWM to ensure 3-Φ sinusoidal mains currents and step up the 3-Φ mains voltages to the higher DC output voltage such that the switches $\mathrm{T_{DC,hp}}$ and $\mathrm{T_{DC,hn}}$ of the DC/DC-stage are permanently on and do not contribute to switching losses. Thus, the DC-link voltage $V_{\mathrm{DC,3/3}}$ is simply equal to the output voltage V_{out}, which is the minimum possible DC-link voltage in this case.

3/3-PWM can be simply implemented without any CM injection, i.e., $v_{\mathrm{CM}} = 0\,\mathrm{V}$ as shown in **Fig. 3a**. However, this comes with two main drawbacks: **(i)** limited linear modulation range without over-modulation and **(ii)** large LF currents $\bar{i}_{\mathrm{C,DCp}}$ and $\bar{i}_{\mathrm{C,DCn}}$ (up to $4\,\mathrm{A}$) flow through the DC-link capacitors, which cause LF DC-link voltage variations (not shown in the figure). Such LF DC-link voltage variations increase the transistors' voltage stresses, lead to additional switching losses, and possibly cause LF distortions of the 3-Φ mains currents [40]–[45]. Importantly, such DC-link voltage variations are inversely proportional to the DC-link capacitance values,

[3]Note that this corresponds to the minimum of three degrees of freedom needed to control the total constant power flow (two mains currents to ensure PFC operation) and the power sharing between the two DC/DC-stage half-bridges (i.e., the DC-link midpoint potential).

[4]Note that conventional DPWM is achieved if one of the two equalities in (2) is attained. E.g., if $v_{\mathrm{CM}} = -1/2V_{\mathrm{DC}} + |v_{\mathrm{min}}|$, the switching node of the phase with the minimum voltage is connected to negative DC-link potential *n*, e.g., if $v_{\mathrm{min}} = \bar{v}_{\mathrm{a'y}}$, the switching node *a'* is connected to *n* by turning on $\mathrm{T_{a,l}}$. As mentioned above, DPWM would lead to relatively high LF midpoint currents (and hence LF currents in the DC-link capacitors) and is therefore not further considered.

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Fig. 3: Exemplary key waveforms for operating over a wide output voltage range, i.e., buck-boost operation, of the considered 3-Φ Bb voltage DC-link PFC rectifier system shown in **Fig. 2**. In the boost-mode, the VSR-stage operates with 3/3-PWM to ensure 3-Φ sinusoidal mains currents and regulate the output voltage. **(a)** 3/3-PWM can be implemented with zero LF CM injection, however, LF capacitive currents (up to 4 A) flow through the DC-link capacitors (note that the DC-link capacitors are replaced with ideal voltage sources such that these LF DC-link capacitor currents do not result in LF DC-link voltage variations). Thus, **(b)** another variety of 3/3-PWM with LF CM voltage injection that ensures zero mid-point current (ZMPC) [19] and hence zero LF DC-link capacitor currents is implemented. **(c)** In the buck-mode, the VSR-stage operates with 1/3-PWM [8], where the DC/DC-stage controls the DC-link voltage to follow the six-pulse shape of the upper envelope of the line-to-line voltage absolute values and hence only one of the VSR-stage's three HBs operates with HF PWM at any given time.

which must be small to allow 1/3-PWM in the buck-mode (see below). Therefore, 3/3-PWM with zero CM injection is discarded in this application.

Alternatively, as shown in [19], it is possible to inject a nonzero CM voltage such that the LF mid-point current $\bar{i}_y$ is zero and, as a result, zero LF currents flow through the DC-link capacitors (see **Fig. 3b**). The required LF CM injection voltage can be obtained by first considering the expression for the LF mid-point current $\bar{i}_y$ in dependence on the phase modulation indices and the phase currents as

$$\bar{i}_y = \sum_s \left(1 - \frac{|\bar{v}_{s'k} + v_{CM}|}{V_{DC}/2}\right) \cdot i_s, \tag{3}$$

where $s \in \{a, b, c\}$, and $i_s = G \cdot \bar{v}_{s'k}$ is the phase current of the 3-Φ mains assuming ohmic behavior with a conductance of G. Then, a zero mid-point current (ZMPC) is attained [19] if

$$\bar{i}_y = G \cdot \sum_s \left(1 - \frac{|\bar{v}_{s'k} + v_{CM}|}{V_{DC}/2}\right) \cdot \bar{v}_{s'k} = 0. \tag{4}$$

From that, the required LF CM voltage $v_{CM,3/3}$ can be calculated as

$$v_{CM,3/3} = v_{CM,ZMPC} = v_{mid} \cdot \left(1 - \frac{|v_{mid}|}{\max(|v_{min}|, |v_{max}|)}\right), \tag{5}$$

where v_{mid} is defined after sorting the 3-Φ mains voltages

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such that $v_{max} > v_{mid} > v_{min}$. Injecting $v_{CM,ZMPC}$ ensures zero midpoint current and hence removes the need for bulky DC-link capacitors as energy buffers even without operating the cascaded DC/DC-stage. Note that $v_{CM,ZMPC}$ always lies within the range defined in (2) without attaining either equality, i.e., without clamping any of the three phases. Note further that $v_{CM,ZMPC}$ does not depend on the DC-link voltage, so that the result from (2) is applicable to the 2/3-PWM-ZMPC method discussed below in **Section II-C**.

Therefore, considering a $400\,\mathrm{V}$ mains and (1), the converter operates in the boost-mode with 3/3-PWM when $V_{out} > 590\,\mathrm{V}$ (see **Fig. 3b**); unless otherwise noted, 3/3-PWM indicates using ZMPC third-harmonic injection. Note that the minimum DC-link voltage allowing 3/3-PWM-ZMPC is slightly larger than the theoretical boost-mode boundary of $\sqrt{3}\hat{V}_{in} = 563\,\mathrm{V}$ as stated in [46].

B. Buck-Mode

The converter operates in the buck-mode when $V_{out} < {}^{3}/_{2}\hat{V}_{in} = 488\,\mathrm{V}$ (see **Fig. 3c**) [46]. For such low output voltages, the DC/DC-stage *must* operate. Advantageously, however, the VSR-stage operates with 1/3-PWM where each phase only switches with PWM during one-third of the mains period (see $v_{a'y}$ in **Fig. 3c**), or in other words, two out of the three phases are clamped at all times. To still obtain 3-Φ sinusoidal mains currents, the two DC/DC-stage HBs have to regulate the DC-link voltage V_{DC} following the six-pulse shape of the envelope of the 3-Φ line-to-line mains voltage absolute values; this necessitates relatively small DC-link capacitors as otherwise excessive capacitive currents would occur. Importantly, no additional switching losses are generated since the DC/DC-stage anyway has to be operated to step down the DC-link voltage to a lower output voltage value.

The required time-varying DC-link voltage $V_{DC,1/3}$ can be derived from (2), i.e., if two phases are required to clamp, both equalities in (2) must be met and we have

$$V_{DC,1/3} = v_{max} - v_{min}. \tag{6}$$

The injected CM voltage $v_{CM,1/3}$ is

$$\begin{aligned} v_{CM,1/3} &= \frac{1}{2}V_{DC} - v_{max} = -\frac{1}{2}V_{DC} + |v_{min}| \\ &= -\frac{1}{2}(v_{max} - |v_{min}|). \end{aligned} \tag{7}$$

Therefore, the LF CM voltage for 1/3-PWM is fixed and not subject to choice (as for 3/3-PWM). Adding this LF CM injection signal to the voltage references of the VSR-stage modulator automatically ensures the desired clamping of the phases with the maximum and the minimum phase voltages and appropriate PWM of the third phase.

Even though the resulting LF mid-point current of the VSR-stage, $\bar{i}_y$, is not zero for 1/3-PWM (notice $i_x \neq -i_z$ in **Fig. 3c**), it is compensated by the cascaded DC/DC-stage that controls the DC-link voltage; this again ensures essentially zero (neglecting the very small current needed to shape the DC-link voltage) LF capacitor current (see $\bar{i}_{C,DCp} = \bar{i}_{C,DCn} = 0$ in **Fig. 3c**).

C. Transition-Mode

Whereas for both, boost-mode and buck-mode operation the stated goals (only three HBs switching, minimum DC-link voltage, no LF currents in the DC-link capacitors) are achieved by the described conventional methods, this is not the case in the transition-mode, i.e., when $488\,\mathrm{V} < V_{out} < 590\,\mathrm{V}$ (for a $400\,\mathrm{V}$ mains). The state-of-the-art transition-mode operation employs a time-varying DC-link voltage $V_{DC} = \max(V_{out}, V_{DC,1/3})$ for a direct change from 3/3-PWM to 1/3-PWM, see **Fig. 4a**. This approach has been analyzed and implemented for 2-L voltage-source front-ends [34] or 3-L front-ends but with (two) cascaded isolated *buck-boost* DC/DC converters [8]. For these cases, this straightforward approach to handling the transition-mode is feasible since either no mid-point current can occur (2-L front-end) or isolated DC/DC-stages provide full buck-boost functionality.

However, in contrast to two-stage systems with isolated DC/DC-stages [8], here only buck, i.e., step-down, functionality can be achieved by the DC/DC-stage. Therefore, the time-varying VSR-stage DC-rail currents $\bar{i}_x$ *and* $\bar{i}_z$ cannot be larger than the DC/DC-stage inductor current $i_{DC/DC}$ (see **Fig. 2**) to avoid LF current flows in the DC-link capacitors and corresponding voltage variation (remember that the DC-link capacitors must be comparably small for 1/3-PWM operation). Considering **Fig. 4a**, note that the converter operates with 1/3-PWM in interval ① and with 3/3-PWM in interval ③, where in both cases the LF DC-link capacitor currents actually *are* zero. However, the state-of-the-art transition-mode operation cannot satisfy the requirement during the highlighted (pink) interval ②, where, e.g., $\bar{i}_x$ is larger than $i_{DC/DC}$, and this current difference (shaded) corresponds to $\bar{i}_{C,DCp}$ flowing through the top DC-link capacitor. These DC-link capacitor currents not only contain LF components but even a DC offset, which implies that practical realizations of the considered topology with finite capacitance DC-link capacitors (note that the DC-link capacitors are replaced in **Fig. 4a** with ideal voltage sources for illustrative purposes) could not operate in this mode. There is thus a need to find alternative modulation schemes for the transition-mode, which do not cause such LF DC-link capacitor currents; two different options are proposed in the following.

The first possible solution is an extension of 3/3-PWM-ZMPC to the 2/3-PWM-ZMPC (see **Fig. 4b**), where the time-varying DC-link voltage allows always to clamp one of the VSR-stage's three phases (the two others are operating with PWM, hence 2/3-PWM). The injected CM voltage is calculated as in (5) to ensure zero midpoint current even during 2/3-PWM operation. Then, the DC-link voltage $V_{DC,ZMPC}$ for 2/3-PWM-ZMPC can be derived from (2) when only one equality is attained as

$$V_{DC,ZMPC} = 2 \cdot \max(-v_{min} - v_{CM,ZMPC}, v_{max} + v_{CM,ZMPC}). \tag{8}$$

The DC-link voltage waveform consists of two sections, i.e., 3/3-PWM ($V_{DC} = V_{out}$) is applied while the output voltage defines the minimum DC-link voltage, and $V_{DC} = V_{DC,ZMPC}$ ensures 2/3-PWM operation of the VSR-stage but *both* DC/DC-

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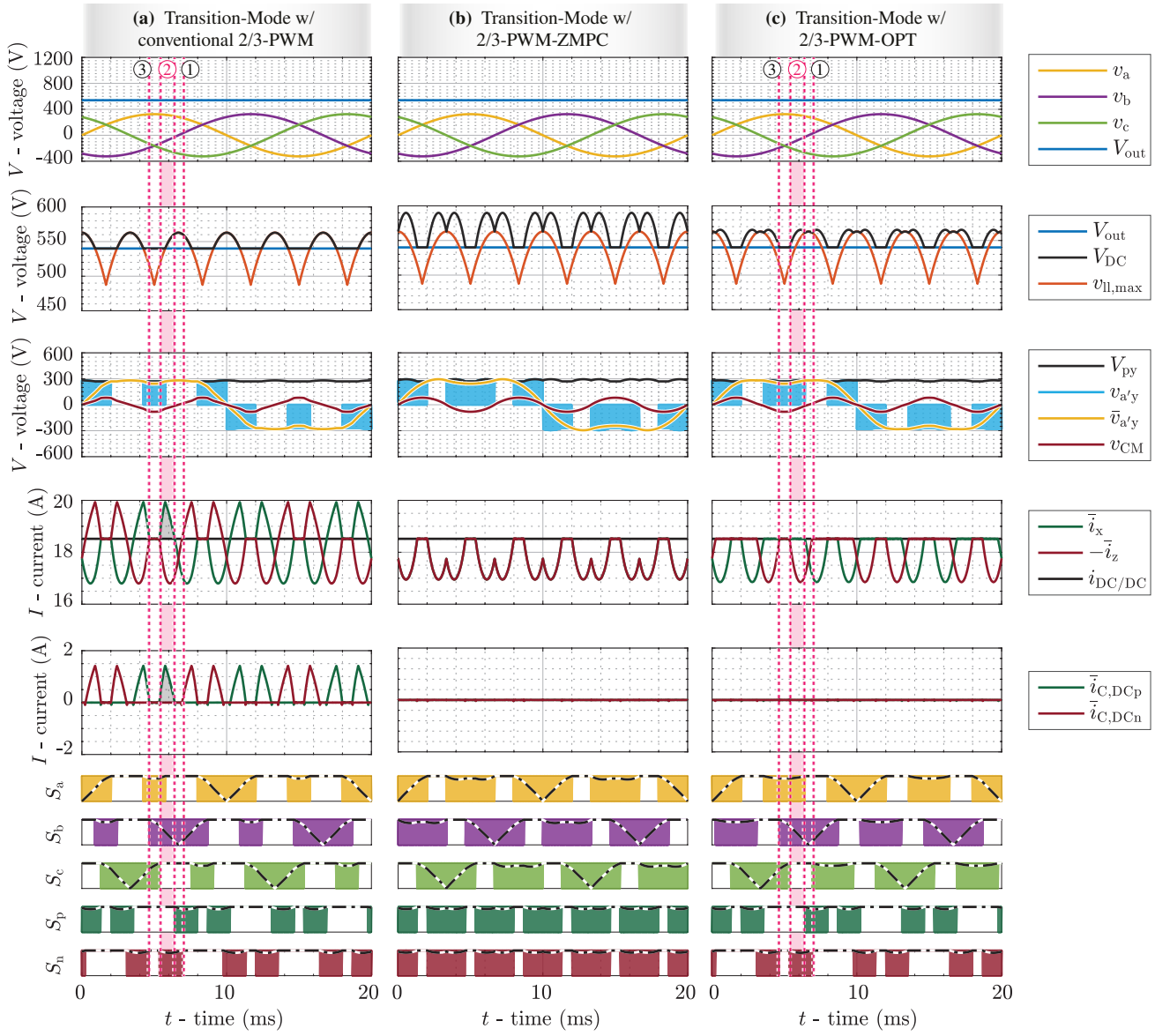

Fig. 4: Exemplary key waveforms for operation in the transition-mode at $V_{out} = 540\,\mathrm{V}$, considering different modulation schemes. **(a)** Conventional 2/3-PWM with $V_{DC} = \max(V_{out}, V_{DC,1/3})$ uses 3/3-PWM in interval ③ and 1/3-PWM in interval 3/3-PWM ①, but the resulting 2/3-PWM in interval ② generates LF currents in the DC-link capacitors (note that here again the DC-link capacitors are replaced with ideal voltage sources such that these LF DC-link capacitor currents do not result in LF DC-link voltage variations) if the DC/DC-stage does not provide buck-boost functionality as in [8]. **(b)** The proposed 2/3-PWM-ZMPC achieves zero LF current in the capacitors but requires PWM-operation of a total of four HBs and a higher-than-necessary DC-link voltage. **(c)** Proposed loss-optimum 2/3-PWM-OPT with adapted DC-link voltage shape (derivations in the text) that results again in 3/3-PWM in interval ③, 1/3-PWM in interval ①, and, advantageously, also only three HBs switching in interval ② as well as minimum possible DC-link voltage.

stage HBs have to operate with PWM (and equal duty cycles) to shape the DC-link voltage accordingly. Consequently, there are time intervals where a total of four HBs operate with PWM—one more than needed, given that the three degrees of freedom that must be controlled remain the same. Hence, 2/3-PWM-ZMPC cannot yet be the loss-optimum operating mode for the transition region.

To arrive at the second proposed solution, it is useful to first reconsider that the state-of-the-art transition-mode operation (see **Fig. 4a**) employs 3/3-PWM during interval ③ and 1/3-PWM during interval ①, and only the highlighted interval ② (pink) is problematic due to LF currents through the DC-link capacitors. Therefore, a second modulation scheme, 2/3-PWM-OPT (see **Fig. 4c**), is proposed for the highlighted interval ② (pink), which ensures that also the transition-mode does never require more than three PWM-operated bridge-legs. Generally speaking, compared to **Fig. 4a**, in interval ② a higher DC-link voltage is necessary to reduce $\overline{i}_x$ such that it is equal or smaller than $i_{DC/DC}$. Equality is preferred in this case such that the upper HB of the DC/DC-stage doesn't have to operate to compensate the current difference between $\overline{i}_x$ and $i_{DC/DC}$.

The operating principle of 2/3-PWM-OPT is explained in detail focusing on the highlighted interval ② (pink) in **Fig. 4c** (note that an analogous consideration can be made for $\overline{i}_z$ and the lower DC/DC-stage HB for intervals where the conven-

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tional transition-mode operation would result in $\bar{i}_z > i_{DC/DC}$). In this exemplary interval, only the phase voltage v_a, i.e., the maximum absolute phase voltage, is positive and the switch-node potential *a'* is alternatively connected to potentials *p* and *y*. By doing so, the phase current i_a can be modulated such that $\bar{i}_x = i_{DC/DC}$ and hence the upper DC/DC-stage HB can be clamped (see S_p), i.e., $T_{DC,hp}$ is permanently on, to save switching losses generated in the DC/DC-stage. The phase with the middle voltage v_{mid}, i.e., phase *b* in this interval, always has to be operated with PWM to ensure 3-Φ sinusoidal mains currents (similar to 1/3-PWM), but the third phase (the phase with the minimum voltage v_{min}, i.e., here phase *c*) can be clamped to the negative DC-link rail. However, because then $\bar{i}_z$ equals the phase current of phase c, we have $\bar{i}_z \neq i_{DC/DC} = \bar{i}_x$ and therefore the lower HB of the DC/DC-stage must operate with PWM to adapt $\bar{i}_z$ to $i_{DC/DC}$. Thus, two out of the three VSR-stage HBs, i.e., those connected to the phase with the maximum voltage v_{max} and the phase with the middle voltage v_{mid}, and the lower HB of the DC/DC-stage (see S_n), i.e., three HBs in total, are operating with PWM in interval ②. The VSR bridge-leg corresponding to the phase with the minimum voltage (see S_c) and the upper HB of the DC/DC-stage (see S_p) are clamped as shown in **Fig. 4c**. Furthermore, compared to the 2/3-PWM-ZMPC discussed above, a lower DC-link voltage is used.

To obtain an expression for the DC-link voltage needed to realize the advantageous 2/3-PWM-OPT, first consider that a CM voltage $v_{CM,OPT}$ has to be injected to ensure that the VSR modulator clamps the phase with the minimum v_{min} voltage, e.g., phase *c* in the considered example, to the negative DC-link rail:

$$v_{CM,OPT} = -\frac{V_{DC,OPT}}{2} + |v_{min}|. \tag{9}$$

The duty cycle of the phase with the maximum v_{max} voltage, e.g., phase *a*, considering the forward voltage conversion and the backward current conversion ($i_{DC/DC} = I_{out}$ due to negligible HF components), can be written as

$$d_{max} = \frac{v_{max} + v_{CM,OPT}}{\frac{V_{DC,OPT}}{2}} = \frac{i_{DC/DC}}{i_{max}} = \frac{I_{out}}{i_{max}}, \tag{10}$$

and the DC-link voltage $V_{DC,OPT}$ can be calculated by inserting (9) into (10) as

$$V_{DC,OPT} = 2 \cdot \frac{v_{max} - v_{min}}{1 + \frac{I_{out}}{i_{max}}}. \tag{11}$$

Until now, only the case where $|v_{max}| > |v_{min}|$ and hence the clamping of the phase with v_{min} is considered. Similarly, considering also the case $|v_{min}| > |v_{max}|$ where, by analogy, the phase with v_{max} should clamp, the general expression for the DC-link voltage $V_{DC,OPT}$ becomes

$$V_{DC,OPT} = 2 \cdot \frac{v_{max} - v_{min}}{1 + \frac{I_{out}}{\max(|i_{max}|, |i_{min}|)}}. \tag{12}$$

Finally, in the optimum transition-mode operation, the time-varying DC-link voltage (see **Fig. 4c**) consists of three sections, i.e., ③ $V_{DC} = V_{out}$ (3/3-PWM), ② $V_{DC} = V_{DC,OPT}$ (2/3-PWM-OPT), and ① $V_{DC} = V_{DC,1/3}$ (1/3-PWM), which guarantees a *true* seamless transition between the buck-mode and boost-mode.

The proposed 2/3-PWM-OPT completes thus the wide-range loss-optimal operation of the analyzed converter from **Fig. 2**:

- Three HBs of the VSR-stage and the DC/DC-stage are switching in total regardless of the operating mode, which is the minimum number of required active HBs.
- The minimum required DC-link voltage, i.e., the minimum switched voltage, is always employed.
- Furthermore, there are no LF currents in the DC-link capacitors.

Note that the conduction losses in a first step solely depend on the system operating points but not the modulation schemes. Thus, the proposed modulation schemes for buck-, boost-, and transition-modes ensure the minimum switching losses of the VSR-stage and the DC/DC-stage, and hence overall loss-optimum operation can be achieved for any operating point by a suitable synergetic control strategy.

III. Synergetic Control Strategy

The proposed synergetic control strategy (see **Fig. 5**, based on generic cascaded-loop control strategy from [47], [48]) ensures a collaborative operation of the VSR-stage and the DC/DC-stage such that the converter always operates in the loss-optimum mode for a given operating point and transitions seamlessly between modes, i.e., boost or buck operation in case of changing operating points. The control system is explained in detail in the following subsections.

A. Output Voltage Control & Mains Current Control

The outermost control loop tracks the output voltage reference V_{out}^* by calculating the corresponding output power reference P_{out}^*, which is used to generate the VSR-stage input reference conductance G^*. The 3-Φ sinusoidal mains current references i_a^*, i_b^*, and i_c^* that are proportional to the corresponding measured 3-Φ input voltages v_a, v_b, and v_c, i.e., ensure purely ohmic operation, directly follow. The 3-Φ mains current errors, resulting from the subtraction of the references from the measured 3-Φ mains currents (boost inductor currents), are fed into the mains current controller to calculate the needed 3-Φ input inductor voltages v_{La}^*, v_{Lb}^*, and v_{Lc}^*. Subtracting these calculated 3-Φ inductor voltage references from the measured 3-Φ input voltages (mains voltage feedforward) sets the 3-Φ VSR-stage voltage references v_a^*, v_b^*, and v_c^*.

B. DC-Link Voltage Reference Generation

The DC-link voltage reference generation block first selects the maximum v_{max}^* and the minimum v_{min}^* of the 3-Φ VSR-stage voltage references, which are used to calculate the time-varying DC-link voltage reference $V_{1/3}^*$, i.e., the upper envelope of the absolute value of the 3-Φ VSR-stage voltage references (see **Fig. 3c**), for 1/3-PWM in buck-mode operation [8]. The DC-link voltage reference for 3/3-PWM operation simply

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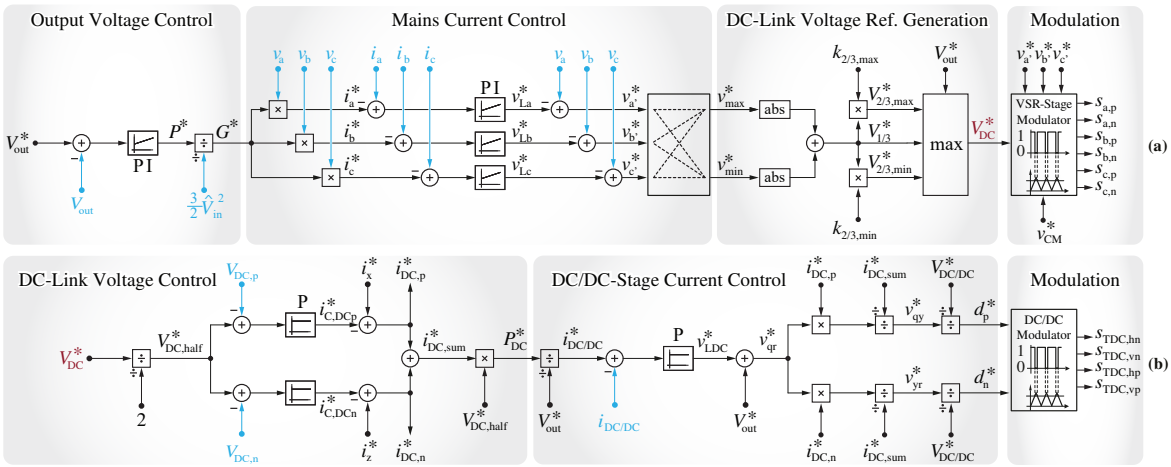

Fig. 5: Proposed synergetic control strategy block diagram for the 3-Φ Bb voltage DC-link PFC rectifier system shown in **Fig. 2**. **(a)** The VSR-stage controller achieves closed-loop DC output voltage control, ensures 3-Φ sinusoidal-shape mains currents, derives required DC-link voltage V_{DC}^* for wide-range loss-optimal operation and generates the VSR-stage gating signals. **(b)** The DC/DC-stage controller achieves closed-loop DC-link voltage V_{DC} and DC/DC-stage inductor current $i_{\mathrm{DC/DC}}$ controls, and ensures proper clamping of zero, one, or both HBs according to different operating modes and modulation schemes.

equals the constant output voltage reference V_{out}^* due to the clamping of the DC/DC-stage (see **Fig. 3b**). During 3/3-PWM operation, the VSR-stage alone ensures 3-Φ sinusoidal mains currents; however, with 1/3-PWM, the 3-Φ mains currents are controlled by both, the VSR-stage (directly by the only switching bridge-leg) and the DC/DC-stage (indirectly by the impressed six-pulse-shaped DC-link voltage according to $V_{1/3}^*$).

The DC-link voltage reference $V_{2/3}^* = V_{\mathrm{DC,OPT}}$ in (12) for the new 2/3-PWM-OPT can be formulated as a function of voltages instead of currents for simpler control implementation by substituting $I_{\mathrm{out}}^* = {}^{P_{\mathrm{out}}^*}/_{V_{\mathrm{out}}^*}$ and

$$i_{\mathrm{max}}^* = G^* \cdot v_{\mathrm{max}}^* = \frac{P_{\mathrm{out}}^*}{{}^3/_2 \cdot \hat{V}_{\mathrm{in}}^2} \cdot v_{\mathrm{max}}^*, \tag{13}$$

$$i_{\mathrm{min}}^* = G^* \cdot v_{\mathrm{min}}^* = \frac{P_{\mathrm{out}}^*}{{}^3/_2 \cdot \hat{V}_{\mathrm{in}}^2} \cdot v_{\mathrm{min}}^* \tag{14}$$

to finally obtain

$$\begin{aligned} V_{2/3}^* &= \max(V_{2/3,\mathrm{max}}^*, V_{2/3,\mathrm{min}}^*) \\ &= \max(k_{2/3,\mathrm{max}}, k_{2/3,\mathrm{min}}) \cdot V_{1/3}^* \end{aligned} \tag{15}$$

where

$$k_{2/3,\mathrm{max}} = \frac{2}{1 + \frac{{}^3/_2 \cdot \hat{V}_{\mathrm{in}}^2}{V_{\mathrm{out}}^* \cdot |v_{\mathrm{max}}^*|}} \quad \text{and} \quad k_{2/3,\mathrm{min}} = \frac{2}{1 + \frac{{}^3/_2 \cdot \hat{V}_{\mathrm{in}}^2}{V_{\mathrm{out}}^* \cdot |v_{\mathrm{min}}^*|}}. \tag{16}$$

This guarantees again that only the minimum number of HBs are switching in the transition-mode.

The final DC-link voltage reference V_{DC}^*

$$V_{\mathrm{DC}}^* = \max(V_{1/3}^*, V_{2/3,\mathrm{max}}^*, V_{2/3,\mathrm{min}}^*, V_{\mathrm{out}}^*) \tag{17}$$

then guarantees seamless and smooth transitions between different operating modes and modulation schemes over a wide output voltage range. The corresponding injected CM voltage can then be calculated based on (2) and (5) as

$$v_{\mathrm{CM}}^* = \max(\min(V_{\mathrm{CM,3/3}}^*, \frac{1}{2}V_{\mathrm{DC}}^* - v_{\mathrm{max}}), -\frac{1}{2}V_{\mathrm{DC}}^* - v_{\mathrm{min}}). \tag{18}$$

Therefore, the duty cycles of the VSR-stage bridge-legs can be determined, e.g., considering phase a, as

$$d_{\mathrm{a}}^* = \frac{v_{\mathrm{a}}^* + v_{\mathrm{CM}}^*}{\frac{1}{2}V_{\mathrm{DC}}^*}. \tag{19}$$

Note that $d_{\mathrm{a}}^* = 1$ is automatically attained whenever possible when operating with 1/3-PWM and 2/3-PWM-OPT as a result of selecting V_{DC}^* and v_{CM}^* as defined above, i.e., each bridge-leg is clamped whenever possible, resulting in minimum VSR-stage switching losses.

C. DC-Link Voltage Control

The DC-link voltage has to be regulated by the DC/DC-stage in the buck-mode (with 1/3-PWM) and transition-mode (with 2/3-PWM-OPT) operation, which is implemented in the *DC-Link Voltage Control* block shown in **Fig. 5**. The voltage error between half of the DC-link voltage $V_{\mathrm{DC,half}}^*$ and the measured upper DC-link capacitor voltage $V_{\mathrm{DC,p}}$ is fed into a P-controller [5] defining the upper DC-link capacitive current reference $i_{\mathrm{C,DCp}}^*$. The LF input current reference $i_{\mathrm{DC,p}}^*$ of the DC/DC-stage upper HB is specified by $i_{\mathrm{C,DCp}}^*$ and the LF current i_{x}^* in the VSR-stage's upper DC rail, which can be calculated with the information of the measured 3-Φ boost inductor currents and the duty cycles. The same logic is applied to the lower DC/DC-stage HB to derive $i_{\mathrm{DC,n}}^*$. Thus, the input power reference P_{DC}^*, the upper input current reference $i_{\mathrm{DC,p}}^*$ and the lower input current reference $i_{\mathrm{DC,n}}^*$ of the DC/DC-stage are forwarded to the following *DC/DC-Stage Current Control* block.

D. DC/DC-Stage Current Control

The buck-inductor current reference $i_{\mathrm{DC/DC}}^*$, set by P_{DC}^* and V_{out}^*, is compared with the measured value $i_{\mathrm{DC/DC}}$ to determine the required voltage v_{LDC}^* over the DC/DC-stage buck inductor.

[5] A P-controller is implemented to avoid a runaway of the voltage error integral if operating with 3/3-PWM and the clamped DC/DC-stage. A PI-controller with an anti-windup functionality is also feasible.

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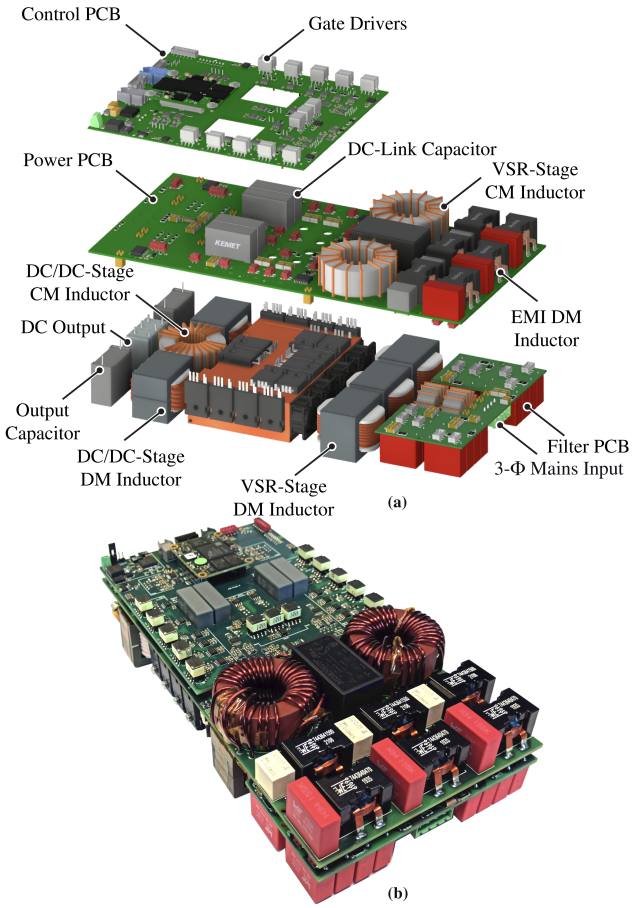

Fig. 6: **(a)** Exploded view and **(b)** photo of the realized 10 kW hardware demonstrator with a power density of 5.4 kW/L (91 W/in^3) and dimensions of 250 × 130 × 57 mm^3 (9.8 × 5.1 × 2.2 in^3), featuring the power circuit shown in **Fig. 2**. The demonstrator operates from the 400 V 3-Φ mains and provides a wide output voltage of 200 V to 800 V. The maximum output current is limited to 25 A.

The sum of v^*_{LDC} and V^*_{out} (output voltage feedforward) leads to the output voltage reference v^*_{qr} of the DC/DC-stage, which needs to be realized by both DC/DC-stage HBs together. Thus, v^*_{qr} is distributed to the two HBs according to the power ratio between the upper and lower HBs; since $V_{\mathrm{DC,p}} = V_{\mathrm{DC,n}}$, the power ratio equals the ratio between $i^*_{\mathrm{DC,p}}$ and $i^*_{\mathrm{DC,n}}$. From that, the output voltage reference v^*_{qy} for the upper HB and v^*_{yr} for the lower HB result. Then, the duty cycles are given by

$$d^*_{\mathrm{p}} = \frac{v^*_{\mathrm{qy}}}{V^*_{\mathrm{DC/DC}}} \quad \text{and} \quad d^*_{\mathrm{n}} = \frac{v^*_{\mathrm{yr}}}{V^*_{\mathrm{DC/DC}}}, \tag{20}$$

where

$$V^*_{\mathrm{DC/DC}} = \frac{1}{2}\max(V^*_{2/3,\mathrm{max}}, V^*_{2/3,\mathrm{min}}, V^*_{1/3}). \tag{21}$$

Note that (20) automatically ensures optimal clamping of both HBs in the different operating modes:

- In the buck-mode ($V^*_{\mathrm{out}} < 488\,\mathrm{V}$), $V^*_{\mathrm{DC/DC}} = {}^1\!/_2 V^*_{1/3}$ since $\max(k_{2/3,\mathrm{max}}, k_{2/3,\mathrm{min}}) < 1$ is always attained[6] and hence $V^*_{2/3,\mathrm{max}} < V^*_{1/3}$ and $V^*_{2/3,\mathrm{min}} < V^*_{1/3}$. Both DC/DC-stage HBs are switching to regulate the DC-link voltage into the required six-pulse shape.
- In the boost-mode, if neglecting v^*_{LDC}, $V^*_{\mathrm{out}} > 590\,\mathrm{V}$ leads to $v^*_{\mathrm{qy}} = v^*_{\mathrm{yr}} = {}^1\!/_2 V^*_{\mathrm{out}} \geq V^*_{\mathrm{DC/DC}} = {}^1\!/_2 \max(V^*_{2/3,\mathrm{max}}, V^*_{2/3,\mathrm{min}})$. Thus, $\mathrm{T}_{\mathrm{DC,hp}}$ and $\mathrm{T}_{\mathrm{DC,hn}}$ of the DC/DC-stage are permanently on since d^*_{p} and d^*_{n} are always larger than unity and saturate the corresponding modulator.
- In the transition-mode ($488\,\mathrm{V} < V^*_{\mathrm{out}} < 590\,\mathrm{V}$), when operating in 2/3-PWM-OPT and $|v_{\mathrm{max}}| > |v_{\mathrm{min}}|$, the upper DC/DC-stage HB should be clamped (see highlighted interval ② in **Fig. 4c**). Neglecting v^*_{LDC} and $i^*_{\mathrm{DC,p}}$, $v^*_{\mathrm{qy}} = {}^1\!/_2\, V^*_{2/3,\mathrm{max}} = V^*_{\mathrm{DC/DC}}$ and $v^*_{\mathrm{yr}} < V^*_{\mathrm{DC/DC}}$, such that the upper HB is permanently conducting ($d^*_{\mathrm{p}} = 1$) and the lower HB is switching ($d^*_{\mathrm{n}} < 1$).[7]

[6] $\max(k_{2/3,\mathrm{max}}, k_{2/3,\mathrm{min}}) \leq \dfrac{2}{1 + \frac{3/2 \cdot \hat{V}^2_{\mathrm{in}}}{V^*_{\mathrm{out}} \cdot \hat{V}_{\mathrm{in}}}} = \dfrac{2V^*_{\mathrm{out}}}{V^*_{\mathrm{out}} + 3/2\hat{V}_{\mathrm{in}}} < 1$ during the buck-mode operation because of $V^*_{\mathrm{out}} < 3/2\hat{V}_{\mathrm{in}}$.

TABLE I: Demonstrator system specifications and list of the main components; the EMI filter component values are listed in **TABLE II**.

	Description	Value
V_{in}	RMS phase voltage	230 V
V_{out}	DC output voltage range	200 V ∼ 800 V
P_{out}	Rated output power	10 kW
$I_{\mathrm{out,max}}$	Output current limit	25 A ($V_{\mathrm{out}} < 400$ V)
$\mathrm{T}_{\mathrm{VSR}}$	VSR-stage semicond. $\mathrm{T}_{\mathrm{h\{1\}}}$	C3M0016120K, 1200 V, 16 mΩ
	VSR-stage semicond. $\mathrm{T}_{\mathrm{k\{y\}}}$	C3M0030090K, 900 V, 30 mΩ
f_{VSR}	VSR-stage sw. freq.	100 kHz
$\mathrm{T}_{\mathrm{DC/DC}}$	DC/DC-stage semicond.	C3M0010090K, 900 V, 10 mΩ
$f_{\mathrm{DC/DC}}$	DC/DC-stage sw. freq.	200 kHz
C_{DC}	DC-link cap.	2×6.6 µF
C_{out}	Output cap.	2×5 µF
$L_{\mathrm{DM,1}}$	Main input DM ind.	3×194 µH (2×KoolMu60 E43/17, 25 turns)
$L_{\mathrm{CM,1}}$	Main input CM ind.	4.6 mH (2×VAC 45/30/15, 12 turns)
$L_{\mathrm{DC,DM}}$	Output DM ind.	2×34 µH (2×N87 E40/16/12, 11 turns)
$L_{\mathrm{DC,CM}}$	Output CM ind.	2.6 mH (VAC 40/25/15, 10 turns)
$C_{\mathrm{CM,VSR}}$	VSR-stage CM cap.	40 nF
$C_{\mathrm{CM,DC/DC}}$	DC/DC-stage CM cap.	40 nF

IV. Hardware and Experimental Verification

A hardware demonstrator is built to experimentally verify the proposed synergetic control structure over the wide output voltage operating range under different modulation schemes. Significant power efficiency improvements are observed by implementing 1/3-PWM in the buck-mode and the new 2/3-PWM-OPT in the transition-mode. Furthermore, conducted EMI noise emission measurements are provided.

A. Hardware Demonstrator

Fig. 6 shows the 10 kW hardware demonstrator of the analyzed 3-Φ Bb voltage DC-link PFC rectifier system and

[7] $v^*_{\mathrm{qy}} = i^*_{\mathrm{x}}/(i^*_{\mathrm{x}} + i^*_{\mathrm{z}})\, V^*_{\mathrm{out}} = V^*_{\mathrm{DC/DC}}$ considering $i^*_{\mathrm{x}} = I^*_{\mathrm{out}}$ and $i^*_{\mathrm{z}} = (V^*_{\mathrm{out}} - V^*_{\mathrm{DC/DC}})/V^*_{\mathrm{DC/DC}}\, I^*_{\mathrm{out}}$ during the highlighted interval when 2/3-PWM is applied.

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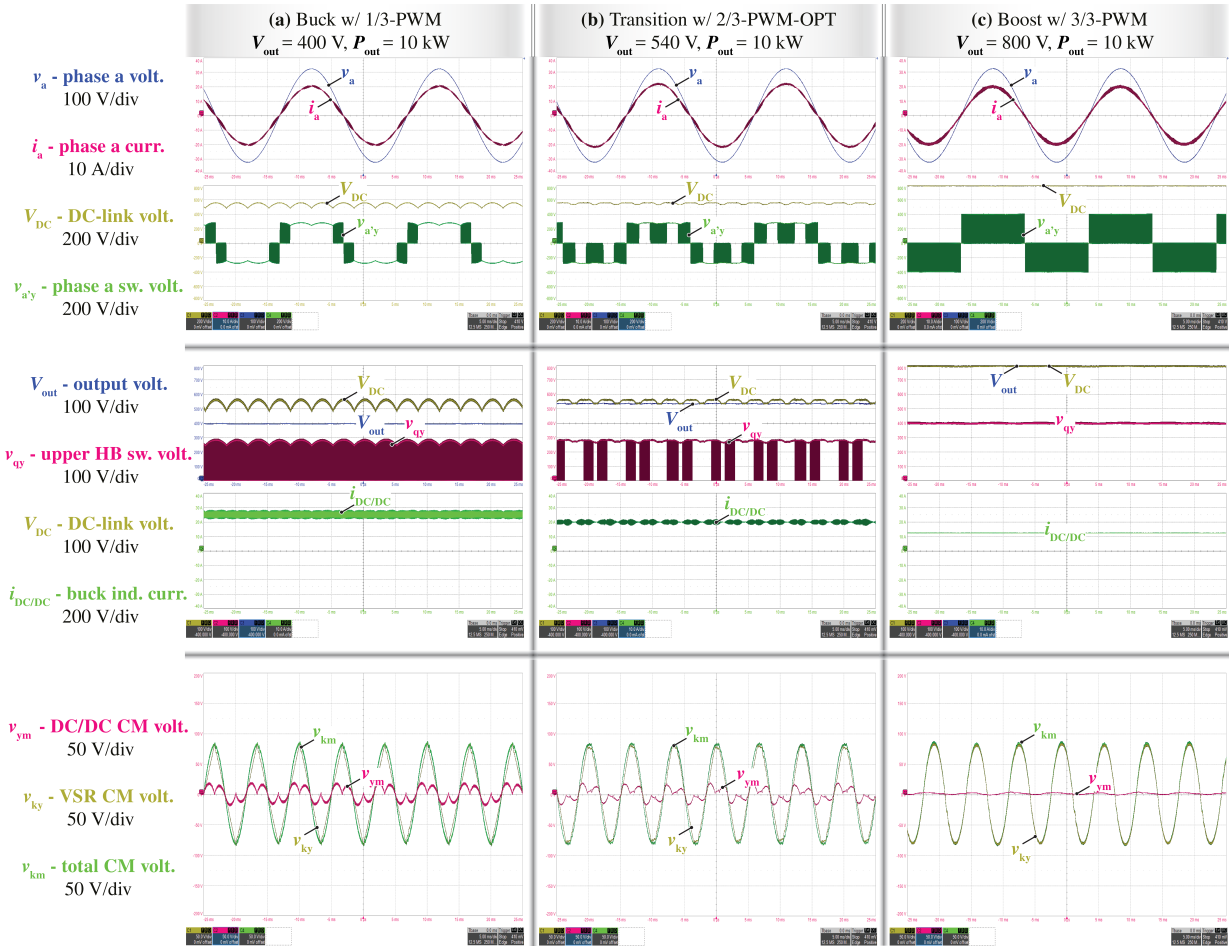

Fig. 7: Experimental waveforms of the converter shown in **Fig. 2** with the proposed synergetic control strategy when operating in **(a)** ***buck-mode***, **(b)** ***transition-mode*** and **(c)** ***boost-mode*** at 10 kW nominal output power. In the ***buck-mode*** operation, the DC/DC-stage regulates the DC-link voltage V_{DC} to the six-pulse shape to facilitate 1/3-PWM of the VSR-stage where only one phase is switching at any given time (see the switched voltage of phase a, $v_{\mathrm{a'y}}$). In the ***transition-mode***, the proposed 2/3-PWM-OPT is applied to ensure not only the automatic and seamless transition between buck- and boost-modes, but also guarantee loss-optimal operation, i.e., only three HBs are switching at any given time. Finally, 3/3-PWM is applied in the VSR-stage during the boost-mode operation while the DC/DC-stage is clamped ($\mathrm{T_{DC,hp}}$ and $\mathrm{T_{DC,hn}}$ are permanently on to avoid switching losses).

its exploded view. The prototype achieves a high power density of 5.4 kW/L (91 $\mathrm{W/in^3}$). The realized demonstrator is composed of three separate PCBs, including a 6-layer control PCB (FPGA, gate drivers, measurement data acquisition, etc.), an 8-layer power PCB carrying the main power converter components, and a 4-layer EMI Filter PCB. The system specifications and key components are listed in **TABLE I**.

B. Experimental Waveforms

Fig. 7 shows measured key waveforms of the 10 kW hardware demonstrator for the three different loss-optimal operating modes, i.e., phase *a* voltage v_{a}, phase *a* current i_{a}, DC-link voltage V_{DC}, and output voltage V_{out}, and proves basic converter functionalities. Furthermore, the switched voltage of phase *a*, $v_{\mathrm{a'y}}$, clearly differentiates the switching or clamping states of the corresponding VSR-stage bridge-leg. Similarly, the switched voltage of the DC/DC-stage's upper HB, v_{qy}, indicates the clamping intervals of the DC/DC-stage. Two integrated CM filters of the VSR-stage and the DC/DC-stage (i.e., capacitive connections between the artificial mains star point k and the DC-link midpoint y; and between the output midpoint m and y, respectively) are used to suppress HF CM noise at the DC-link and DC output midpoints and the measured CM capacitor voltages v_{ym} and v_{ky} thus mainly consist of LF components.

Fig. 7a presents the buck-mode operation with $V_{\mathrm{out}} = 400\,\mathrm{V}$, $P_{\mathrm{out}} = 10\,\mathrm{kW}$. The DC/DC-stage regulates V_{DC} into the six-pulse shape, i.e., the envelope of the line-to-line voltage absolute values to achieve 1/3-PWM operation (see $v_{\mathrm{a'y}}$) of the VSR-stage, i.e., each phase switches only during one-third of a mains period. **Fig. 7b** presents the transition-mode operation with $V_{\mathrm{out}} = 540\,\mathrm{V}$, $P_{\mathrm{out}} = 10\,\mathrm{kW}$. Note that V_{DC} is in excellent agreement with the analytical reference shown in **Fig. 4c**, and the extended clamping interval of the DC/DC-stage can be seen in v_{qy}. **Fig. 7c** shows boost-mode operation with $V_{\mathrm{out}} = 800\,\mathrm{V}$, $P_{\mathrm{out}} = 10\,\mathrm{kW}$ where all three phases of the VSR-stage switch all the time and the DC/DC-stage clamps, i.e., $\mathrm{T_{DC,hp}}$ and $\mathrm{T_{DC,hn}}$ are permanently on.

The proposed control strategy is verified in **Fig. 8**, where automatic and smooth transitions between different operating modes are achieved when the output voltage reference values increase from 460 V to 600 V. Both modulation schemes

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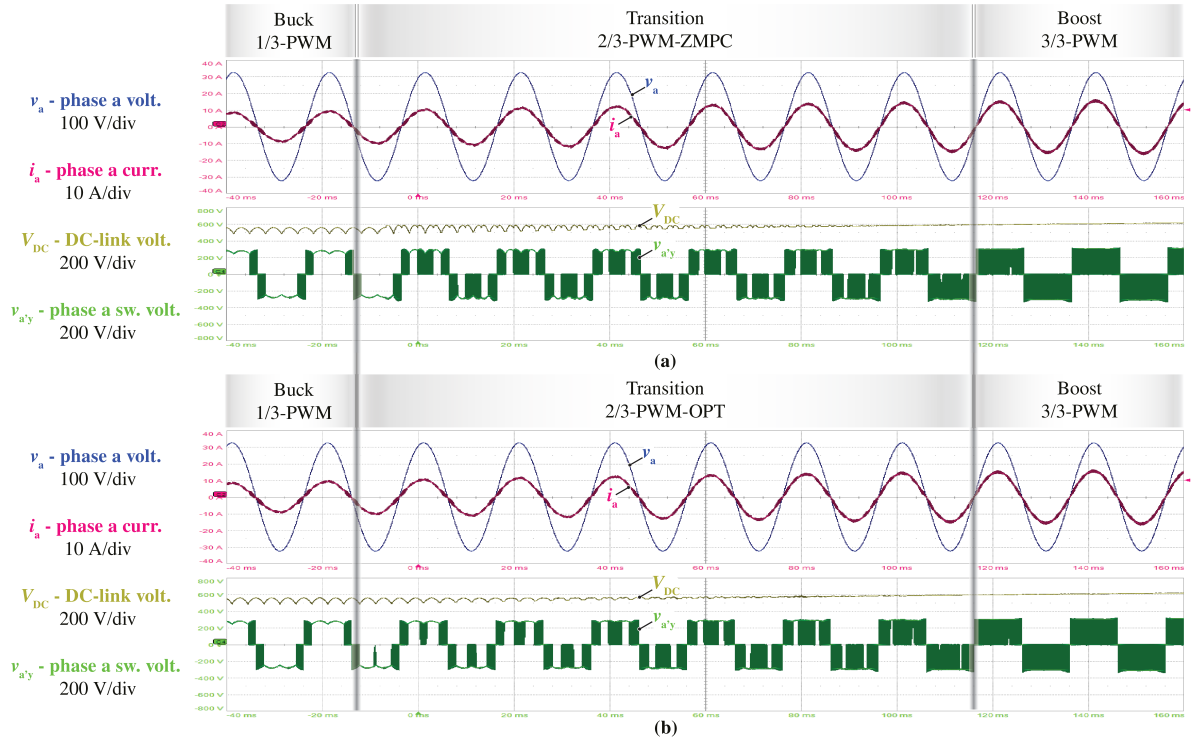

Fig. 8: Experimental waveforms of the converter shown in **Fig. 2** with the proposed synergetic control strategy operating with a constant resistive load of $50\,\Omega$ and a linearly increasing output voltage $V_{\text{out}} = 460\,\text{V} \sim 600\,\text{V}$, where different modulation schemes, i.e., **(a)** 2/3-PWM-ZMPC, and **(b)** 2/3-PWM-OPT, are applied in the transition-mode. 2/3-PWM-OPT achieves an automatic and seamless transition from the buck-mode to the boost-mode with the proposed control structure (see **Fig. 5**) with an extended clamping time of the VSR-stage bridge-legs (see $v_{a'y}$) and also of the DC/DC-stage bridge-legs (not shown), compared to 2/3-PWM-ZMPC. Note further the different shapes of the DC-link voltage V_{DC} between the modes (see also **Fig. 4**).

proposed for the transition-mode are compared, i.e., **(a)** 2/3-PWM-ZMPC and **(b)** the proposed loss-optimal 2/3-PWM. Note that to implement the transition mode with the (sub-optimal) 2/3-PWM-ZMPC, a slight modification of the control structure from **Fig. 5** is needed; specifically, $V^*_{2/3}$ has to be changed to the DC-link voltage reference $V^*_{\text{DC, ZMPC}}$ from (8).

C. Efficiency Measurement

The achievable efficiency improvement is quantified on the realized $10\,\text{kW}$ hardware demonstrator shown in **Fig. 6** considering operation over a wide output voltage range (from $200\,\text{V}$ to $800\,\text{V}$) and a wide output power range (from $25\,\%$ to $100\,\%$ of the rated load). The (measured) 3D efficiency surface (see **Fig. 9a**), featuring a fairly flat characteristic over the full operating area, is first shown for the proposed loss-optimal modulation scheme, i.e., 1/3-PWM in the buck-mode, 2/3-PWM-OPT in the transition-mode, and 3/3-PWM in the boost-mode. This surface is further visualized as a 2D contour plot in **Fig. 9c**, where the measured operating points are indicated. It is clear that high-efficiency operation, e.g., efficiencies above 98%, are achieved over a large part of the wide output voltage and power range. **Fig. 10a** shows efficiency versus output power for different output voltages and **Fig. 10a** shows efficiency versus output voltage at rated power, where the peak efficiency of 98.8% at $10\,\text{kW}$ can be noticed.

To highlight the efficiency advantages of using 1/3-PWM over 3/3-PWM in the buck-mode, efficiencies when operating with 3/3-PWM[8] in the buck-mode and the (sub-optimal) 2/3-PWM-ZMPC in the transition-mode are also measured (see **Fig. 9b**). The efficiency improvements are quantified in the contour plot shown in **Fig. 9d**. Clearly, using 1/3-PWM in the buck-mode realizes a significant improvement of up to 3.2%, and the proposed 2/3-PWM-OPT gives still a notable improvement of 0.8% over 2/3-PWM-ZMPC. **Fig. 10b** visualizes the efficiency gains at rated power for the different output voltages. Note that no efficiency difference is expected in the boost-mode, where 3/3-PWM (with ZMPC) is used in all cases.

D. EMI Measurement

Finally, conducted EMI tests have been carried out to assess the compliance of the realized $10\,\text{kW}$ hardware demonstrator (see **Fig. 6**) with the limits according to CISPR 11 Class A for the frequency range of $150\,\text{kHz}$ to $30\,\text{MHz}$. The designed EMI filter parameters are listed in **TABLE II**. The test setup consists of a Rhode & Schwarz ESPI3 EMI test receiver and a Rhode & Schwarz ESH2-Z5 three-phase LISN.

First, **Fig. 11** presents EMI measurement results when operating in the buck-mode ($V_{\text{out}} = 400\,\text{V}$, $P_{\text{out}} = 5\,\text{kW}$) with different modulation schemes, i.e., 3/3-PWM and 1/3-PWM. $8.5\,\text{dB}\mu\text{V}$ more noise emission is measured if 3/3-PWM is

[8]Using $V_{\text{DC}} = \sqrt{3}\hat{V}_{\text{in}}$, i.e., the minimum possible value for 3/3-PWM, and triangular third harmonic injection, i.e., $v_{\text{CM}} = -1/2(v_{\text{max}} + v_{\text{min}})$ (i.e., the same LF CM injection as results for 1/3-PWM), are applied for a fair comparison in the buck-mode. In the boost-mode, however,3/3-PWM-ZMPC is used as before. The same approach is also used in the later EMI comparison of 1/3-PWM and 3/3-PWM in the buck-mode.

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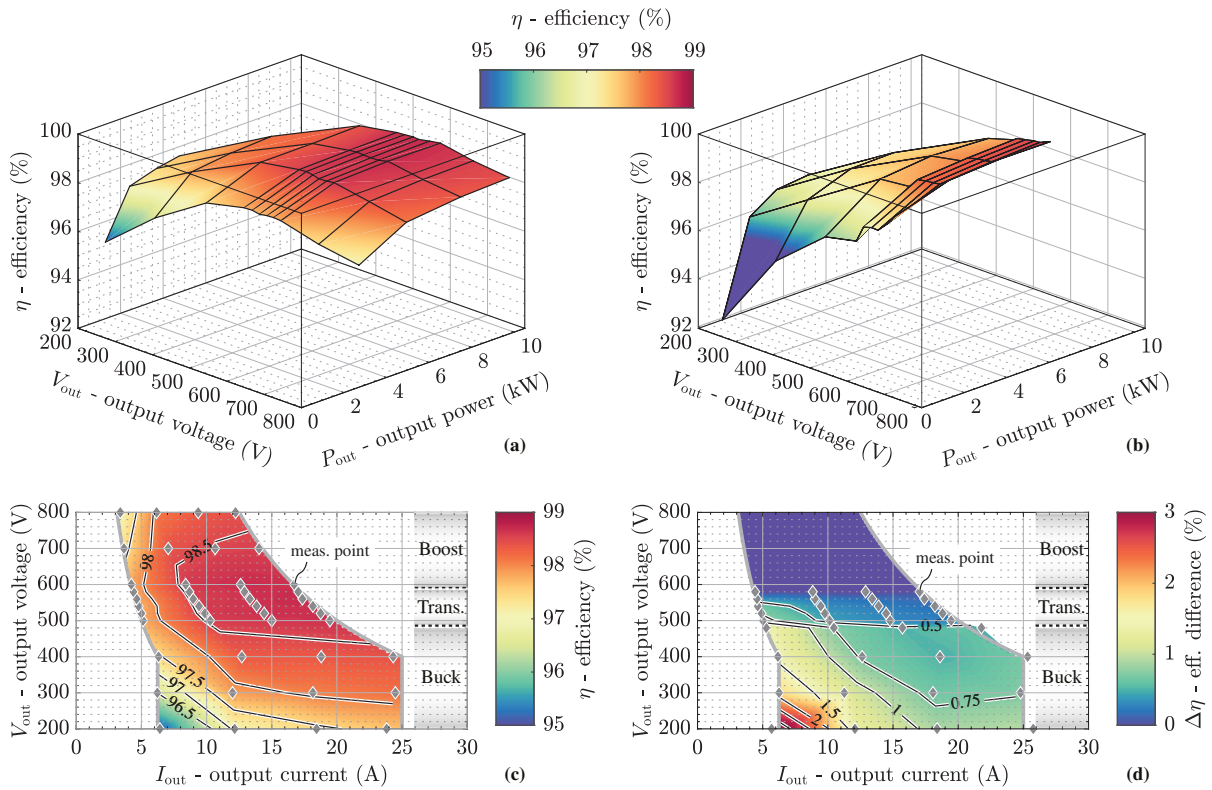

Fig. 9: Measured (Yokogawa WT3000) efficiencies of the realized 10 kW hardware demonstrator shown in **Fig. 6**, using **(a)** the proposed loss-optimal modulation scheme (1/3-PWM in the buck-mode, 2/3-PWM-OPT in the transition mode, and 3/3-PWM (with ZMPC) in the boost-mode) and **(b)** the conventional operating scheme, i.e., 3/3-PWM (without ZMPC) in the buck-mode and 2/3-PWM-ZMPC in the transition-mode. **(c)** shows the efficiency contours corresponding to **(a)** and indicates the measured points. **(d)** quantifies the efficiency difference between the proposed **(a)** and state-of-the-art **(b)** methods, highlighting efficiency improvements of up to 3.2% and 0.8% in the buck-mode and the transition-mode, respectively. Note that efficiency surfaces and curves are linearly interpolated from measured points.

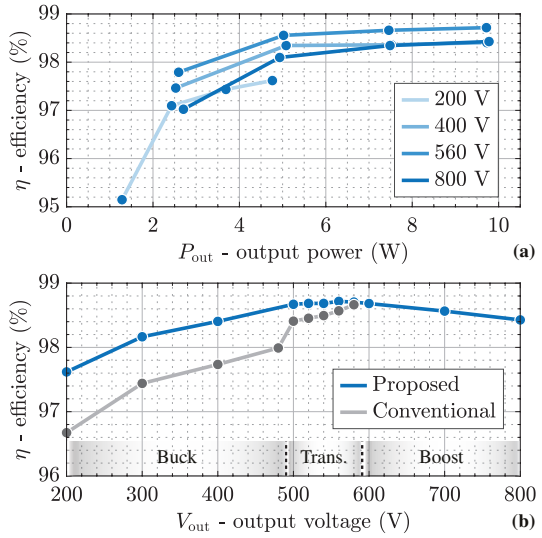

Fig. 10: Measured (Yokogawa WT3000) efficiency curves, i.e., **(a)** efficiency versus output power P_{out} (using the proposed loss-optimal modulation scheme) and **(b)** efficiency versus output voltage V_{out} at rated power (or rated output current below 400 V), where also the curve for conventional operation is shown as a reference. A peak efficiency of 98.8 % when $V_{\text{out}} = 560\,\text{V}$ and $P_{\text{out}} = 10\,\text{kW}$ can be achieved.

TABLE II: EMI Filter Specifications.

	Description	Value
$C_{\text{DM,1}}$	1st EMI DM film capacitor	3×3 µF
$C_{\text{CM,1}}$	1st EMI CM ceramic capacitor	18 nF
$L_{\text{DM,2}}$	2nd EMI DM inductor	3×15 µH, *WE 7443641500*
$C_{\text{DM,2}}$	2nd EMI DM film capacitor	3×6 µF
$L_{\text{CM,2}}$	2nd EMI CM inductor	870 µH, VAC 25/16/10, 8 turns
$C_{\text{CM,2}}$	2nd EMI CM ceramic capacitor	18 nF
$L_{\text{DM,3}}$	3rd EMI DM inductor	3×4.7 µH, *WE 7443640470*
$L_{\text{CM,3}}$	3rd EMI DM inductor	870 µH, VAC 25/16/10, 8 turns

applied instead of 1/3-PWM, which can be explained by the following two reasons:

- The EMI noise sources of the VSR-stage, in a first step, can be simply represented by the rms value of all HF components [49], i.e., the HF components of $v_{\text{CM}} = 1/3 \cdot (v_{\text{a'y}} + v_{\text{b'y}} + v_{\text{c'y}})$ and of $v_{\text{DM}} = v_{\text{a'y}} - v_{\text{CM}}$ (phase a as an example). Thus, 1/3-PWM achieves 2 dBµV less DM noise emission and 4 dBµV less CM noise emission compared with the conventional 3/3-PWM as shown in **Fig. 12**.
- The voltage-time area (peak value) stresses applied to the EMI DM/CM inductors are also compared between 1/3-PWM and conventional 3/3-PWM in **Fig. 12**. Similar DM stresses but significantly increased CM stress, i.e., 33% larger applied voltage-time area compared to 1/3-PWM, are observed when using 3/3-PWM.

Note that the DC/DC-stage operates similarly for both 1/3-

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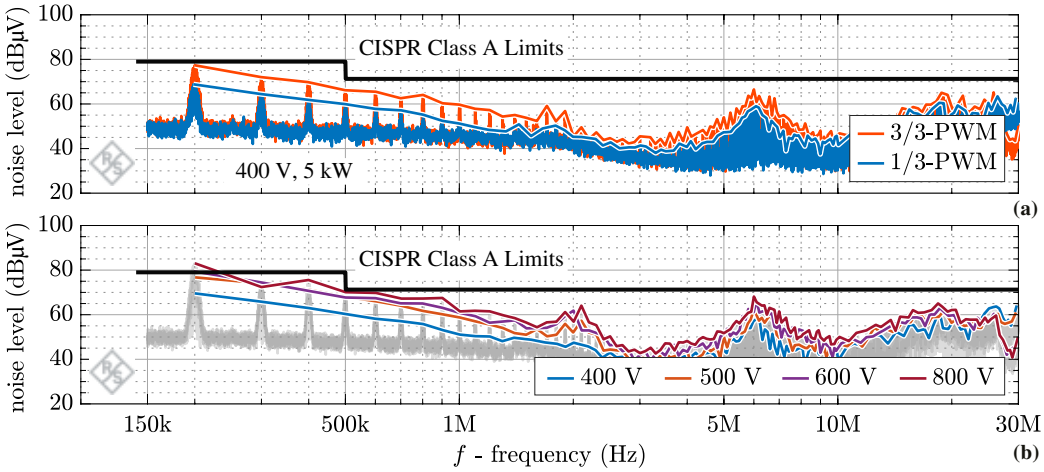

Fig. 11: Conducted EMI noise emission measurements. **(a)** Comparison between 1/3-PWM and 3/3-PWM operating at $V_{\text{out}} = 400\,\text{V}$ and $P_{\text{out}} = 5\,\text{kW}$, i.e., in the buck-mode. **(b)** Pre-qualification measurements at rated power and four typical output voltages which are measured on the realized 10 kW hardware demonstrator shown in **Fig. 6**. The CISPR 11 peak (PK) detector has been used with a 4 kHz step size, 9 kHz resolution bandwidth (RBW), and 1 ms measurement time. The local peak values are connected as an envelope for easier comparisons between different operating points.

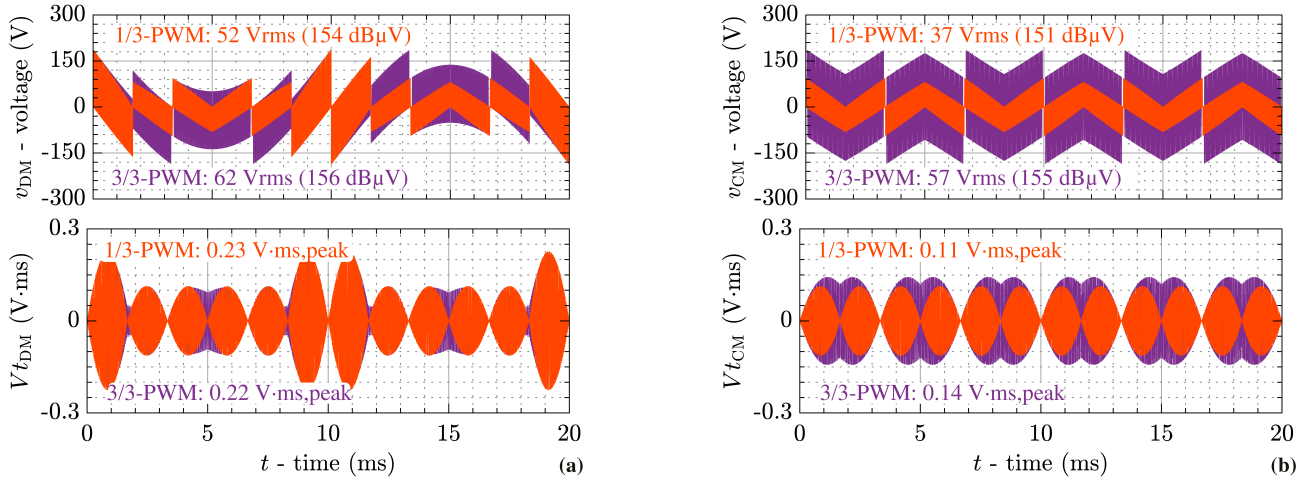

Fig. 12: Comparison of analytically calculated HF **(a)** DM and **(b)** CM noise source characteristics of the VSR-stage using 1/3-PWM (red) and 3/3-PWM (purple) for operation in the buck-mode at $V_{\text{out}} = 400\,\text{V}$. Note that the operating conditions for the DC/DC-stage are similar in both cases and hence neglected.

PWM and 3/3-PWM employed in the buck-mode, i.e., both HBs are always switching but only at slightly different DC-link voltages, so the impact from the DC/DC-stage can be neglected. Furthermore, this analysis also validates that the EMI filter designed for 3/3-PWM can be directly used in 1/3-PWM operation without any additional EMI redesign or filter modifications.

Finally, **Fig. 11b** summarized conducted EMI pre-compliance measurements of the hardware demonstrator for four typical output voltage operating points and rated output power, where always the loss-optimal modulation method is used (i.e., 1/3-PWM in the buck-mode for $V_{\text{out}} = 400\,\text{V}$, 2/3-PWM-OPT in the transition mode for $V_{\text{out}} = 500\,\text{V}$, and 3/3-PWM (with ZMPC) in the boost-mode for $V_{\text{out}} = 600\,\text{V}$ and $V_{\text{out}} = 800\,\text{V}$). Except for some minor violations at the maximum output voltage, which is likely due to partial saturation of CM chokes and could be addressed by minor redesigns, the demonstrator meets the CISPR 11 Class A limits.

V. Conclusion

Aiming for a standard building block for isolated and non-isolated EV chargers, this paper comprehensively studies and analyzes a three-phase (3-Φ) boost-buck (Bb) voltage DC-link AC/DC converter that consists of a 3-Φ three-level (3-L) T-type (Vienna) voltage source rectifier (VSR)-stage and a 3-L buck-type DC/DC-stage. Whereas loss-optimum modulation schemes for the buck-mode (1/3-PWM) and for the boost-mode (3/3-PWM) are known, this paper proposes a new modulation scheme for the transition-mode (i.e., for output voltages between buck-mode and boost-mode): the new 2/3-PWM-OPT enables loss-optimal operation for the full wide output voltage range of 200 V to 800 V. This loss-optimal operation mode ensures that only three (of the converter's five) half-bridges (HBs) are actively switching (i.e., operate with PWM) at any given point in time and do so with the minimum possible DC-link voltage, which results in the minimum possible switching losses. Furthermore, a synergetic control strategy is proposed to operate the VSR-stage and the DC/DC-stage collaboratively

to achieve automatic and seamless transitions between the different loss-optimum operating modes and modulation schemes when the output voltage changes.

The operating modes and the control strategy are implemented and verified with a compact $10\,\mathrm{kW}$ hardware demonstrator ($5.4\,\mathrm{kW/L}$ or $91\,\mathrm{W/in^3}$) with a peak efficiency of 98.8% at rated load and $560\,\mathrm{V}$ output voltage. Comprehensive efficiency measurements confirm the expected improvement achieved by the loss-optimal operation over the basic decoupled operation of the two converter stages, i.e., up to 3.2% in the buck-mode with 1/3-PWM and up to 0.8% in the boost-mode with 2/3-PWM-OPT. Finally, the conducted EMI compliance of CISPR 11 Class A is tested and the regulations are largely met. Importantly, an EMI filter designed for 3/3-PWM can be directly used for 1/3-PWM operation.

All in all, the modulation and control concept presented in this paper can be considered the optimum way of operating a three-level boost-buck voltage DC-link AC/DC grid interface with a wide output voltage range.

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