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A Three-Phase Synergetically Controlled Buck-Boost Current DC-Link EV Charger

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Abstract—With the ever-increasing share of electric vehicles (EVs) comes a need for highly efficient and compact EV chargers. EV charger modules should provide a wide output voltage range (200 V to 1000 V) to ensure compatibility with various EV battery voltages. Thus, buck-boost functionality is needed, which can advantageously be realized by a current DC-link topology: a buck-type current-source rectifier (CSR) stage and a downstream three-level (3-L) boost-type DC/DC-stage share the main magnetic component (the DC-link inductor). Furthermore, the two stages can operate collaboratively: for low output voltages, the CSR-stage controls the output voltage and the DC/DC-stage is clamped to avoid switching losses; for high output voltages, the DC/DC-stage shapes the DC-link current such that the CSR-stage operates with 2/3-PWM (switching limited to two out of the three phases) and hence with reduced switching losses. This paper thus introduces a simplified synergetic control concept that ensures this loss-optimum operation of the two-stage system for any output voltage. A compact 10-kW hardware demonstrator with a power density of 6.4 kW/dm^3 (107.5 W/in^3) is then used to verify the control concept and the seamless transitions between operating modes. For the first time, a system-level experimental demonstration of the loss savings achieved by 2/3-PWM is provided, and pre-compliance conducted EMI test results meet CISPR 11 Class A. Moreover, a detailed experimental characterization of losses/efficiency over the full range of output voltage and power confirms the loss models and the design procedure presented earlier. Finally, the demonstrator shows quite a flat efficiency characteristic (higher than 98% for most operating points with output voltages above 400 V and more than 25% of rated load) with a peak efficiency of 98.8% at 520 V output voltage and 5 kW. All in all, the presented current DC-link buck-boost PFC rectifier system features a promising solution for future isolated or non-isolated EV charger modules.

Index Terms—Electric Vehicle Chargers, Three-Phase Buck-Boost Current DC-Link PFC Rectifier, Two-Third Pulse-Width Modulation, Synergetic Control.

I. INTRODUCTION

The International Energy Agency (IEA) estimates that there will be 220 million electric vehicles (EVs) on the road by 2030, with China, Europe, and North America accounting for the majority of this growth according to the "Global EV Outlook 2021" report [1]. Obviously, EV batteries must be recharged or might even serve as energy storage complementing fluctuating renewable generation in future energy systems [2]. Hence, EV charging technology is vital to the widespread adoption of EVs and to shaping the future of low-carbon-emission road transport.

A typical battery charging profile comprises two charging modes, i.e., constant current (CC) mode and constant voltage (CV) mode [3], [4]. Starting with a discharged battery, first, a high charging current is applied in the CC charging mode
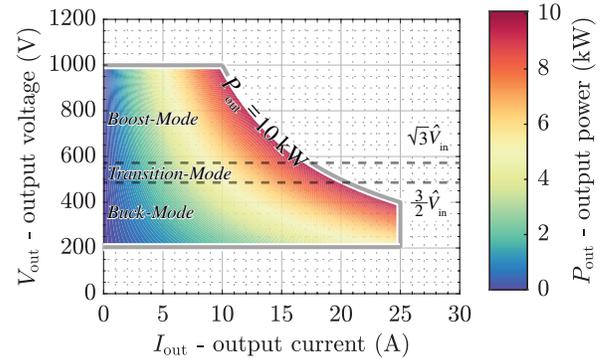

Fig. 1: Typical operating range of a 10 kW EV charger module covering a output voltage from 200 V to 1000 V with an output current limit of $I_{\text{out}} = 25$ A. Such a wide output voltage range is covered by three main operating modes, i.e., buck-mode, transition-mode, and boost-mode.

until the battery voltage reaches a certain threshold voltage, and then above this threshold voltage, the charger is switched to CV charging mode, completing the charging process with a decreasing current at an almost constant battery voltage to avoid thermal run-away of the battery [5]. Hence, EV chargers do not operate at full load most of the time: in the CC mode, although the charger provides rated current, the battery voltage only gradually increases starting typically from about 80% of the rated voltage for a lithium-ion battery [3]; in the CV mode, only a small charging current is allowed if the battery voltage is close to the rated value. Various nominal battery voltages such as 400 V or 800 V are in use, and hence standards such as CHAdeMO [6] define wide output voltage ranges of 150 V to 1000 V for universal EV chargers. Thus, high-efficiency operation over wide output-power and output-voltage ranges, i.e., a flat high-efficiency characteristic, is a desirable feature of power converters used for EV charging.

EV chargers interface the AC mains to the DC terminals of EV batteries and are typically realized with two converter stages [7]: a grid-side AC/DC PFC rectifier and a subsequent, typically isolated, DC/DC-stage. Such isolated converter stages can be implemented, for example, as a dual active bridge (DAB) converter [8]–[11] or as an LLC resonant converter [12], which both provide an adjustable voltage gain. Even though, in this case, the required ultra-wide output voltage regulation capability can be collaboratively provided by both the DC/DC converter and the 3-Φ PFC rectifier front-end, loss-optimal operating modes of the whole system depend on the specific loss characteristics of the PFC rectifier and the DC/DC-stage. In other words, these loss-optimal operating modes are different for each specific realization of these
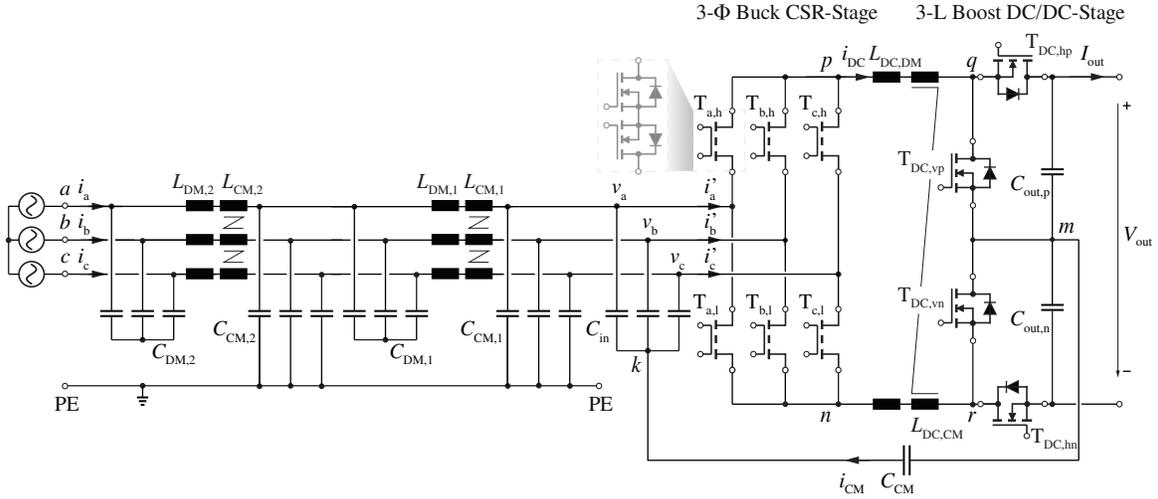
Fig. 2: Power circuit of the considered $10\,\text{kW}$ three-phase (3-Φ) buck-boost (bB) current DC-link PFC rectifier system including CM/DM EMI filters, which employs a 3-Φ buck-type current-source rectifier (CSR)-stage cascaded by a 3-L boost-type DC/DC-stage via a shared DC-link inductor. To filter the high-frequency common-mode (CM) noise at the DC output port, an integrated CM filter consisting of a shared CM inductor $L_{\text{DC,CM}}$ in the DC-link and a capacitor C_{CM} that ties the DC output midpoint to the artificial mains neutral point k, formed by input capacitors, is applied. **Tab. I** lists the key specifications and components.

converter stages. Thus, optimal designs of such a cascaded system have to take the front-end and the isolation-stage into account at the same time instead of optimizing them separately. To avoid such design and control issues, and to achieve high efficiency, often series-resonant DC/DC-stages with limited voltage control range, i.e., DC transformers (DCXs) [13]–[15], are used [16]. Then, the AC/DC PFC rectifier stage must provide buck-boost functionality to cover the wide output voltage range (typ. $200\,\text{V}$ to $1000\,\text{V}$, see **Fig. 1**). This is especially also the case in future non-isolated EV chargers [17], [18].

Today, most EV chargers employ topologies with a voltage DC-link [19] (i.e., a DC-link capacitor is placed between a boost-type PFC rectifier and a buck-type DC/DC converter, realizing boost-buck functionality). Alternatively, however, topologies with a current DC-link (i.e., a DC-link inductor connects a buck-type PFC rectifier and a boost-type DC/DC converter) can also be applied.

Current DC-link topologies have first been employed in thyristor-based line-commutated medium-voltage drives in the 1970s [20]. Later, with the availability of gate-turn-off thyristors (GTOs) or gate-commutated thyristors (GCTs), PWM operation and thus motor-friendly waveforms and reliable short-circuit protection could be realized [21]–[25]. Applications with lower voltages and power levels have also been considered due to the advent of wide-bandgap (WBG) power semiconductors, which facilitate higher switching frequencies and thus a reduction of the otherwise potentially large DC-link inductor volume [26], such as variable speed drives [27]–[30], data center power supplies [31]–[33], solid-state transformers [34], electric springs [35], grid interfaces for renewable energy sources [36], and recently also EV chargers [37]–[40]. Furthermore, extensive research has been conducted on the duality between and the comparative analyses of voltage DC-link and current DC-link converters [41]–[46].

However, current DC-link systems require switching devices

with the capability to block both voltage polarities and to conduct at least one or possibly (for bidirectional AC/DC conversion) both current directions. These switching devices were commonly realized by series connection of diodes with uni-polar devices, e.g., normally-on SiC JFETs [27], [47], for uni-directional operations. However, recently, the development of monolithic bidirectional power transistors has gained traction [48]–[50]; these devices provide the required functionality with only about one fourth of the chip area required for today's realizations based on anti-series connections of uni-polar devices [51]; hence, in contrast to voltage DC-link topologies, current DC-link topologies feature a significant potential for future performance improvements and/or cost reductions.

Therefore, targeting a universal[1] EV charger AC/DC module covering the wide operating range shown in **Fig. 1**, the 3-Φ bidirectional buck-boost (bB) current DC-link PFC rectifier system shown in **Fig. 2** is considered in this paper. So far, a similar topology has commonly been realized by a 3-Φ buck-type current-source rectifier (CSR)-stage and a subsequent two-level (2-L) boost-type DC/DC-stage [52]–[54]. However, in this paper, a 3-L boost-type DC/DC-stage is preferably employed to avoid considerable hard-switching losses occurring at high output voltages for EV battery charger applications. Compared to a conventional realization with a 3-Φ boost-buck (Bb) voltage DC-link PFC rectifier [55], advantageously only one shared main magnetic component, i.e., the DC-link inductor connecting the CSR-stage and the DC/DC-stage, is needed instead of three AC-side boost inductors plus at least one DC-side inductor of the then needed buck-type DC/DC-stage, which facilitates a compact converter realization.

The conventional loss-optimal operation and the corre-

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[1]Note that [18] discusses a control method for the proposed topology, which regulates the low-frequency ground leakage current to zero and allows a direct connection of the DC output midpoint to protective earth, hence facilitating non-isolated charger applications.

TABLE I: System specifications and key components of the demonstrator introduced in **Section V**.

	Description	Value
V_{in}	RMS phase volt.	230 V
V_{out}	DC output volt. range	200 V∼1000 V
P_{out}	Rated output power	10 kW
$I_{out,max}$	Output curr. limit	25 A ($V_{out} < 400$ V)
T_{CSR}	CSR-stage semi.	C3M0021120K, 1200 V, 21 mΩ
f_{CSR}	CSR-stage sw. freq.	100 kHz
$T_{DC/DC}$	DC/DC-stage semi.	C3M0010090K, 900 V, 10 mΩ
$f_{DC/DC}$	DC/DC-stage sw. freq.	100 kHz
$2 \times L_{DC,DM}$	DC-link DM ind.	2×125 µH (3×N87 ELP 43/10/28, 14 turns)
$2 \times L_{DC,CM}$	DC-link CM ind.	2×5.5 mH (VAC 500F 40/25/15, 10 turns)
C_{in}	Input filter cap.	3×6 µF
$C_{out,p} = C_{out,n}$	Output filter cap.	2×11.2 µF
C_{CM}	Integrated filter cap.	88 nF
$L_{DM,1} = L_{DM,2}$	EMI DM ind.	15 µH
$C_{DM,1} = C_{DM,2}$	EMI DM cap.	3 µF
$L_{CM,1} = L_{CM,2}$	EMI CM ind.	1.2 mH (VAC 20/12.5/8, 11 turns)
$C_{CM,1} = C_{CM,2}$	EMI CM cap.	18.8 nF

sponding control of such two-stage 3-Φ buck-boost current DC-link PFC rectifiers, considering 2-L DC/DC-stages, have been analyzed, e.g., in [53], [54], where a robust controller enabling operation with heavily unbalanced mains is presented in [53], and [54] derives a detailed control-oriented small-signal model. In both cases, the implemented control methods can achieve a state-of-the-art loss-optimal operation: if the output voltage is relatively low (buck-mode, see **Fig. 1**), the DC/DC-stage is clamped without generating switching losses but the CSR-stage solely regulates the output voltage; advantageously the DC/DC boost-stage is only activated if the output voltage is high[2] (boost-mode, see **Fig. 1**).

However, if the DC/DC-stage has to operate, it can advantageously be used to shape the DC-link current to follow the maximum of the absolute values of the three mains currents, which allows advanced 2/3-PWM operation of the CSR-stage, i.e., only active switching states are needed but not the zero (freewheeling) switching states [49], [53], [56], [57]. Thus, the advanced 2/3-PWM only needs to switch two instead of three phases of the CSR-stage within one switching period, resulting in a significant reduction in switching losses because there are fewer switching instants and these happen at lower voltages (see **Section II.B** for further details). Taking advantage of this, a synergetic control concept that operates the converter shown in **Fig. 2** in the loss-optimal mode for any output voltage (i.e., employs 2/3-PWM whenever possible, and clamps the DC/DC-stage if the output voltage is sufficiently low) has been introduced in [40]. However, the controller structure presented in [40] is quite complex regarding its implementation, and

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[2]The output voltage is higher than $3/2 \cdot \hat{V}_{in}$ with $\hat{V}_{in}$ denoting the phase voltage amplitude, i.e., the maximum output voltage that a buck-type CSR-stage can generate.

the concept has further never been experimentally verified, especially over a wide output voltage range where different modulation schemes and operating modes have to be covered.

Furthermore, [49] reports significant calculated performance improvements achieved by using advanced 2/3-PWM instead of conventional 3/3-PWM (with a constant DC-link current that is at least as high as the peak value of the phase currents), but considers only the CSR-stage. Thus, [38], [39] have addressed the system-level losses (i.e., the CSR-stage and the DC/DC-stage) and provide a detailed loss modeling analysis and EMI filter design procedure for the analyzed topology shown in **Fig. 2**, and use Pareto optimization to select a final converter design. However, there is again a lack of a comprehensive experimental evaluation of the system-level loss reduction as well as a possible impact on the EMI emission signature of using 2/3-PWM.

Therefore, this paper addresses the research gaps mentioned earlier by introducing a simplified and intuitive implementation of the synergetic control concept retaining all the advantageous features, e.g., achieving loss-optimal operation with advanced 2/3-PWM and ensuring seamless transitions between different operating modes democratically. The proposed control strategy is then verified on a realized 10 kW hardware demonstrator to, importantly, provide extensive experimental verification of the proposed design and the synergetic control method, e.g., efficiency characteristics over a wide operating range, efficiency improvement achievable with 2/3-PWM, and conducted EMI noise emissions.

First, **Section II** derives and explains the advanced 2/3-PWM concept for current DC-link systems with the comparison of conventional 3/3-PWM, before **Section III** discusses the loss-optimal operating modes for the three regions of the wide output voltage range (200 V to 1000 V) indicated in **Fig. 1**. **Section IV** then presents the new simplified synergetic control structure that ensures operation in the respective loss-optimal mode and seamless transitions between these modes. **Section V** introduces a 10 kW hardware demonstrator and provides extensive experimental results. Detailed efficiency measurements in the full operating range demonstrate a flat efficiency characteristic and a peak efficiency of 98.8%. EMI pre-compliance test results meeting CISPR 11 Class A limits are also provided. Finally, **Section VI** concludes this paper.

II. CURRENT DC-LINK PULSE-WIDTH MODULATION

The CSR-stage (see **Fig. 2**) consists of two commutation cells, each comprising three bidirectional switches (e.g., the high-side commutation cell consists of $T_{a,h}$, $T_{b,h}$, and $T_{c,h}$). At any given time, one and only one (otherwise, the line-to-line voltage would be short-circuited) switch per commutation cell is turned on and connects the DC-link current to one of the three-phase terminals. Therefore, the switching state of the CSR-stage can be described in the form [ab] (see **Fig. 3**), where this specific example indicates that the high-side commutation cell connects phase a to the DC-link and the low-side commutation cell connects phase b to the DC-link. Freewheeling states are possible, too, e.g., [bb] indicates that the DC-link current freewheels through the two commutation
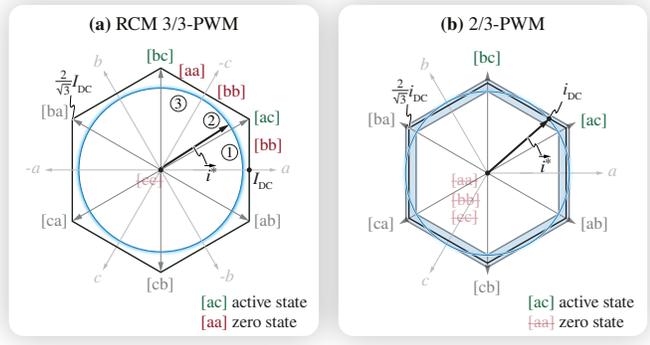
Fig. 3: Space vector diagrams of **(a)** Reduced CM (RCM) 3/3-PWM where the hexagon size is fixed by a constant I_{DC}, i.e., the active space vectors' magnitude is $2/\sqrt{3}\,I_{DC}$ and **(b)** 2/3-PWM where the hexagon size is pulsating (over the shaded area) according to a time-varying i_{DC}, i.e., the active space vectors' magnitude is $2/\sqrt{3}\,i_{DC}$. The switching state of the CSR-stage is expressed by the turned-on switches of the high-side and low-side commutation cells as, for example, [ac], which indicates that the DC-link current flows through $T_{a,h}$ and $T_{c,l}$.

TABLE II: Modulation sequences, i.e., switching state sequences, within one switching period considering three exemplary sectors (see **Fig. 3**). The hard turn-on switching transitions of the two switches connected to phase a are indicated by the $\Rightarrow$ symbol, whereas the soft turn-on and all turn-off switching transitions are indicated by the $\rightarrow$ symbol.

Sector	RCM 3/3-PWM	2/3-PWM
①	[bb]$\Rightarrow$[ab]$\rightarrow$[ac]$\rightarrow$[ab]$\rightarrow$[bb]	[ab]$\rightarrow$[ac]$\rightarrow$[ab]
②	[bb]$\rightarrow$[bc]$\Rightarrow$[ac]$\rightarrow$[bc]$\rightarrow$[bb]	[bc]$\Rightarrow$[ac]$\rightarrow$[bc]
③	[aa]$\rightarrow$[ac]$\rightarrow$[bc]$\rightarrow$[ac]$\rightarrow$[aa]	[ac]$\rightarrow$[bc]$\rightarrow$[ac]

cells' switches connected to phase b. In each switching period, a sequence of switching states must be applied to realize sinusoidal local average values of the phase currents, i'_a, i'_b, and i'_c. Two conceptually different PWM schemes, i.e., conventional 3/3-PWM and advanced 2/3-PWM [53], [56], can be applied and are discussed in the following.

A. Conventional 3/3-PWM

Conventionally, current DC-link rectifiers operate with a constant DC-link current I_{DC} that must be at least as high as the peak value of the phase currents. A constant DC-link current and the available switching states define six active space vectors with a magnitude of $2/\sqrt{3}\,I_{DC}$ and three zero vectors (freewheeling states) as indicated in **Fig. 3a**. To realize a desired input current space vector $\vec{i}^*$, each switching period is composed of the two closest active states and one zero state. Therefore, all three phases are switching with PWM ("3/3-PWM", see **Fig. 4a**) within one switching period.

In the example shown in **Fig. 3a**, which considers a vector $\vec{i}^*$ in sector ②, the active states [ac] and [bc] are needed, whereas the selection of the zero state ([aa] or [bb] or [cc]) is a degree of freedom to optimize, e.g., the overall switching losses [26] or the resulting low-frequency CM voltage [58]. If the zero state corresponding to the phase with the minimum phase voltage, i.e., phase b and hence state [bb] in sector ②, is selected, a Reduced Common-Mode (RCM) 3/3-PWM[3] results without sacrificing switching losses [58], which advantageously features a continuous low-frequency CM voltage without any voltage step at the sector boundaries [39]. This facilitates the integrated CM filter composed of $L_{DC,CM}$ and C_{CM} (see **Fig. 2**). **Tab. II** lists the resulting RCM 3/3-PWM switching sequences for $\vec{i}^*$ in three exemplary sectors. Note that the sequences are symmetric with respect to the center of a switching period, which facilitates synchronous sampling of the local average (over one switching period) DC-link current

[3]Unless otherwise noted, 3/3-PWM indicates RCM 3/3-PWM in the rest of paper.

and further ensures that only one commutation cell switches (instead of two commutation cells) during each transition [26], [27], [39], [44], [58].

Note that the modulation index of the CSR-stage is

$$M = \frac{\hat{I}_{in}}{i_{DC}} = \frac{\bar{v}_{pn}}{\frac{3}{2}\hat{V}_{in}} \leq 1, \tag{1}$$

and hence a maximum DC output voltage of voltage $\bar{v}_{pn} = V_{out} \leq 3/2\hat{V}_{in} = 488\,\text{V}$ (the numerical value refers to a $400\,\text{V}$ mains) can be realized without a downstream DC/DC-stage (or with that DC/DC-stage not operating as shown in **Fig. 2**).

B. Advanced 2/3-PWM

Differently, if such a DC/DC-stage is present (see **Fig. 2**), the DC/DC-stage can be utilized to realize 2/3-PWM of the CSR-stage [49], [53], [56], [57], which requires a time-varying DC-link current i_{DC}. This time-varying DC-link current i_{DC} follows the upper envelope of the 3-Φ current absolute values (see **Fig. 4b**), i.e., shows the typical six-pulse shape. In the space vector diagram (see **Fig. 3b**), such a six-pulse-shaped DC-link current is translated into a correspondingly pulsating size of the hexagon spanned by the six active vectors (whose length, after all, is given by the instantaneous value of the DC-link current) [49]. Zero states are not needed to modify the length of the synthesized vector; actually, any point on the hexagon can be reached by only applying active vectors. Because now the hexagon's size is pulsating, it becomes possible to synthesize the circular trajectory of $\vec{i}^*$ without any zero states, which is clearly visible from the exemplary switching sequences given in **Tab. II**. Consequently, each switching period is only composed of two active switching states but no zero state such that only two out of three phases are switching with PWM ("2/3-PWM") over one switching period. The switching sequence is implemented to minimize the voltage-time area of the DC-link inductor, i.e., the corresponding switching-frequency DC-link current ripple, by centering the switching state with a larger v_{pn} within one switching period, e.g., in sector ②, $v_{ac} > v_{bc}$ such that the switching state [ac] is centered, and vice versa in sector ③ [39], [49].[4]

Importantly, an additional converter stage, e.g., a boost DC/DC-stage as shown in **Fig. 2**, is always needed to im-

[4]Note that the switched voltage of the 3-L boost DC/DC-stage is also aligned at the center of one switching period such that the voltage-time area of the DC-link inductor, i.e., the time integral of the voltage difference $v_{pn} - v_{qr}$ (see **Fig. 2**), is minimized.
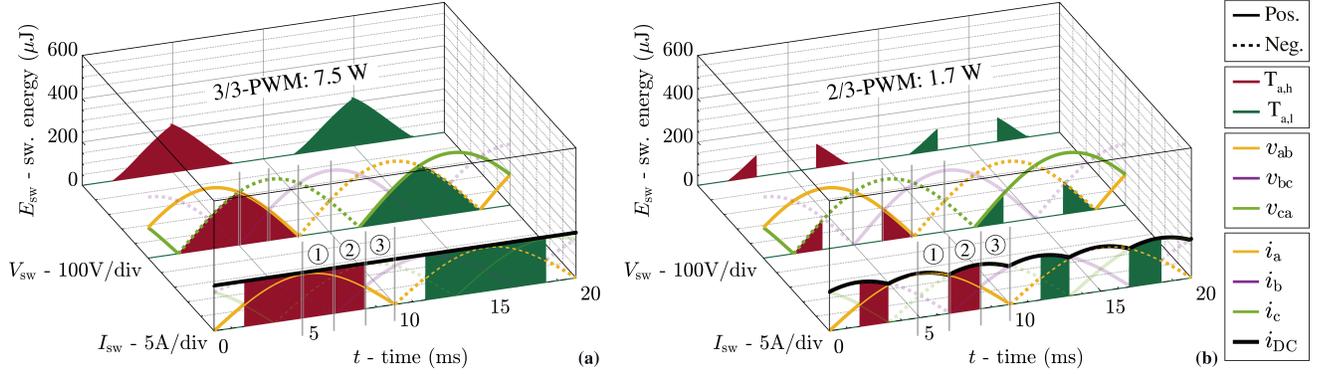
Fig. 4: Calculated hard-switching energy dissipated in the switches $T_{a,h}$ (red) and $T_{a,l}$ (green) connected to phase a over one mains period, and corresponding switched voltages and currents when **(a)** 3/3-PWM and **(b)** 2/3-PWM are applied. In both cases, $V_{out} = 800\,\text{V}$ and $P_{out} = 10\,\text{kW}$. In average, 1.7 W instead of 7.5 W, i.e., a 77% reduction of switching losses, results if 2/3-PWM instead of 3/3-PWM is employed, since the switches switch less frequently and with reduced voltages and currents (details in the text). Note that soft-switching transitions and their losses are neglected.
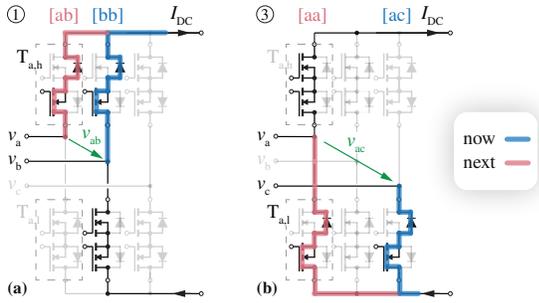

Fig. 5: Two exemplary switching states before and after actual commutations occurring in sectors **(a)** ① and **(b)** ③ (see **Fig. 3**), which directly involve $T_{a,h}$ or $T_{a,l}$, respectively. In sector ①, switching from [bb] to [ab] is a hard-switching transition since the switched voltage $v_{ab} > 0$ and the switched current flows out of the switching node (see **Fig. 2**). In sector ③, the switched voltage $v_{ac} > 0$ but the switched current flows into the switching node. Thus, switching from [ac] to [aa] is a soft transition. A more detailed explanation is given in the main text.

plement 2/3-PWM because **(i)** the six-pulse shape DC-link current has to be regulated by this additional converter stage; **(ii)** 2/3-PWM can only rectify 3-Φ mains voltages into six-pulse shape $\bar{v}_{pn}$ at the output of the CSR-stage, so that this converter stage is required to regulate $\bar{v}_{pn}$ into a constant DC output voltage.

C. Switching Loss Comparison

The potential switching loss savings of operating the CSR-stage with 2/3-PWM instead of with 3/3-PWM are analyzed in the following. Focusing on the CSR-stage, a high output voltage ($V_{out} = 800\,\text{V}$) that requires operating the boost-type DC/DC-stage in both cases is considered. **Fig. 4** compares the hard-switching losses E_{sw} generated in the two bidirectional switches connected to phase a (i.e., $T_{a,h}$ and $T_{a,l}$) considering the 3/3-PWM[5] and the 2/3-PWM for $V_{out} = 800\,\text{V}$ and $P_{out} = 10\,\text{kW}$.

Before further exploring these results, it is important to briefly discuss the physical realization of these switches, which

is indicated in **Fig. 2** and shown in detail in **Fig. 5**, and the nature of the commutations. In general, commutations occur between two switches of one commutation cell in a current DC-link rectifier, e.g., changing the state from [bb] to [ab] implies that the DC-link current commutates from $T_{b,h}$ to $T_{a,h}$ as indicated in **Fig. 5**; the involved commutation voltage is the line-to-line voltage v_{ab}. As the line-to-line voltage attains both polarities, each switch must be realized by an anti-series connection of two MOSFETs to block these bipolar voltages. Note that, different from the voltage DC-link PFC rectifier where the commutation loop closes over the DC-side commutation capacitors (in parallel with the DC-link capacitors), the commutation loop of the current DC-link rectifier includes AC-side commutation capacitors (in parallel with the AC-side filter capacitors C_{in} in **Fig. 2**).

For a given polarity of a line-to-line voltage, e.g., v_{ab}, two of the four involved MOSFETs can either be turned-on or turned-off without affecting the switching state because their anti-parallel diodes are forward-biased by the line-to-line voltage. Whereas it is generally advantageous to keep these MOSFETs on (to reduce conduction losses), the current-direction-dependent four-step commutation sequences [59] that are needed in practice to ensure that (i) there is always a path for the DC-link current and (ii) the AC-side capacitors are never short-circuited, result in the (intermediate) circuit configurations just prior and after the actual current commutation as shown in **Fig. 5**. It is clearly recognizable that the actual commutations are identical to those known from half-bridge arrangements with the voltage DC-link; however, the assignment of turn-on and turn-off losses to the individual MOSFETs changes with the polarity of the involved line-to-line voltage. As here the focus is on system-level loss behavior, losses are assigned to the bidirectional switches, e.g., $T_{a,h}$ or $T_{a,l}$, without considering the individual MOSFETs for simplicity. Thus, considering the example occurring in ① when implementing 3/3-PWM (see **Fig. 5a**), the transition from [bb] to [ab] results in a hard-switching with $T_{a,h}$ subject to a hard turn-on.[6] The other exemplary transition in the low-

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[5]3/3-PWM uses $i_{DC} = \hat{i}_{DC,2/3} = \hat{I}_{in}$, which is the minimum constant DC-link current required to generate 3-Φ sinusoidal mains currents without modulation saturation.

[6]All hard-switching losses are assigned to the turning-on switch for simplicity [38]

side commutation cell from [ac] to [aa] occurs in ③ when implementing 3/3-PWM (see **Fig. 5b**), which results in a soft-switched with $T_{a,l}$. Soft-switching transitions are assumed to be lossless.

The hard-switching losses E_{sw} of a given transition can be modeled as

$$E_{sw} = (k_1 I_{sw}^2 + k_2 I_{sw} + k_3)V_{sw} + (C_{oss,Q} + C_{par})V_{sw}^2, \quad (2)$$

where V_{sw} and I_{sw} indicate the switched voltage and current, respectively. The losses contain two main contributions, i.e., losses introduced by the overlap of the switched voltage and current waveforms, and capacitive losses resulting from the charging and discharging of the semiconductor (charge-equivalent) output capacitance $C_{oss,Q}$ and the parasitic (PCB, etc.) capacitance C_{par} [38].

The hard-switching losses dissipated in $T_{a,h}$ and $T_{a,l}$ are indicated **Fig. 4** assuming PFC operation with unity power factor over one mains period. Furthermore, the modulation sequences, i.e., the switching state sequences, of three exemplary sectors are listed in **TABLE II**. In sector ①, the switching transition from [bb] to [ab] contributes to significant switching losses because of a comparably large switched line-to-line voltage v_{ab}. However, such a hard-switching transition only exists for 3/3-PMW since the zero state [bb] is not needed for 2/3-PWM; note that thus significantly longer intervals without hard-switching losses are achieved when using 2/3-PWM. In sector ②, hard-switching losses are generated when switching from [bc] to [ac] for both 3/3-PWM and 2/3-PWM. However, importantly, in sector ②, the switched line-to-line voltage v_{ab} (see **Fig. 4**) is lower, leading to relatively small switching losses compared to the one generated in sector ① with 3/3-PWM. In sector ③, $T_{a,h}$ and $T_{a,l}$ are not subject to hard turn-on transitions and hence almost no switching losses are generated for both, 3/3-PWM and 2/3-PWM.

Thus, advantageously, 2/3-PWM does not need those hard-switched transitions that in 3/3-WPM result in the largest contributions to the overall switching losses because of high switched voltages. Considering, e.g., the applied SiC MOS-FET *C3M0021120K* and its detailed switching loss models based on calorimetric measurements [38], averaging the hard-switching energy dissipation over one mains period results in switching losses of $1.7\,\text{W}$ for 2/3-PWM instead of $7.5\,\text{W}$ for 3/3-PWM, i.e., a 77% reduction of switching losses (for PFC operation with unity power factor). Note that furthermore also lower conduction losses (reduced by $8\,\%$ [49]) are expected since 2/3-PWM employs the minimum possible time-varying DC-link current.

III. LOSS-OPTIMAL OPERATION

Whereas 2/3-PWM reduced the CSR-stage switching losses, it requires the DC/DC-stage to operate; on the other hand, the CSR-stage alone can control low output voltages but then needs to operate with 3/3-PWM. It is therefore interesting to consider the loss-optimal operating modes of the 3-Φ bB current DC-link PFC rectifier system (see **Fig. 2**), whose key specifications and circuit parameters are listed in **Tab. I**.

The wide output voltage range ($200\,\text{V}$ to $1000\,\text{V}$) is covered by three operating modes [39], i.e., buck-mode ($V_{out} <$
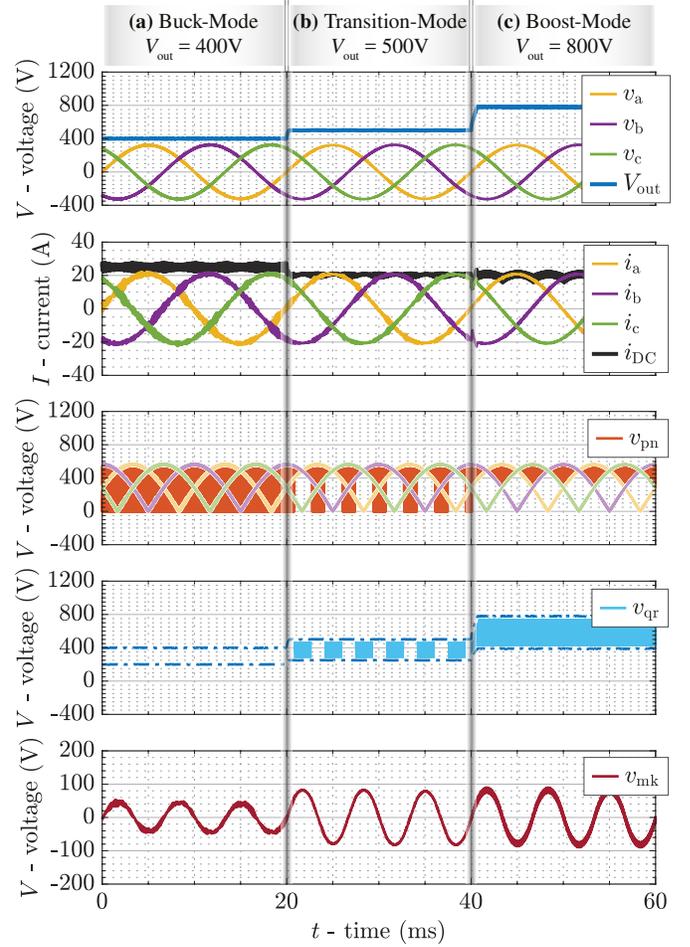

Fig. 6: Simulated key waveforms of the 3-Φ bB current DC-link PFC rectifier system shown in **Fig. 2** when operating in **(a)** buck-mode, **(b)** transition-modem, and **(c)** boost-mode when supplying constant power at different output voltages. The switched DC-side voltage of the CSR-stage, v_{pn}, and the switched input voltage of the DC/DC-stage, v_{qr}, indicate the CSR-stage modulation method (with 2/3-PWM, v_{pn} never attains zero as no zero states are employed) and/or the clamping of the DC/DC-stage. The voltage v_{mk} across the integrated CM filter capacitor C_{CM} verifies that mainly an LF CM voltage appears at the output terminals. Note that v_{qr} is a 3-L switched voltage with the levels of 0, $V_{out}/2$, and V_{out} if the DC/DC-stage is actively switching.

$3/2\hat{V}_{in} = 488\,\text{V}$), boost-mode ($V_{out} > \sqrt{3}\hat{V}_{in} = 563\,\text{V}$), and, in between, transition-mode ($3/2\hat{V}_{in} < V_{out} < \sqrt{3}\hat{V}_{in}$), by collaboratively operating the CSR-stage and the DC/DC-stage; see also the simulated key waveforms in **Fig. 6**. The semiconductor losses, as the main contribution to the total converter, are minimized if the following two criteria are met:

1) The minimum possible DC-link current should be used, which results in minimum conduction losses of the whole system as the DC-link current flows through the turned-on semiconductors of the CSR-stage and the DC/DC-stage, and in the DC-link inductor. The CSR-stage forms the 3-Φ mains currents (see **Section II**), and likewise the DC/DC-stage forms the output DC current, by pulse-width modulating the DC-link current. Thus,

$$i_{DC} \geq \max(|i_a|, |i_b|, |i_c|, I_{out}) \quad (3)$$

must be guaranteed at any moment; equality results in the (potentially time-varying) minimum possible DC-link

current.

2) The number of switching instants and/or the switched voltages/currents should be minimized. Thus, 2/3-PWM of the CSR-stage should be used whenever the DC/DC-stage must operate anyhow because of a high output voltage, or alternatively, the DC/DC-stage should be clamped (i.e., $T_{DC,hp}$ and $T_{DC,hn}$ are permanently on).

These three main operating modes are then explained in detail below.

A. Buck-Mode

If the output voltage is low, i.e., $V_{out} < {}^{3}/{}_{2}\hat{V}_{in} = 488\,\text{V}$, the converter operates in the buck-mode (see **Fig. 6a**). The output voltage can be obtained by the CSR-stage directly stepping down the 3-Φ mains voltages, and no boost functionality is needed, i.e., the switching losses of the DC/DC-stage can be avoided by permanently turning on $T_{DC,hp}$ and $T_{DC,hn}$ (note that constant $v_{qr} = V_{out}$ in **Fig. 6a**). Furthermore, clamping the DC/DC-stage automatically results in

$$i_{DC} = I_{DC,3/3} = I_{out} > \max(|i_a^*|, |i_b^*|, |i_c^*|), \qquad (4)$$

such that the minimum possible DC-link current is applied according to (3). Sinusoidal 3-Φ mains currents are realized by 3/3-PWM of the CSR-stage, i.e., v_{pn} also attains zero (corresponding to the zero switching states) in **Fig. 6a**.

B. Boost-Mode

If the output voltage is high, i.e., $V_{out} > \sqrt{3}\hat{V}_{in} = 563\,\text{V}$, the converter operates in the boost-mode (see **Fig. 6c**). The DC/DC-stage *must* operate to step-up the output voltage of the CSR-stage to higher output voltages. Thus, advantageously, the two converter stages should be operated synergetically/collaboratively: as the DC/DC-stage is needed anyways, it can control the DC-link current to the six-pulse shape defined by

$$i_{DC} = i_{DC,2/3} = \max(|i_a|, |i_b|, |i_c|) > I_{out}, \qquad (5)$$

which allows implementing 2/3-PWM of the CSR-stage with significantly reduced switching losses (see **Section II**). Note that in **Fig. 6c**, the input voltage of the DC/DC-stage, v_{qr}, is now a high-frequency (HF) switched voltage, and on the other hand, the DC-side voltage of the CSR-stage, v_{pn} never attains zero, corresponding to the absence of zero states in 2/3-PWM. The time-varying DC-link current $i_{DC,2/3}$ is also the minimum possible DC-link current according to (3) and hence minimizes the overall conduction losses.

C. Transition-Mode

If the output voltage is in the range of ${}^{3}/{}_{2}\hat{V}_{in} < V_{out} < \sqrt{3}\hat{V}_{in}$, i.e., higher than the buck-mode boundary but lower than the boost-mode boundary, the boost functionality provided by the DC/DC-stage is not needed continuously, but only during parts of the mains period. By selecting the DC-link current as in (3), essentially

$$i_{DC} = \max(I_{DC,3/3}, i_{DC,2/3}) \qquad (6)$$

results and hence the CSR-stage operation alternates between 3/3-PWM and 2/3-PWM accordingly, and the DC/DC-stage is activated only when the boost functionality is required. This is clearly visibly in the simulated v_{pn} and v_{qr} waveforms shown in **Fig. 6b**.

IV. SYNERGETIC CONTROL STRATEGY

A synergetic control strategy of the 3-Φ bB current DC-link PFC rectifier system (see **Fig. 2**), which ensures that two converter stages always operate collaboratively in loss-optimum modes and transitions seamlessly between these modes if the output voltage changes, is presented in this section. Whereas a control method in [40] has been introduced earlier, we present here a simplified and intuitive version (without modulation indices of two stages) that, however, does not sacrifice any functionality. **Fig. 7** shows the corresponding block diagram and highlights the three main functional blocks, i.e., *Output Voltage Control*, *DC-Link Current Reference Generation*, and *DC-Link Current Control*, which are explained in detail in the following subsections.

A. Output Voltage Control

The outermost control loop (see **Fig. 7a**) tracks the output voltage reference V_{out}^* by providing the corresponding power reference P^*. From that, the CSR-stage input reference conductance G^* follows as

$$G^* = \frac{P^*}{\frac{3}{2}\,\hat{V}_{in,meas}^2}. \qquad (7)$$

The 3-Φ sinusoidal mains current references i_a^*, i_b^*, and i_c^* that are then selected proportional to the corresponding measured 3-Φ input voltages v_a, v_b, and v_c such that purely ohmic operation of the 3-Φ mains results. The output current reference I_{out}^* is calculated by dividing P^* by V_{out}^*.

B. DC-Link Current Reference Generation

The selection of the appropriate DC-link current reference (see **Fig. 7b**) is at the core of the proposed synergetic control structure and vital to achieving seamless and automatic transitions between the different operating modes and modulation schemes. As discussed above in **Section III**, in the buck-mode, $i_{DC} = I_{DC,3/3}^* = I_{out}^*$ is used, which results in 3/3-PWM of the CSR-stage while the DC/DC-stage is clamped. In the boost-mode, $i_{DC} = i_{DC,2/3}^* = \max(|i_a^*|, |i_b^*|, |i_c^*|)$ is needed ro realize 2/3-PWM of the CSR-stage. Thus, the overall DC-link current reference is

$$i_{DC}^* = \max(I_{DC,3/3}^*, i_{DC,2/3}^*), \qquad (8)$$

i.e., the DC-link current reference always corresponds to the minimum possible DC-link current leading to reduced switching losses and conduction losses.

C. DC-Link Current Control

Finally, the DC-link current is closed-loop-controlled (see **Fig. 7c**) by comparing the DC-link current reference i_{DC}^* with the measured DC-link current i_{DC}. The deviation is processed
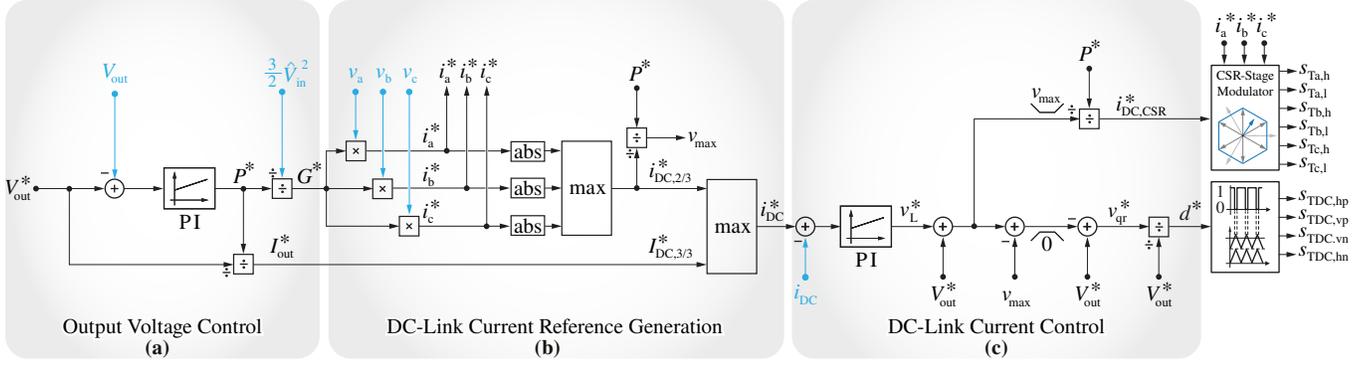
Fig. 7: Block diagram of the proposed synergetic control strategy 3-Φ buck-boost current DC-link PFC rectifier system (see **Fig. 2**). The three main functional blocks enable collaborative operation of the 3-Φ CSR-stage and of the boost-type DC/DC-stage, and seamless transitions between the buck- and boost-modes needed to cover the wide output voltage range. Note that regular sampling is employed to sense only local-average (over one switching period) quantities.

by a PI-controller that then defines the voltage v_L^* across the DC-link inductor L_{DC} needed to counteract the control error. It is material to highlight that v_L^* can be realized by either the CSR-stage *and/or* the DC/DC-stage, e.g., a positive v_L^* can be generated by either an increased output voltage v_{pn} of the CSR-stage or a decreased input voltage v_{qr} of the DC/DC-stage (see **Fig. 2** for the definition of these voltages). Thus, the second part of the DC-link current control structure is designed to democratically assign v_L^* to the CSR-stage or the DC/DC-stage according to the loss-optimal operating modes discussed in **Section III**.

To do so, it is useful to define $v_{max} = P^*/i_{DC,2/3}^*$, i.e., v_{max} is the local average value of the CSR-stage's DC-side voltage v_{pn} that would result if $i_{DC} = i_{DC,2/3}^*$ as needed for 2/3-PWM. Note that v_{max} is thus time-varying, too, to deliver constant power.

If $V_{out}^* < v_{max}$, the CSR-stage alone can regulate the DC-link current and the DC/DC-stage should be clamped, i.e., permanently gating $T_{DC,hp}$ and $T_{DC,hn}$ on. A positive v_L^* can thus be realized by increasing the CSR-stage's DC-side voltage v_{pn}, i.e., a shortening of the zero states used in 3/3-PWM of the CSR-stage. Thus, a positive v_L^* should result in a reduced reference DC-link current $i_{DC,CSR}^*$ fed to the space-vector pulse-width modulator (SVPWM) of the CSR-stage. Following the control diagram and assuming that v_L^* is comparably small, we have

$$i_{DC,CSR}^* = \frac{P_{out}^*}{\min(V_{out}^* + v_L^*, v_{max})} = \frac{P_{out}^*}{V_{out}^* + v_L^*}, \qquad (9)$$

which results in the desired behavior. Likewise, a negative v_L^* results in an increase of $i_{DC,CSR}^*$ and hence in an elongation of the zero vector dwell times. The DC/DC-stage modulation index d^* is calculated as

$$d^* = \frac{-\max(v_L^* + V_{out}^* - v_{max}, 0) + V_{out}^*}{V_{out}^*} = \frac{0 + V_{out}^*}{V_{out}^*} = 1, \tag{10}$$

so that d^* is not affected by v_L^* and ensures that $T_{DC,hp}$ and $T_{DC,hn}$ are turned on continuously.

If, conversely, $V_{out}^* > v_{max}$, only the DC/DC-stage can regulate the DC-link current since the CSR-stage operates with 2/3-PWM, i.e., no zero switching states and, thus, no voltage regulation capability. A positive v_L^* can then be realized by

decreasing the input voltage v_{qr} of the DC/DC-stage. Therefore, the DC/DC-stage modulation index d^* is modified by v_L^* (which, again, is assumed to be comparably small) as

$$d^* = \frac{-\max(v_L^* + V_{out}^* - v_{max}, 0) + V_{out}^*}{V_{out}^*} = \frac{v_{max} - v_L^*}{V_{out}^*}. \tag{11}$$

On the other hand,

$$i_{DC,CSR}^* = \frac{P_{out}^*}{\min(V_{out}^* + v_L^*, v_{max})} = \frac{P_{out}^*}{v_{max}} = i_{DC,2/3}^* \tag{12}$$

results, which ensures 2/3-PWM operation of the CSR-stage.

Note that in the transition-mode, therefore i_{DC} is regulated alternatively by the CSR-stage or by the DC/DC-stage, i.e., v_L^* is realized by either (modified) 3/3-PWM of the CSR-stage as in (9) or by (modified) DC/DC-stage duty cycles as in (11). Importantly, there are no abrupt changes in v_L^* but only different converter stages realize the required v_L^* depending on the (instantaneous) relation of V_{out}^* and v_{max}. Advantageously, the loop gain of the DC-link current control is not affected, and seamless transitions between different operating points are achieved.

V. EXPERIMENTAL VERIFICATION

A $10\,\mathrm{kW}$ hardware demonstrator (see **Fig. 8**) has been built to experimentally verify the proposed synergetic control structure and to comprehensively characterize the conducted EMI performance and efficiency behavior over the wide output voltage and power ranges. Detailed modeling of component losses and volumes, a corresponding Pareto optimization (considering efficiency and power density), and finally a selected design have been presented earlier in [38], [39], considering a compact two-stage EMI filter providing sufficient attenuation, i.e., the maximum required attenuation over the wide output voltage range, to meet the requirements of CISPR 11 class A. Thus, design details are not reiterated here for the sake of brevity. **Tab. I** summarizes the key components of the realized demonstrator.[7]

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[7]Minor differences with respect to the selected design from [38] are due to mechanical/availability considerations. The loss calculations shown in the following employ the loss models from [38] but, of course, consider the actual components' data.
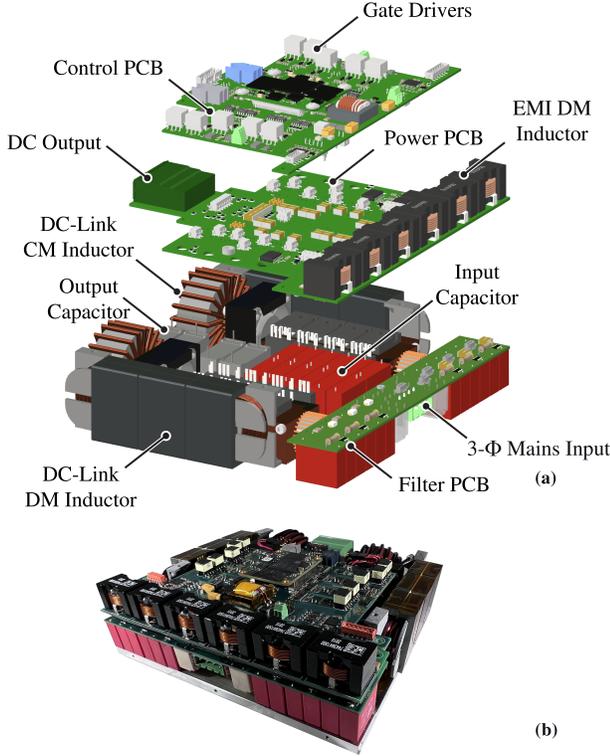
Fig. 8: **(a)** Exploded view of the 10 kW 3-Φ bB current DC-link PFC rectifier hardware demonstrator (see **Fig. 2** for the schematics and **Tab. I** for key components) and **(b)** photo of the realized prototype. The dimensions are $184 \times 172 \times 49\,\text{mm}^3$ ($9.8 \times 5.1 \times 1.9\,\text{in}^3$), resulting in a power density of $6.4\,\text{kW}/\text{dm}^3$ ($107.5\,\text{W}/\text{in}^3$). Operating from the 400 V 3-Φ mains and employing 1200 V SiC (CSR-stage) and 900 V SiC (DC/DC-stage) MOSFETs, a wide output voltage range of 200 V to 1000 V is covered.

Fig. 8 shows an exploded-view 3D CAD rendering and a photo of the 10 kW hardware demonstrator with outer dimensions of $184 \times 172 \times 49\,\text{mm}^3$ ($9.8 \times 5.1 \times 1.9\,\text{in}^3$) and thus a power density of $6.4\,\text{kW}/\text{dm}^3$ ($107.5\,\text{W}/\text{in}^3$). The CSR-stage employs anti-series connections of 1200 V SiC MOSFETs for each bidirectional switch and the 3-L DC/DC-stage uses 900 V SiC MOSFETs. The realized demonstrator is composed of three separate PCBs: the control PCB (Zynq 7000 SoC, gate drivers, measurement data acquisition, etc.), the power PCB (carrying the power transistors, AC-side and DC-side capacitors, etc.), and a dedicated EMI Filter PCB.

A. Experimental Waveforms

Characteristic waveforms of the 10 kW hardware demonstrator are presented in **Fig. 9** for operation in **(a)** buck-mode, **(b)** transition-mode, and **(c)** boost-mode. The phase a voltage v_a, the phase a current i_a, the DC-link current i_{DC}, and the output voltage V_{out} illustrate the desired behavior at the AC input and the DC output. Furthermore, the switched voltage v_{pn} at the output of the CSR-stage clearly indicates the CSR-stage operation with 2/3-PWM or 3/3-PWM. Similarly, the switched voltages v_{qm} and v_{mr} indicate whether the DC/DC-stage operates or is clamped. The measured CM capacitor voltage v_{mk}, mainly consisting of LF components, verifies the function of the integrated CM filter, i.e., suppressing the HF

CM noise at the DC output. Note the close similarity of the measured waveforms to the simulation results shown in **Fig. 6**.

Specifically, **Fig. 9a** presents buck-mode operation with $V_{out} = 400\,\text{V}$, $P_{out} = 10\,\text{kW}$, where the CSR-stage operates with 3/3-PWM and the DC/DC-stage clamps, i.e., $T_{DC,hp}$ and $T_{DC,hn}$ are permanently on as visible from v_{qm} and v_{mr}. **Fig. 9c** shows boost-mode operation with $V_{out} = 1000\,\text{V}$, $P_{out} = 10\,\text{kW}$, where the DC-link current i_{DC} is regulated into the six-pulse shape, i.e., the envelope of the phase current absolute values, needed for 2/3-PWM of the CSR-stage, i.e., v_{pn} never attains zero volt (freewheeling states are not employed), resulting in reduced switching losses of the CSR-stage. However, the DC/DC-stage has to regulate the DC-link current in the boost-mode and control the output voltage at the same time. In the transition-mode operation, the CSR-stage alternatively operates with 2/3-PWM and 3/3-PWM and the DC/DC-stage is democratically activated to shape the DC-link current if needed; this ensures loss-optimal operation.

The proposed control strategy is thoroughly verified by the measurements shown in **Fig. 10**, where the output voltage steps up from 0 V to 800 V with a load resistance of 80 Ω. Automatic and smooth transitions between different the operating modes, i.e., buck-mode, transition-mode, and boost-mode, are achieved, and the loss-optimum modulation (i.e., 2/3-PWM of the CSR-stage if possible; clamped DC/DC-stage otherwise) employed. Note further the smooth start-up, which the current DC-link topology achieves without the need for pre-charging a DC-link capacitor (via pre-charge resistors) as is the case for voltage DC-link converters.

B. Efficiency Measurements

The efficiency of the 10 kW hardware demonstrator shown in **Fig. 8** is measured (Yokogawa WT3000) over the full wide output voltage (from 200 to 1000 V) and output power (from full load down to 25 % load) ranges. Thus, **Fig. 11a** shows the measured efficiency results in dependence of the output voltage and the load, considering the loss-optimum operating mode for each operating point; **Fig. 11b** shows the same information in a 2D contour plot, where in addition the operating points at which the efficiency measurements have been taken are indicated (linear interpolation is used in between). Clearly, the converter features a relatively flat characteristic over the full operating area. High efficiencies, i.e., above 98%, are achieved for a large part of the operating range, i.e., in most of the operating range where output voltages above 400 V and more than 25% of rated load. To further illustrate this, **Fig. 12a** shows efficiency versus output voltage at rated power, and **Fig. 12b** shows efficiency versus output power for different output voltages. A peak efficiency of 98.8% at 520 V and 5 kW can be observed.

It is further worthwhile, for the first time, to experimentally quantify the system-level efficiency improvement when using 2/3-PWM instead of 3/3-PWM in the boost-mode and the transition-mode (note that the boost-type DC/DC stage sensibly *must* be clamped in the buck-mode). **Fig. 11c** shows the measured efficiency when operating with 3/3-PWM in those parts of the operating range where the loss-optimal operation
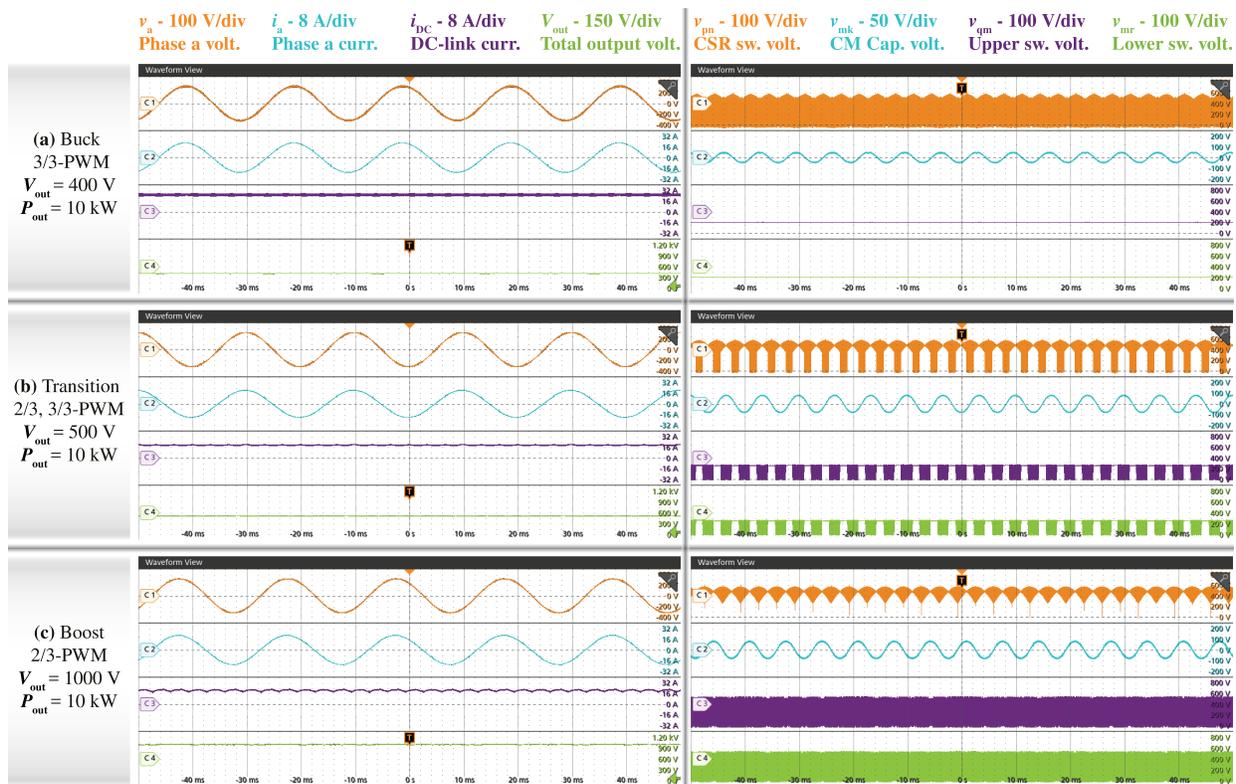
Fig. 9: Experimental waveforms of the converter shown in **Fig. 8**, operating with the proposed synergetic control strategy. **(a)** Buck-mode, where the CSR-stage uses 3/3-PWM to step down the mains voltage to the low output voltage and the DC/DC-stage is clamped (note that v_{qm} and v_{mr} are constant). **(b)** Transition-mode, where the CSR-stage changes between 3/3-PWM and 2/3-PWM, and the DC/DC-stage is democratically activated only when the boost functionality is required. **(c)** Boost-mode, where the DC/DC-stage regulates the DC-link current i_{DC} to the six-pulse shape needed for 2/3-PWM of the CSR-stage (note the absence of the zero level in v_{pn}).
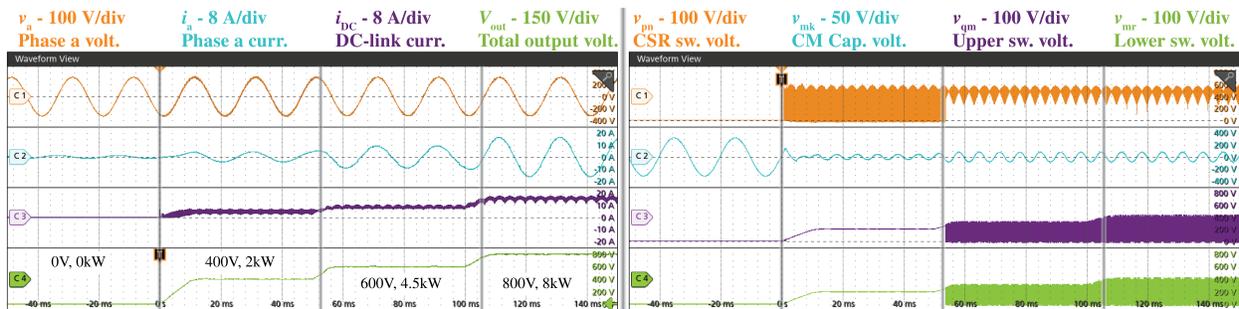

Fig. 10: Experimental waveforms of the converter shown in **Fig. 8** when supplying a resistive load of $80\,\Omega$ and the output voltage set point is changed from $0\,V$ to $800\,V$, i.e., covering a wide output voltage range. Automatic and seamless transitions from buck-mode to boost-mode are achieved by the proposed synergetic control strategy (see **Fig. 7**). Note also the very smooth start-up.

would employ 2/3-PWM. **Fig. 11d** then shows the efficiency improvements between the proposed loss-optimum operation (using 2/3-PWM whenever possible) and the conventional approach that does never employ 2/3-PWM, indicating improvements of up to 1% in the transition-mode and the boost-mode (again, no difference is expected in the buck-mode).

Finally, **Fig. 13** provides the calculated loss breakdowns versus **(a)** output voltage at rated power, **(b)** output power at $400\,V$ (buck-mode), and **(c)** output power at $800\,V$ (boost-mode). The loss modeling has been presented earlier [38], but the calculation results shown here have been updated to reflect the components actually used in the demonstrator (see **Tab. I**). Moreover, the loss breakdowns provide the following

observations:

- Conduction losses account for a significant proportion of the total losses. As these reduce with the square of the current (and accordingly with the power), a relatively flat efficiency characteristic of the converter results.
- In buck-mode, the CSR-stage operating with 3/3-PWM contributes considerable switching losses whereas the DC/DC-stage only generates conduction losses and zero switching losses due to clamping.
- In boost-mode, 2/3-PWM is used for the CSR-stage and leads to almost negligible switching losses. On the other hand, the DC/DC-stage generates comparably high switching losses because of the high switched voltage
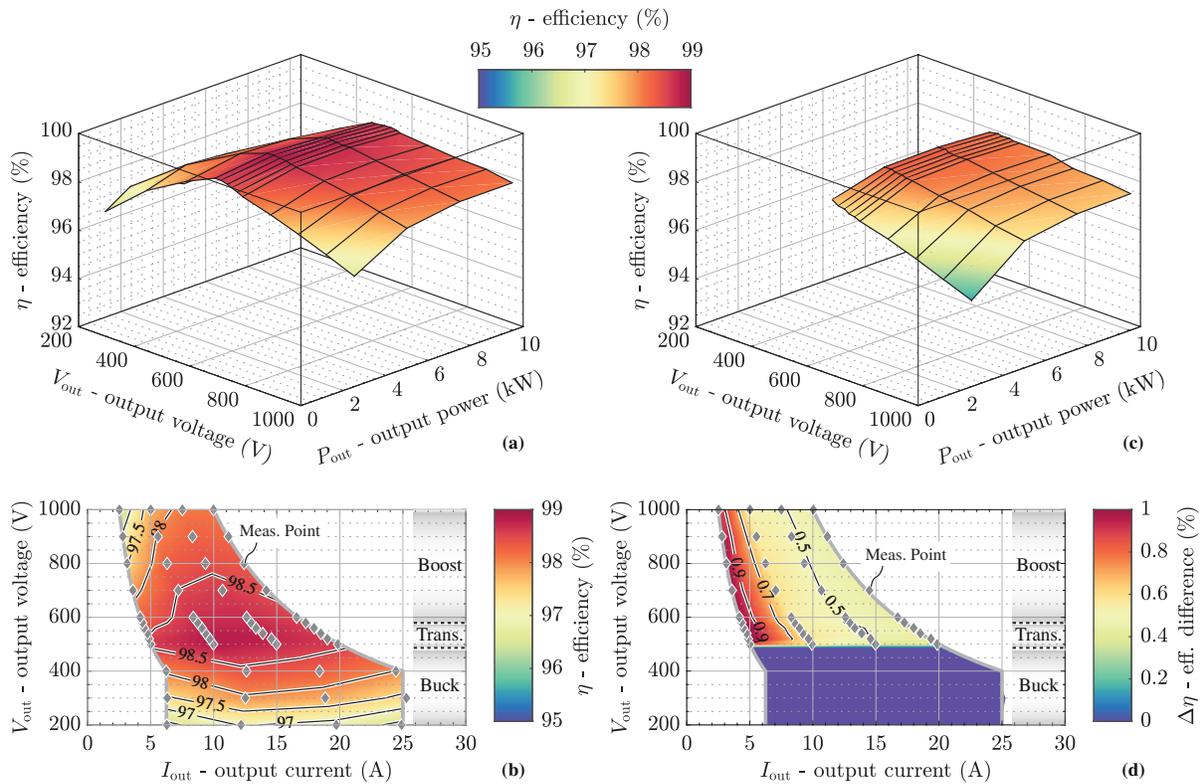
Fig. 11: Measured (Yokogawa WT3000) efficiencies of the realized 10 kW hardware demonstrator shown in **Fig. 8** when operating over a wide output voltage (200 V to 1000 V) and output power (from full load to 25 % load) ranges, using **(a)** the proposed loss-optimal modulation scheme with 2/3-PWM of the CSR-stage whenever possible; **(b)** shows the corresponding efficiency contours and indicates the measured operating points (linear interpolation in-between). **(c)** shows the measured efficiency of conventional operation using 3/3-PWM instead of 2/3-PWM where applicable (i.e., in the boost-mode and the transition-mode). **(d)** quantifies the efficiency difference between **(a)** the proposed and **(c)** state-of-the-art methods, highlighting up to 1% efficiency improvement in the transition-mode and the boost-mode. Note that no efficiency difference is expected in the buck-mode, where 3/3-PWM must be used in all cases. Thus, **(c)** does not show efficiencies for buck-mode operating points; the efficiency difference in that operating range is always zero (see **(d)**).
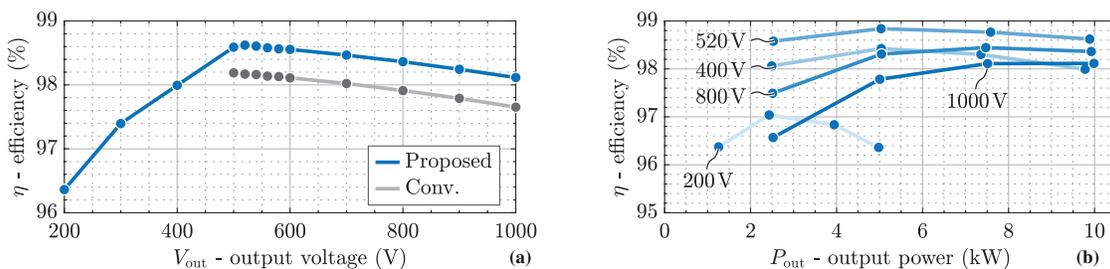

Fig. 12: Measured (Yokogawa WT3000) efficiency curves of the realized 10 kW hardware demonstrator shown in **Fig. 8**. **(a)** Efficiency versus output voltage V_{out} at rated power (or rated output current below 400 V, see **Fig. 1**), and **(b)** efficiency versus output power P_{out} (using the proposed loss-optimal modulation scheme). A peak efficiency of 98.8% when $V_{out} = 520$ V and $P_{out} = 5$ kW is achieved.
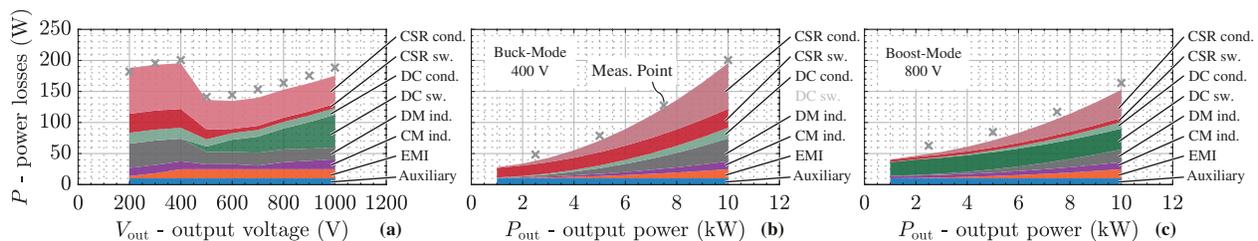

Fig. 13: Calculated loss breakdowns of the converter shown in **Fig. 8** and loss-optimal operation, in **(a)** for different output voltages V_{out} and rated power (or rated output current below 400 V), in **(b)** for buck-mode operation ($V_{out} = 400$ V) and varying power P_{out}, and in **(c)** for boost-mode operation ($V_{out} = 800$ V) and varying power. The measured (Yokogawa WT3000) total losses are in excellent agreement with the calculations.

(boost-mode).

Fig. 13 also indicates the measured (Yokogawa WT3000)

losses, and a very close match between calculation and measurement can be observed.
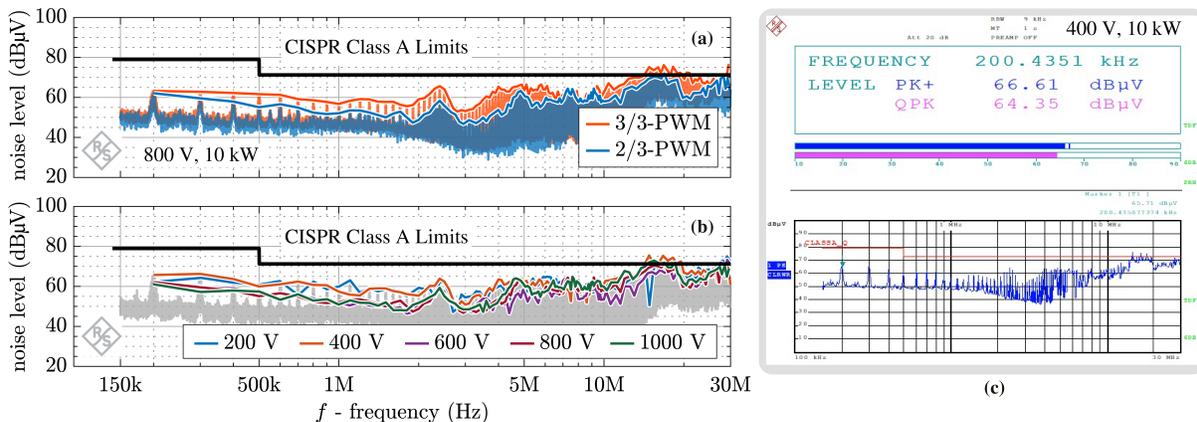
Fig. 14: Measured conducted EMI noise emission spectra of the realized 10 kW hardware demonstrator shown in **Fig. 8**. The Rhode & Schwar ESPI3 test receiver uses the CISPR 11 peak (PK) detector with resolution bandwidth of 9 kHz, 4 kHz step size, and 1 ms measurement time. The local peak values are connected by colored envelopes for easier comparisons between different operating points. **(a)** Comparison of the EMI noise emissions between 2/3-PWM and 3/3-PWM when operating in the boost-mode, i.e., $V_{out} = 800$ V, $P_{out} = 10$ kW, indicating a maximum reduction of 9.7 dBμV at 2.4 MHz when using 2/3-PWM instead of 3/3-PWM. **(b)** Final conducted EMI pre-compliance test results of the demonstrator using the loss-optimum operating modes for each operating point (different output voltages, rated power); note that the minor violations of the CISPR 11 Class A limit above 10 MHz could likely be d by placing the converter in a grounded housing. **(c)** Screenshot directly taken from the EMI test receiver at the worst-case operating point ($V_{out} = 400$ V, $P_{out} = 10$ kW), indicating the quasi-peak (QP) value of 64.4 dBμV at 200 kHz.
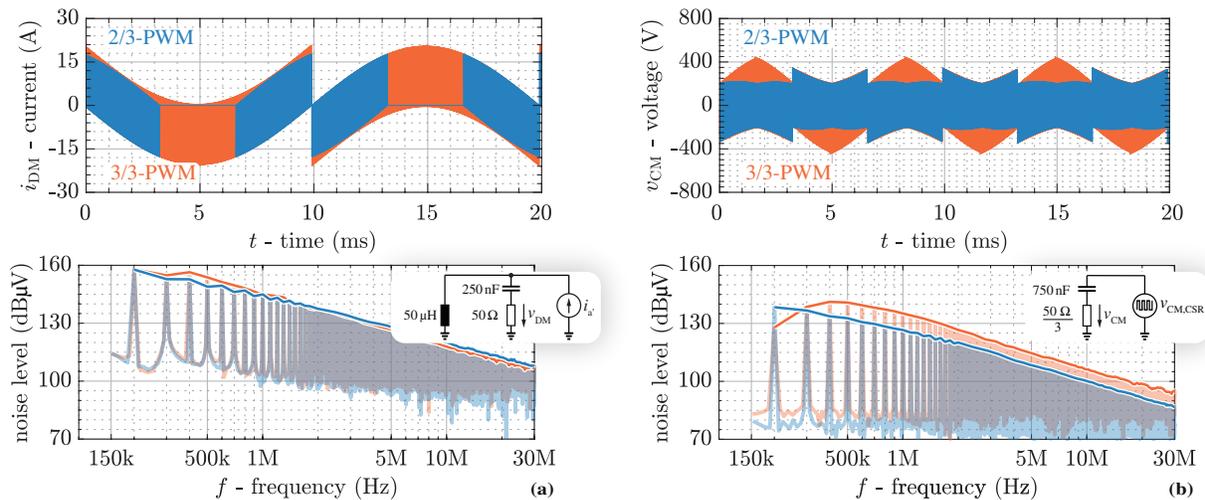

Fig. 15: Comparison of calculated HF **(a)** DM and **(b)** CM EMI noise waveforms and spectra (as they would appear at the LISN without an EMI filter present) for operation with 2/3-PWM **(blue)** or 3/3-PWM **(orange)** in the boost-mode at $V_{out} = 800$ V and $P_{out} = 10$ kW.

C. EMI Measurement

Conducted EMI pre-compliance tests have been carried out to assess the compliance of the realized 10 kW hardware demonstrator (see **Fig. 8**) with the limits set forth in CISPR 11 Class A for the frequency range of 150 kHz to 30 MHz. The test setup consists of a Rhode & Schwarz ESH2-Z5 three-phase LISN and a Rhode & Schwarz ESPI3 EMI test receiver.

First, the differences in the conducted EMI emission characteristics when operating with 2/3-PWM or, conventionally, 3/3-PWM for boost-mode operating points are compared. **Fig. 14 (a)** presents EMI measurement results when operating in the boost-mode ($V_{out} = 800$ V, $P_{out} = 10$ kW) with the two different modulation schemes used in the CSR-stage. In general, 2/3-PWM results in lower noise levels, with a maximum reduction of 9.7 dBμV at 2.4 MHz. This can be explained by the difference between DM/CM noise sources:

Fig. 15 first presents the HF DM/CM noise source waveforms generated by 2/3-PWM and 3/3-PWM, i.e., the switched current $i_{a'}$ (see **Fig. 2**), and the CSR-stage CM voltage $v_{CM,CSR} = (v_{pk} + v_{nk})/2$ (see [38] for a detailed analysis; note that the CM noise generated by the DC/DC-stage is neglected here since the focus is on comparing the EMI performances of different CSR-stage modulation schemes). To compare the required EMI filter efforts, the DM and CM voltage spectra that would be measured by a LISN in the absence of an EMI filter are provided. The DM noise source can thus be represented by the voltage that would appear at the LISN's 50 Ω measurement resistor if $i_{a'}$ would directly flow in this resistor. On the other hand, the CM voltage defined above is directly the relevant noise source if a comparably large parasitic capacitance of the converter's output to PE is assumed as a worst case. The thus calculated noise spectra (see **Fig. 15**) indicate that 2/3-PWM results in a reduction of the DM noise

of up to $6\,\mathrm{dB\mu V}$ (at $500\,\mathrm{kHz}$). Regarding the CM noise, the maximum reduction is similar, i.e., $6\,\mathrm{dB\mu V} \sim 8\,\mathrm{dB\mu V}$, but observed for (almost) all frequency components. Hence, it can be assumed that mainly the lower CM noise, which is a direct consequence of the CSR-stage not using zero states with 2/3-PWM [39], contributes to the overall lower noise emissions of the converter operating with 2/3-PWM compared to 3/3-PWM. This implies further that a converter originally designed without considering 2/3-PWM can advantageously be operated with 2/3-PWM (by, essentially, only changing the control method) without the need for a redesign of the EMI filter.

Moreover, considering the loss-optimum operation, **Fig. 14b** shows conducted EMI noise emission measurements of the $10\,\mathrm{kW}$ demonstrator over the full output voltage range at rated power (note that the output current limit restricts the power to $P_\mathrm{out} = 5\,\mathrm{kW}$ for the operating point at $V_\mathrm{out} = 200\,\mathrm{V}$). Because the designed EMI filter (see **Tab. I**) achieves similar DM and CM attenuation, e.g., roughly $110\,\mathrm{dB\mu V}$ at $200\,\mathrm{kHz}$ according to the detailed discussion in [38], and because of the higher DM noise emission levels for the exemplary operating point discussed in the context of **Fig. 15**, it is likely that the DM noise dominates in the measurement results, especially when the CSR-stage operates with high modulation indices. Thus, focusing on the measured noise at $200\,\mathrm{kHz}$, i.e., the first harmonic of the switching frequency that lies inside of the regulated frequency range, it is observed that:

- Higher noise results for operating points in the buck-mode, e.g., $V_\mathrm{out} = 200\,\mathrm{V}$ or $400\,\mathrm{V}$, than for operating points in the boost-mode, e.g., $V_\mathrm{out} = 600\,\mathrm{V}$, $800\,\mathrm{V}$, or $1000\,\mathrm{V}$, since a higher DC-link current, i.e., a constant DC-link current of $25\,\mathrm{A}$ in the buck-mode instead of a six-pulse-shaped DC-link current with a peak value of $20.5\,\mathrm{A}$ in the boost-mode, must be used.
- The worst case at $400\,\mathrm{V}$ is expected by comparing RMS values of the HF switched current $i_\mathrm{a'}$, i.e., $10.5\,\mathrm{A}$ at $200\,\mathrm{V}$, $10.8\,\mathrm{A}$ at $400\,\mathrm{V}$, and $6.8\,\mathrm{A}$ at $800\,\mathrm{V}$.
- Similar EMI noise spectra are measured for the three operating points in boost-mode since the CSR-stage operates identically with 2/3-PWM and thus with the same DC-link current. These results indicate that the DC/DC-stage does not strongly affect the AC-side EMI performance.

Finally, considering the worst-case operating point at $V_\mathrm{out} = 400\,\mathrm{V}$ and $P_\mathrm{out} = 10\,\mathrm{kW}$, **Fig. 14c** shows a screenshot of the EMI test receiver with a quasi-peak (QP) measurement result of $64.4\,\mathrm{dB\mu V}$ at $200\,\mathrm{kHz}$, which indicates compliance with CISPR 11 Class A.

VI. Conclusion

Targeting advanced AC/DC front-end converters for EV charger applications, this paper thoroughly studies and analyzes a three-phase (3-Φ) buck-boost (bB) current DC-link PFC rectifier that consists of a 3-Φ buck-type current-source rectifier (CSR)-stage cascaded by a 3-L boost-type DC/DC-stage via a shared DC-link inductor. An ultra-wide output voltage range, i.e., from $200\,\mathrm{V}$ to $1000\,\mathrm{V}$, can be covered

by three loss-optimal operating modes: in the buck-mode (for low output voltages), the CSR-stage operates with Reduced Common-Mode (RCM) 3/3-PWM and the DC/DC-stage is clamped to avoid switching losses; in the boost-mode (for high output voltages), the CSR-stage operates with 2/3-PWM, i.e., only two out of three phases switch within one switching period such that the CSR-stage bridge-legs switch less frequently, and advantageously only in those respective sectors of the main periods where the switching occurs at relatively low voltages and currents; at the same time, still sinusoidal grid currents are achieved by using the DC/DC-stage to shape the DC-link current to follow the typical six-pulse shape given by the maximum absolute values of the 3-Φ mains currents. Furthermore, a simple and intuitive synergetic control strategy is proposed to operate the CSR-stage and the DC/DC-stage collaboratively in the loss-optimum operating modes, and to achieve an automatic, seamless transition between these loss-optimal operating modes when the output voltage changes. In particular, this also ensures loss-optimum operation in the transition-mode (for output voltages between buck-mode and boost-mode), where the minimum possible DC-link current is always ensured and the system hence seamlessly and democratically transitions between 3/3-PWM and 2/3-PWM several times per mains period.

A compact $10\,\mathrm{kW}$ hardware demonstrator with a power density of $6.4\,\mathrm{kW/dm^3}$ ($107.5\,\mathrm{W/in^3}$) is presented and used to verify, for the first time, the key functionality of the proposed synergetic control method. Then, comprehensive efficiency measurements over the full output voltage and power ranges confirm a flat efficiency characteristic (higher than 98% for most operating points with output voltages above $400\,\mathrm{V}$ and more than 25% of rated load), and a peak efficiency of 98.8% at $V_\mathrm{out} = 520\,\mathrm{V}$ and $P_\mathrm{out} = 5\,\mathrm{kW}$ (partial load). These measurements agree closely with the calculation results presented earlier. Again, for the first time, the efficiency improvement of 2/3-PWM over 3/3-PWM on the system-level, i.e., including a DC/DC-stage, has been experimentally confirmed to be up to 1%. Finally, the conducted EMI pre-compliance tests reveal that, for a given operating point where both PWM schemes are applicable, 2/3-PWM results in lower noise emissions than 3/3-PWM. Using the loss-optimum operating modes, measurements taken over the full output voltage range and rated power indicate compliance with CISPR 11 Class A.

All in all, current DC-link buck-boost PFC rectifiers such as the system presented herein are promising realization options for future EV chargers that require a wide output voltage range, high efficiency, and compact size.

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