A Novel Low-Loss Modulation Strategy for High-Power Bi-directional Buck+Boost Converters

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Abstract — A novel low-loss, constant-frequency, zero-voltage-switching (ZVS) modulation strategy for bi-directional, cascaded, buck-boost DC/DC converters, used in a hybrid electrical vehicle (HEV), is presented and its benefits over state-of-the-art converters and soft-switching solutions are discussed in a comparative evaluation. To obtain ZVS with the purposed modulation strategy, the buck+boost inductance is selected and the switches are gated in a way that the inductor current has a negative offset current at the beginning and the end of each pulse period. This allows the MOSFET switches to turn on when the anti-parallel body diode is conducting. As the novel modulation strategy is a software-only solution, there are no additional expenses for active or passive components compared to conventional modulation implementations. Furthermore, an analytical and simulation investigation predicts an excellent efficiency over the complete operating range and a higher power density for a multi-phase converter equipped with the low-loss modulation. Experimental measurements performed with a converter prototype verify the mode of operation and the ZVS principle.

I. INTRODUCTION

Drive systems for Hybrid Electrical Vehicles (HEVs) include energy storage elements such as batteries, and these are typically connected by DC/DC converters to a common DC link that supplies the main motor inverter. For feeding back the braking energy, a bi-directional energy flow has to be implemented. Depending on the cell number and characteristics of the battery, the battery voltage range may overlap with the nominal DC link voltage range. In this case, the DC/DC converter has to be able to function in both the buck and boost operating modes.

Furthermore, a converter for this application has to meet the prevalent automotive requirements, such as being a low cost design, and minimizing the component sizes and count. Fixed frequency operation is desired due to EMI restrictions and a high efficiency over a wide output power range, as well as a highly compact design and a low overall weight are required.

One commonly used converter topology for this application is the hard-switched, cascaded, buck+boost converter [1][2]. In order to improve efficiency, silicon carbide (SiC) technology could be applied [3]. Furthermore, there is a wide variety of soft-switching auxiliary circuits to extend this converter topology, including the Auxiliary Resonant Commutated Pole (ARCP) [4][5], Zero Current Transition (ZCT) [6][7] or Snubber Assisted Zero Voltage and Zero Current Transition (SAZZ) [8] methods.

An alternative approach to achieve ZVS of the cascaded buck+boost converter (Fig. 1) is to implement a novel low-loss modulation strategy. This is a software-only solution that does not need any additional active or passive components and therefore offers an increased efficiency while maintaining a low component count and simplicity of the power electronics circuit.

In this paper, the state-of-the-art soft-switching additions for the cascaded buck+boost converter, and the further soft-switching concepts and benefits of the proposed alternative modulation method are discussed (**Section II**). In **Section III** a detailed description of the operating principle of the novel low-loss modulation method, the requirements for ZVS operation and an optimized switching strategy are presented. Analytical results, including an efficiency comparison of the conventional hard-switched and the proposed soft-switched buck+boost converter and results of a converter volume optimization are given in **Section IV**. Simulation and experimental results, which verify the method of operation, are presented in **Section V.**

II. TOPOLOGIES

A problem of the cascaded buck+boost converter, shown in Fig. 1, operated in continuous conduction mode (CCM) and with conventional pulse width modulation (PWM) is the significant switch turn-on loss caused by the reverse recovery of the anti-parallel diode of the complementary switch in the half-bridge. These higher losses typically result in an overall efficiency of approximately 92% [2].

In the literature, several ways to improve the loss behavior can be found: First of all, the internal switch anti-parallel diodes (body diodes) may be substituted by low recovery charge silicon carbide types to avoid switching losses caused by reverse recovery. In combination with multi-phase technology, greater efficiency and power density could be achieved [3]. Besides the fact that SiC

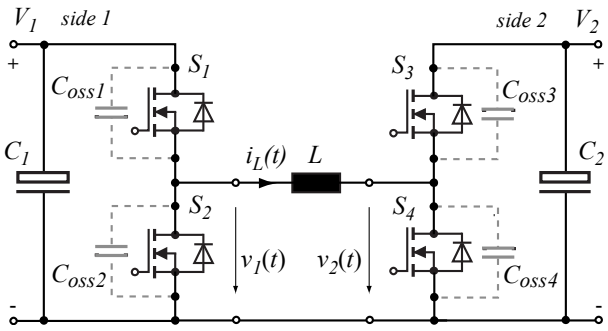

Fig 1: Cascaded buck+boost converter for bi-directional power-flow, shown with parasitic MOSFET output capacitances $C_{oss,1}$.

technology is expensive, a hard-switched converter is often not a preferred solution because of increased EMI emissions caused by high rate of voltage change (*dV/dt*), which involves the filter design. Therefore, secondly, the transistors should be operated such that

a) Zero Current Switching (ZCS)
b) Zero Voltage Switching (ZVS)
c) and/or low switching losses

are achieved. When lowering switching losses by these soft-switching techniques, the rate of voltage change is reduced at the same time. Thus, lower EMI emissions are also expected. On the other hand the switching frequency f_s may be increased without severe impact on switching losses, resulting in a smaller volume of the passive components.

A. Auxiliary Circuitry

A variety of soft-switching solutions applicable to the half bridges used in the cascaded buck+boost converter have been presented in the literature [4]-[9]. These are based on the following fundamental ZVS or ZCS concepts:

- Synchronous Resonant DC Link (SRDCL)
- Auxiliary Resonant Commutated Pole (ARCP)
- Zero Current Transition (ZCT)
- Snubber Assisted Zero Voltage and Zero Current Transition (SAZZ).

In these concepts, the basic operating principle is to conduct the main inductor current in an additional resonant circuit such that the main switch is operated with ZVS and/or ZCS, where the resonant process is initiated by auxiliary switches.

The SRDCL [9] suffers from additional components in the main current path, high peak currents in the resonant circuit and a resonant overshoot of the DC link voltage of approximately 1.5 times the DC link voltage. ARCP [4][5], ZCT [6][7] and SAZZ [8] do not have the drawback of a resonant overshoot, but the auxiliary switch peak currents are greater than the main inductor current.

All of the mentioned solutions require additional active and passive components as well as gate drive circuitry. For instance, four auxiliary switches are employed in the case of ARCP, ZCT or SAZZ plus the resonant capacitors and inductors and four additional diodes in the case of SAZZ, when applied to the cascaded buck+boost converter. Another drawback is the PWM duty cycle limitation caused by the time consumed by the resonant transition.

B. Resonant Converters

Besides soft-switching extensions to well known hard-switched converters, there are a number of independent resonant, soft-switching, bi-directional buck-boost converter concepts like the constant-frequency zero-voltage-switching quasi-square-wave (CF-ZVS-QSC) converter [10], SEPIC converter [1][11] or the zero-voltage zero-current switching (ZVZCS) converter presented in [11].

Compared to the proposed converter with low-loss modulation method, the main drawbacks of these converters are a doubled switch blocking voltage stress and diode recovery losses in case of the SEPIC [11], a larger number of passive components as well as a larger inductance value for the main inductor in the SEPIC and ZVZCS topology [10]. Furthermore, SEPIC and ZVZCS use a capacitive energy transfer that performs badly in high-power applications. Other drawbacks of resonant converters are variable switching frequency, which complicate EMI filter design, or limitations in operating range for soft-switching.

III. LOW-LOSS MODULATION STRATEGY

To overcome the above-mentioned drawbacks like additional component effort, capacitive energy transfer or variable switching frequency, a new constant-frequency zero-voltage switching modulation strategy is proposed.

A. Operating Principle

In conventional PWM for the cascaded buck+boost converter only one of the two half bridges is switched and static control signals are applied to the switches of the other bridge leg [2].

In contrast, with the proposed new modulation method, each of the four switches S_1 to S_4 is turned on and off exactly once per pulse period $T_p = 1 / f_s$. Turn-on is accomplished under ZVS when the anti-parallel body diode is conducting. A negative inductor offset current $-I_0$ is needed to fulfill this condition (Fig. 2). The pulse period T_p can be divided into four modes according to the four switching states of S_1 to S_4, as shown in Fig. 2 and Fig. 3.

At the beginning of time period $t_0 \le t < t_1$ the switch S_2 is conducting and therefore is turned off under ZVS. The negative inductor current $i_L(t)$ charges the parasitic drain-source capacitance C_{oss2} of S_2 and discharges C_{oss1} respectively. The body diode of S_1 takes over $i_L(t)$ and S_1 can now switched on under ZVS and conducts the current when $i_L(t)$ becomes positive (Fig. 3 (a)). Due to the applied inductor voltage $v_L(t) = V_1$ the inductor current rises in this time period.

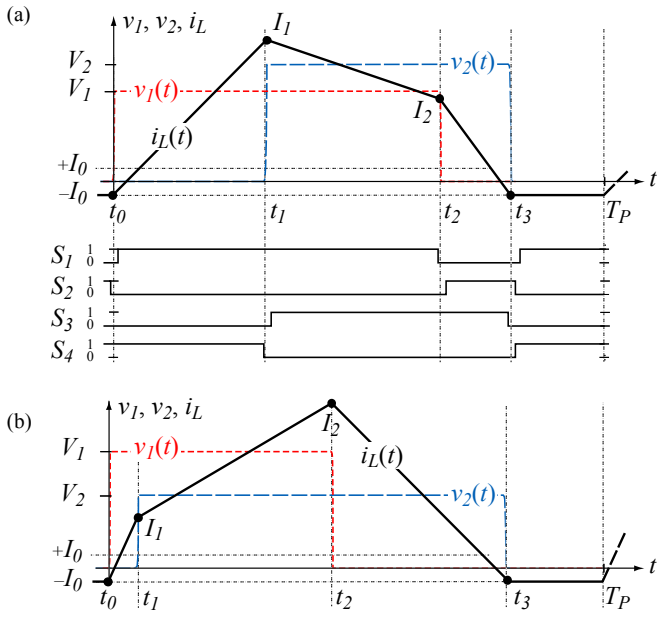

Fig. 2: Basic timing diagram for switch S_1 to S_4 control signals and inductor current i_L for boost operation ($V_2 > V_1$) (a) and basic timing diagram for buck operation ($V_2 < V_1$) (b).

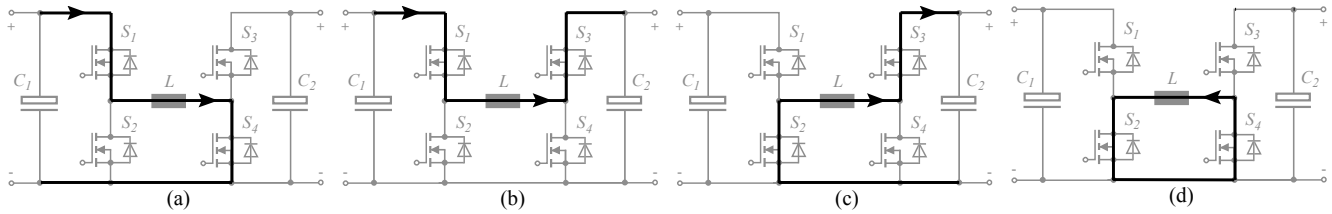

Fig. 3: Inductor current flow for time intervals $t_0 < t < t_1$ (a), $t_1 < t < t_2$ (b), $t_2 < t < t_3$ (c) and $t_3 < t < T_p$ (d). Current direction reverses in (a) and (c) as can be seen in Fig 2, which is not shown for the reason of simplicity.

At $t = t_1$, S_4 is conducting, therefore turned off under ZVS and $i_L(t)$ charges C_{oss4} and discharges C_{oss3} respectively. Again, S_3 can be turned on under ZVS. The applied inductor voltage $v_L(t) = V_1 - V_2$ either causes i_L to rise (buck operation) or fall (boost operation) during the time period $t_1 \leq t < t_2$ depending on V_1 and V_2.

The ZVS principle also applies to the remaining two switching actions at $t = t_2$ (S_1 is turned off and S_2 is turned on) and $t = t_3$ (S_3 is turned off and S_4 is turned on).

In the last time period $t_3 < t < T_p$ the switches S_2 and S_4 are turned on and the switches S_1 and S_3 are turned off, so that the current $i_L(t)$ circulates in the power circuit as shown in Fig. 3 (d). This is to keep the switching frequency constant and to provide the negative offset current needed for ZVS at the beginning of the subsequent pulse period.

B. *Calculation of the switching times*

Starting with the basic inductor current waveforms as depicted in Fig. 2 for buck and boost operation, assuming constant voltages V_1 and V_2 and neglecting resistances of the inductor and the switches S_i, the differential equation

$$v_L(t) = v_1(t) - v_2(t) = L \cdot \frac{d}{dt} i_L(t) \qquad (1)$$

is solved in the four time intervals and yields:

$$t_1 - t_0 = L \cdot \frac{I_0 + I_1}{V_1} \qquad (2)$$

$$t_2 - t_1 = L \cdot \frac{I_2 - I_1}{V_1 - V_2} \qquad (3)$$

$$t_3 - t_2 = L \cdot \frac{I_0 + I_2}{V_2} . \qquad (4)$$

The average power P_{tr} transferred from converter *side 1* to *side 2* is calculated from

$$P_{tr} = \frac{1}{T_p} \cdot \int_{t_0}^{T_p} v_1(t) \cdot i_1(t) dt . \qquad (5)$$

The integral (5) can be solved for the current waveform depicted in Fig. 2 and $t_0 = 0$:

$$P_{tr} = \frac{V_1}{T_p} \cdot \int_0^{t_2} i_L(t) dt = \frac{V_1}{2 \cdot T_p} \left((I_1 + I_2) \cdot t_2 - (I_0 + I_2) \cdot t_1 \right). \qquad (6)$$

The set of equations (2)-(4), (6) with unknowns t_1, t_2, I_1, I_2 may be solved to calculate the switching times t_1, t_2 for the desired operating point (V_1, V_2, P_{tr}) and a given time t_3. Furthermore, the maximum of P_{tr} is calculated as

$$P_{tr,max}(t_3) = \frac{V_1 V_2 \cdot \left(I_0^2 L^2 - 2 I_0 L \cdot (V_1 + V_2) \cdot t_3 + V_1 V_2 \cdot {t_3}^2 \right)}{2 \cdot L \cdot T_p \cdot \left(V_1^2 + V_1 V_2 + V_2^2 \right)} . \qquad (7)$$

The inductance of the buck+boost inductor L has to be derived from (7) for a given operating voltage and power range and $t_3 = T_p$ in such a manner that $P_{tr,max}$ will never be exceeded, otherwise the constraints for soft switching will be violated. The maximum inductance L depends on the minima of V_1 and V_2 and the rated converter peak power $P_{max} = P_{tr,max}(T_p)$ as shown, exemplarily, in Fig. 4.

C. *Optimized Switching Pattern*

As stated before, there is the degree of freedom to choose the switching time t_3 for a given converter operating point. An example is depicted in Fig. 5: Assuming a exemplary current waveform (marked by $-I_0$, I_1, I_2), there are two possibilities to increase P_{tr}. Firstly, the switching time t_3 could be kept constant and the times t_1 and t_2 adjusted (waveform B). Secondly, the switching time t_3 could be shifted towards the end of the switching period T_p (waveform A). This is preferred because of a lower peak and RMS inductor current and thus lower inductor losses.

Besides the considerations for a low RMS current, a continuous variation of $t_1 \ldots t_3$ without any steps is desired over the operating voltage and power range for the reason of steady control behavior of the modulator and a low-error

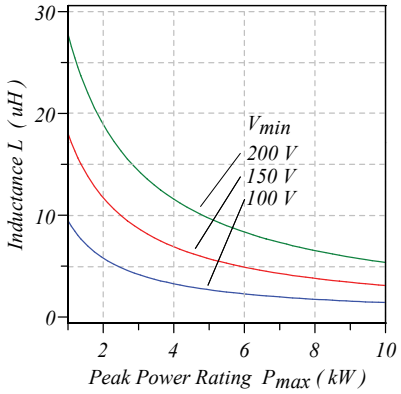

Fig. 4: Maximum inductance L, shown for $V_{1,min} = V_{2,min} = V_{min}$, $I_0 = 10$A, and $f_s = 100$kHz as function of the converter peak power rating P_{max}.

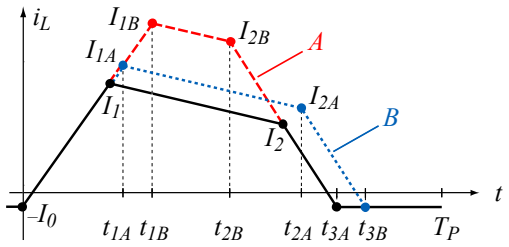

Fig. 5: Possibilities to increase transferred power P_{tr}: Keeping t_3 constant (waveform A) and shifting t_3 towards the end of the switching period T_p (waveform B).

implementation of a three-dimensional, lookup-table-based interpolation of the switching times. To address both requirements, a time calculation scheme is derived for a given power P_{tr}:

- The minimum of t_3 is calculated by differentiation of V_1 and V_2 at the limit of ZVS operation ($I_1 = +I_0$ for buck operation and $I_2 = +I_0$ for boost operation respectively) and is used as a initial value $t_{3,min}$ for t_3. The initial value is normally applicable at the upper ends of the operating voltage range.
- If the energy $E_{tr} = P_{tr} \cdot T_p$ could not be converted within $t_0 < t < t_{3,min}$, t_3 is shifted towards the end of the pulse period at the limit of ZVS operation until the transfer of E_{tr} for any combination of V_1 and V_2 is possible (cf. Fig. 5, waveform A).
- When t_3 is shifted that far to match T_p, t_1 and t_2 are adjusted as depicted in Fig. 5, waveform B.

The calculated, normalized values for $t_1 \ldots t_3$ for a voltage transfer ratio of $V_2 / V_1 = 2$ and $V_{2,max} = 450$V are shown in Fig. 6.

D. *Ensuring ZVS condition*

The minimum absolute value needed for I_0 depends on the resonant circuit formed by L and the MOSFET output capacitances C_{oss} of the affected half-bridge as well as the converter input and output voltage levels V_1 and V_2, which excite the LC-circuit:

$$I_0 \geq \max(V_{1\max}, V_{2\max}) \cdot \sqrt{\frac{C_{oss}}{L}} \qquad (8)$$

If the condition (8) is true, the energy stored in the inductor L at turn-off of a switch is large enough to completely transfer the charge between the both parasitic MOSFET output capacitances of the half-bridge, so that the complementary switch of the half-bridge can be turned on at zero voltage. The same applies to the absolute value of $i_L(t)$ at $t = t_1$ and $t = t_2$ inducing the conditions:

$$I_1 \geq I_0 \quad \text{and} \quad I_2 \geq I_0 \qquad (9)$$

It should be noted that (8) is an approximation, since C_{oss} shows a nonlinear, voltage-dependent characteristic. Furthermore, the number of paralleled MOSFETs has to be taken into consideration.

A drift of i_L below $-I_0$ in the time period $t_3 < t < T_p$ due to component nonlinearity or inexact timing must be avoided to keep conduction losses low. An accurate high-speed zero-crossing detection could be used to exactly determine the time t_3.

Another option, which is implemented in the converter prototype, is to monitor the half-bridge voltages $v_1(t)$ and $v_2(t)$ with high-speed analog comparators to detect a zero voltage level. For instance, i_L is falling in time period $t_2 < t < t_3$. When i_L becomes negative the body diode of S_4 starts conducting and $v_2(t)$ steps to zero, causing the comparator output to change. This information is then used to turn on S_4 under ZVS.

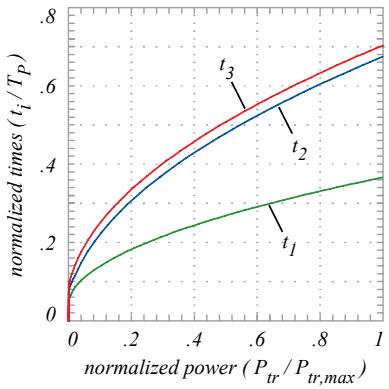

Fig. 6: Normalized output power $P/P_{tr,max}$ and times t_i/T_p for $V_2=V_{2,max}$ and a voltage transfer ratio of $V_2/V_1=2$.

IV. ANALYTICAL RESULTS

A. *Efficiency Comparison*

For comparison of the novel modulation strategy to the hard-switched cascaded buck+boost topology operated with conventional PWM, the semiconductor conduction and switching losses are analytically calculated based on measured switching losses of two MOSFETs in half-bridge configuration and V_{max} = 450V. Figure 7 shows an improvement in efficiency of 3% and an excellent efficiency over the full input and output voltage range at nominal power as effect of the soft-switching. Furthermore, the efficiency for part load conditions (better than 93% at 10% nominal power) is a great advantage for automotive applications and could even be improved with a multi-phase converter concept and by changing the number of operating phases in dependency on the required output power.

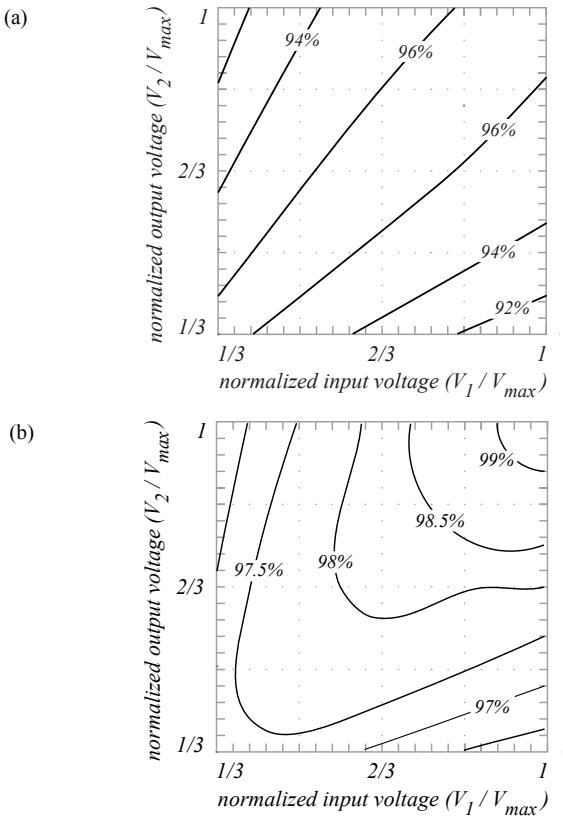

Fig. 7: Calculated semiconductor efficiency for cascaded buck+boost converter in hard-switched operation (a) and operated with the novel low-loss modulation strategy (b).

B. *Expected Power Density*

A multi-phase converter concept is a means to minimize the overall converter volume. To optimize power density, the individual converter components such as inductor, filter or number of semiconductors are investigated in terms of phase count and switching frequency.

The worst case inductor peak current I_{max} (cf. I_1 in Fig. 2 (a) for boost operation) is found at a voltage transfer ratio of $V_2 / V_1 = 2$ and for the rated peak power P_{max}. With the assumption that the energy $½ \cdot L \cdot I_0^2$ is much smaller than the energy $P_{max} \cdot T_p$ transferred within a switching period, the negative offset current $-I_0$ could be neglected and I_{max} is approximated to:

$$I_{\max} \approx \cdot \sqrt{\frac{P_{\max}}{f_s \cdot L}} \qquad (10)$$

The volume of the inductor in a first step is assumed proportional to the stored energy

$$E_L = \frac{1}{2} \cdot L I_{\max}^2 = \frac{P_{\max}}{f_s}, \qquad (11)$$

which is calculated from (10). That is why the volume of L is constant for any number of phases N at a certain switching frequency f_s and decreases with increasing f_s.

On both sides of the converter the filter structure shown in Fig. 8 is used. For the filter design, the phases are modeled as current sources that connect to a Π-filter with a damped common capacitor C_0 and the load R_L. A split filter design is necessary because of the requirement of a low-impedance connection of the phase output capacitors $C_{2,i}$ to the half-bridge. When N is increased, the ripple current calculated from the superposition of the N current sources decreases. In this case and in the case of a higher f_s, smaller reactive filter component sizes are needed and therefore a lower volume is achieved.

Furthermore, the volume occupied by the MOSFET switches including a liquid cooler is calculated with an iterative optimization algorithm. Starting with one MOSFET for each of the switches S_1 to S_4, the number of paralleled MOSFETs for the worst performing switch is incremented consecutively until the calculated efficiency is sufficient. It turns out and can also be seen from the modes shown in Fig. 3 that the RMS currents are higher for the switches S_1 and S_3. Thus, a ratio for the switch counts of approximately $S_1 / S_2 \approx S_3 / S_4 \approx 4 / 3$ is determined.

The results of the phase count optimization are shown in Figs. 9 and 10 for a typical peak power rating of P_{max}=70kW and V_{max}=450V. The volume is calculated for IXFB82N60P MOSFETs in a TO-264 package, film capacitors and the inductor L built from planar EILP ferrite cores.

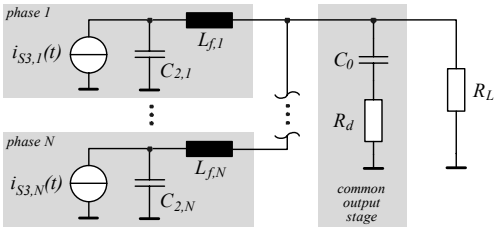

Fig. 8: Phase interconnection and input/output filter structure shown for converter side 2.

The volume share of the converter sections is shown in Fig. 9 for f_s = 100 kHz. The total converter volume decreases with higher f_s whereas a minimum occurs at a phase count $4 \le N \le 6$ depending on f_s (Fig. 10). A value of $N = 6$ is chosen for the reason of the greater flexibility for partial load operation. In this case, for a liquid-cooled converter with ideally packing of the converter sections and a volume ratio of V_{cooler}/V_{semi} = 1.4 for the semiconductors, including mounting and the cooler, the calculated power density for N = 6 is 27 kW/dm^3 for f_s = 100 kHz and 30 kW/dm^3 for f_s = 150 kHz respectively. Integration of converter and motor housing allows a saving in the cooler volume. By applying a thermal optimization strategy as presented in [12], it is possible to even reduce the inductor size in comparison to a standard design. It is estimated that with new inductor cooling techniques the power density could be increased to 40 kW/dm^3 for a switching frequency of f_s = 100 kHz and 42 kW/dm^3 for f_s = 150 kHz.

The calculated overall efficiency of a single converter module and the related loss components for the worst case operating point (boost operation 225V→450V) are listed in Tab. 1. The high efficiency more than compensates for the drawback of a higher filtering effort caused by the increased inductor RMS and peak current.

TABLE 1
Worst case loss distribution and efficiency

Total Losses	171 W	
Conduction	112 W	66 %
Switching	26 W	15 %
Winding	18 W	11 %
Core	9 W	5 %
Filter	6 W	3 %
Efficiency ≈ 96%		

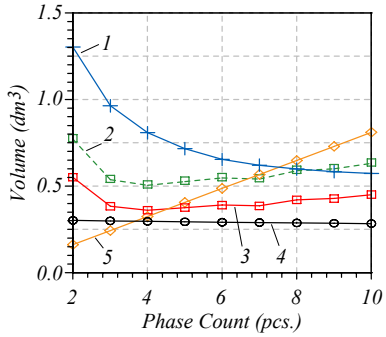

Fig. 9: Volume share of the converter sections for f_s = 100kHz, input and output filter including capacitors C_1 and C_2, (1), liquid cooler (2), semiconductors (3), inductor L (4), gate drive and control circuit (5)

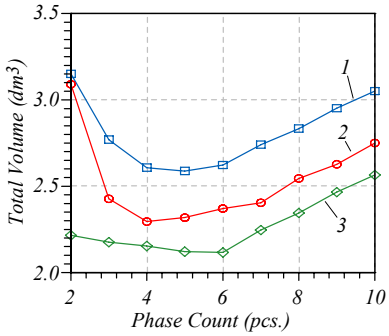

Fig. 10: Total converter volume (volume of liquid cooler not included) for switching frequencies f_s of 50 kHz (1), 100 kHz (2) and 150 kHz (3).

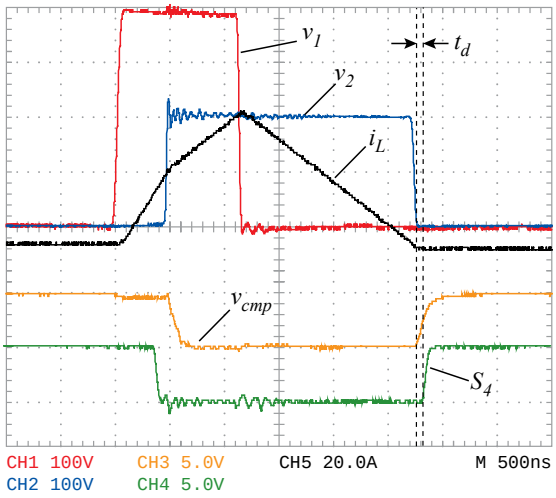

Fig 11: Ensuring ZVS by monitoring of S_4 drain-source voltage $v_2(t)$ with a comparator signal $v_{cmp}(t)$; switch S_4 control signal.

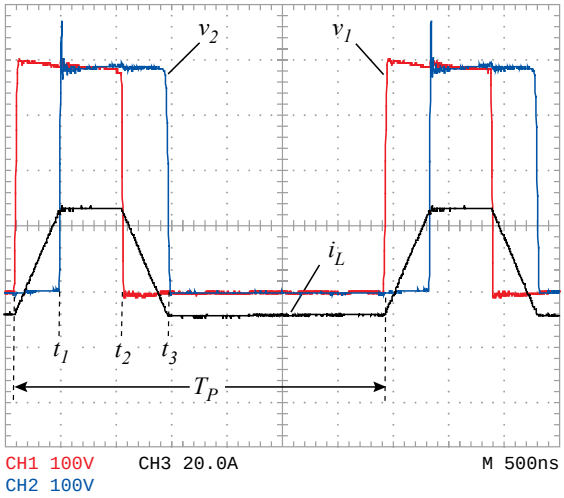

Fig. 12: Waveforms for equal input and output voltage $V_1 = V_2 = 200$V supplying a resistive load at 1.5 kW.

V. EXPERIMENTAL VERIFICATION

To demonstrate the new modulation strategy, a prototype dimensioned for P_{max} = 10 kW and V_{max} = 450 V (that requires an inductance of L = 6.5 µH) has been built. The switching times t_1 to t_3 are pre-calculated offline for different operating points and given values of L and I_0. These are interpolated in three-dimensions for V_1, V_2 and P_{tr} by the controller software and provided to a CPLD-implemented state-machine, which generates the switching patterns.

Figure 11 shows an experimentally measured inductor current $i_L(t)$ and the half-bridge voltages $v_1(t)$ and $v_2(t)$ for the case of buck operation and a voltage transfer ratio $v = V_2 / V_1 = ½$. As described in section III, comparators are used to monitor the half-bridge voltages $v_1(t)$ and $v_2(t)$ to ensure ZVS conditions. For instance, turn-on of the switch S_4 is derived from the digital comparator output signal $v_{cmp}(t)$ and a certain dead-time t_d as depicted in Fig. 11.

The case of operation with identical input and output voltages $V_1 = V_2 = 200$V is shown in Fig. 12 for a power of P_{tr} = 1.5 kW. Due to the fact of the control-optimized switching pattern, the times t_2 and t_3 are not placed towards the end of the pulse period.

VI. CONLUSION

In this paper a comparison between different converter topologies and soft-switching circuitry for a bi-directional buck+boost DC/DC converter, which could be used in an automotive application, are discussed. Major disadvantages of state-of-the-art converters are low efficiency, expensive technology or complex power circuitry.

To deal with those drawbacks, a novel constant-frequency, soft-switching modulation strategy for a cascaded buck+boost topology is presented, along with a detailed description of the operating principle.

The proposed new modulation strategy not only provides an excellent overall efficiency of at least 96% at nominal power but also features a higher efficiency for partial load operation. In addition, it results in a simple power circuitry and a high power density, which is proved by analytical calculations considering a multi-phase converter design.

Furthermore, the novel modulation strategy is successfully implemented in a prototype and measurements verify the control concept.

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