A Novel Low-Loss Modulation Strategy for High-Power Bidirectional Buck + Boost Converters

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***Abstract*—A novel, low-loss, constant-frequency, zero-voltage-switching (ZVS) modulation strategy for bidirectional, cascaded, buck–boost dc–dc converters, used in hybrid electrical vehicles or fuel cell vehicles (FCVs), is presented and its benefits over state-of-the-art converters and soft-switching solutions are discussed in a comparative evaluation. To obtain ZVS with the proposed modulation strategy, the buck + boost inductance is selected and the switches are gated in a way that the inductor current has a negative offset current at the beginning and the end of each pulse period. This allows the MOSFET switches to turn on when the antiparallel body diode is conducting. As the novel modulation strategy is a software-only solution, there are no additional expenses for the active or passive components compared to conventional modulation implementations. Furthermore, an analytical and simulation investigation predicts an excellent efficiency over the complete operating range and a higher power density for a nonisolated multiphase converter equipped with the low-loss modulation. Experimental measurements performed with 12 kW, 17.4 kW/L prototypes in stand-alone and multiphase configuration verify the low-loss operation over a wide output power range and a maximum efficiency of 98.3% is achieved.**

***Index Terms*—DC–DC power conversion, fuel cells, power conversion.**

I. Introduction

HYBRID electrical vehicles (HEVs) or fuel cell vehicles (FCVs) have improved fuel economy and reduced emissions compared to conventional drive trains with a single combustion engine [1]. Both HEVs and FCVs require energy storage elements such as batteries or ultracapacitors that provide power to the electric drive system during acceleration and are used for regenerative braking. Nickel metal hydride or lithium ion HV batteries that are used in HEV or FCV today, have a rated voltage in the range of 250 V and an operating voltage of 150–270 V [2], depending on the state of charge. The energy storage elements and the HV inverter dc link are connected by bidirectional dc–dc converters [3]. The dc-link voltage is typically higher than the battery or capacitor voltage. However, depending on the design of the propulsion system and the individual components like the number of cells and characteristics of a HV battery, the battery voltage range may overlap with the nominal HVdc-link voltage range. A nominal dc-link voltage in the range of 400 V is considered to be a tradeoff between the converter current load and costs for drive trains up to 100 kW [3]. Additionally, in FCVs with the FC directly connected to the dc link, also the dc-link voltage is variable due to the load characteristics of the FC [2]. In these cases, the dc–dc converter has to be able to function in both the buck and boost operating modes. A maximum voltage of 450 V at the battery terminals and the dc-link terminal of the converter and a maximum voltage transfer ratio of 3 is required to cover the field of application. In contrast to converters that interconnect the HVdc link and the 14 V low-voltage bus (e.g., [4]), isolation for safety reasons is not required when a HV battery is interfaced.

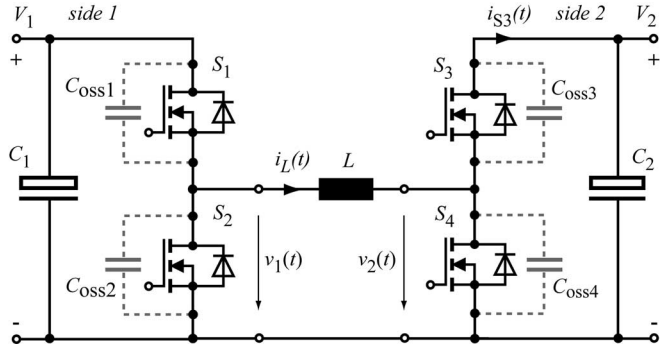

Fig. 1. Cascaded buck + boost converter for bidirectional power flow, shown with parasitic MOSFET output capacitances $C_{\mathrm{oss},i}$.

Furthermore, a converter for this application has to meet the prevalent automotive requirements, such as being a low-cost design, and minimizing the component size and count. This can be achieved by increased switching frequency and interleaved operation of multiple converter phases [5]. Fixed-frequency operation is desired due to electromagnetic interference (EMI) restrictions and a highly compact design and a low overall weight are required. An excellent efficiency of the dc–dc converter over a wide input and output power range is also a critical issue since it directly affects the overall drive train efficiency. At light load conditions the overall efficiency of a multiphase converter system is significantly improved by partial operation of the individual converters, each in the optimum efficiency range [6]. For high load conditions low individual losses in the phases are required.

One commonly used converter topology for this application is the hard-switched, cascaded, buck + boost converter [8], [9] shown in Fig. 1. When operated in continuous conduction mode (CCM) and with conventional pulse width modulation (PWM) the significant switch turn-ON loss caused by the reverse recovery of the antiparallel diode of the complementary switch in the half bridge typically results in a low maximum overall efficiency of approximately 92% [9]. Furthermore, for large voltage transfer ratios, e.g., 200–400 V, the efficiency drops significantly (Section III).

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In the literature, several ways to improve the loss behavior can be found. First, the internal switch antiparallel diodes (body diodes) may be substituted by silicon carbide diodes to avoid switching losses caused by reverse recovery. However, SiC diodes are still expensive and a hard-switched converter is often not a preferred solution because of increased EMI emissions caused by high rate of voltage change ($\mathrm{d}V/\mathrm{d}t$). Therefore, converters are proposed so that the transistors are operated with

1) zero-current switching (ZCS);
2) zero-voltage switching (ZVS);
3) low switching losses.

When lowering switching losses by these soft-switching techniques, the rate of voltage change is reduced at the same time and lower EMI emissions are also expected. On the other hand, the switching frequency f_s may be increased without severely impacting the switching losses, therefore resulting in a smaller volume of the passive components.

Secondly, with multiphase converter systems, greater efficiency and power density could be achieved [6], [7], independent of the converter topology. Each individual converter of the multiphase system shows an efficiency that typically drops at low output power due to the switching losses and the constant losses in the auxiliary circuitry. The efficiency is raised at low output power since not all of the N phases are operated, and therefore, the remaining phases now operate at their optimum efficiency point. Furthermore, when a phase shift of the phase currents is introduced, a multiple of the switching frequency f_s is effective at the output of the converter system, and thus the filter volume is reduced for a given ripple target.

A. Auxiliary Circuitry

A variety of soft-switching solutions, including circuits for PWM inverters, that are also applicable to the half bridges used in the cascaded buck + boost converter have been presented in the literature [10]–[16]. These are based on the following fundamental ZVS or ZCS concepts:

1) synchronous resonant dc link (SRDCL) [10], [11];
2) auxiliary resonant commutated pole (ARCP) [12], [13];
3) zero-current transition (ZCT) [14], [15];
4) snubber-assisted zero voltage and ZCT (SAZZ) [16].

In these concepts, the basic operating principle is to conduct the main inductor current in an additional resonant circuit such that the main switch is operated with ZVS and/or ZCS, where the resonant process is initiated by auxiliary switches.

The SRDCL [10] suffers from additional components in the main current path, high peak currents in the resonant circuit, and a resonant overshoot of the dc-link voltage of approximately 1.5 times the dc-link voltage. The modified resonant SRDCL proposed [11] and the ARCP [12], [13], ZCT [14], [15], and SAZZ [16] do not have the drawback of a resonant overshoot, but the auxiliary switch peak currents are greater than the main inductor current.

All of the mentioned solutions require additional active and passive components as well as gate drive circuitry. For instance, four auxiliary switches are employed in the case of ARCP, ZCT, or SAZZ plus the resonant capacitors and inductors (and four additional diodes in the case of SAZZ), when applied to the cascaded buck + boost converter. Another drawback is the limited PWM duty cycle range due to the additional time required by the resonant transition.

B. Resonant Converters

Besides soft-switching extensions to well-known hard-switched converters, there are a number of independent resonant, soft-switching, bidirectional buck–boost converter concepts like the constant-frequency ZVS quasi-square-wave (CF-ZVS-QSC) converter [17], single ended primary inductor converter (SEPIC) [8], [18] or the zero-voltage zero-current switching (ZVZCS) converter presented in [18].

The main drawbacks of these converters are doubled switch blocking voltage stress and diode recovery losses in case of the SEPIC [18], a larger number of passive components as well as a larger inductance value for the main inductor in the SEPIC and ZVZCS topology [17]. Furthermore, SEPIC and ZVZCS use a capacitive energy transfer that performs badly in high-power applications. Other drawbacks of resonant converters are variable switching frequency, which complicates EMI filter design, or limitations in operating range for soft switching.

II. Proposed Low-Loss Modulation Strategy

An alternative approach to achieve ZVS of the cascaded buck + boost converter (Fig. 1) is to implement a novel constant-frequency ZVS modulation strategy. This is a software-only solution that does not need any additional active or passive components, and therefore offers an increased efficiency while maintaining a low component count and simplicity of the power electronics circuit.

A. Operating Principle

In conventional PWM for the cascaded buck + boost converter, only one of the two half bridges is switched and static control signals are applied to the switches of the other bridge leg [9]. In contrast, with the proposed new modulation method, each of the four switches S_1 to S_4 is turned on and off exactly once per pulse period $T_p = 1/f_s$ to shape the inductor current i_L for minimal switching losses. The characteristic inductor current waveform (Fig. 2) first ensures that turn-ON of the four switches is accomplished under ZVS and ZCS for each switching instance, since the antiparallel body diode of the switch is conducting. A negative inductor offset current $-I_0$ is needed to fulfill this condition at the start t_0 of the pulse period. Additionally, the diode of the complementary switch in the half bridge is blocking, thus no diode reverse recovery losses are produced at turn-ON of a switch and turn-ON losses are negligible. Second, as an effect of the parasitic output capacitances C_{oss}, the turn-OFF losses of MOSFET switches are typically reasonable low. This is because the output capacitance delays the voltage raise at the switch and allows the switch to turn off under ZVS conditions before the voltage rises significantly above zero. For minimal turn-OFF losses short turn-OFF times are essential. These are achieved by a minimum resistance in

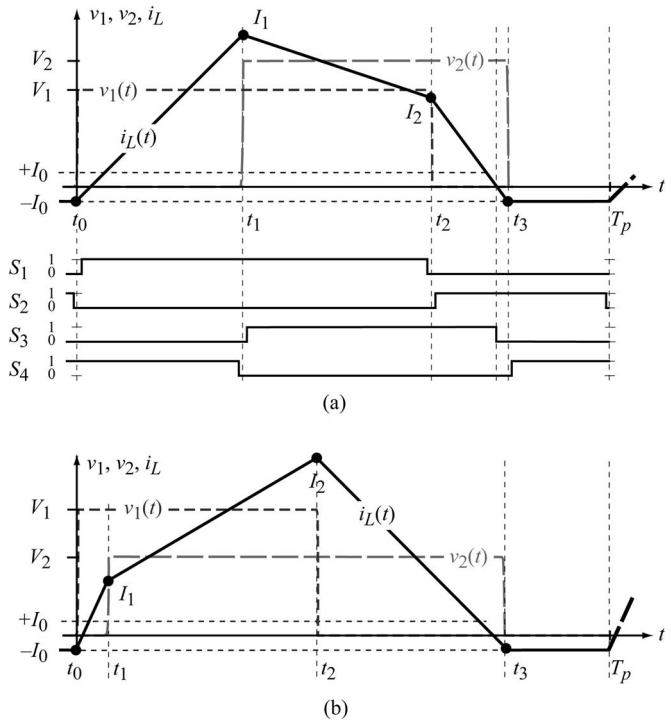

Fig. 2. (a) Basic timing diagram for switch S_1 to S_4 control signals and inductor current i_L for boost operation ($V_2 > V_1$). (b) Basic timing diagram for buck operation ($V_2 < V_1$).

the turn-OFF path of the gate driver. During the commutation interval between turn-OFF of a first switch and turn-ON of the complementary switch in the half bridge, the inductor current i_L charges the output capacitance of the first switch and discharges the output capacitance of the complementary switch, whereas energy is transferred between the output capacitances of both switches and the buck + boost inductor L. A detailed description of the modulation strategy is given in the following section.

The pulse period T_p can be divided into four modes according to the four switching states of S_1 to S_4, as shown in Figs. 2 and 3. At the beginning of the time period $t_0 \leq t < t_1$ the switch S_2 and S_4/D_4 are conducting, and therefore S_2 is turned off under ZVS due to the parasitic output capacitances of the MOSFET switches. During the commutation interval, the negative inductor current $i_L(t)$ charges the parasitic drain–source capacitance $C_{\rm oss2}$ of S_2 and discharges $C_{\rm oss1}$, respectively, energy is transferred from the inductor L to the capacitances [Fig. 3(a)]. The body diode of S_1 takes over $i_L(t)$ and S_1 can now be switched on under ZVS/ZCS. After turn-ON of S_1, the MOSFET channel of S_1 conducts the inductor current since the voltage drop across the on resistance R_{ds1} is lower than the forward voltage of the body diode (reverse conduction). The resulting current path in the power stage during the time period $t_0 < t < t_1$ is shown in Fig. 3(b). Due to the applied inductor voltage $v_L(t) = V_1$ the inductor current rises in this time period.

At $t = t_1$, S_4 is conducting, therefore the output capacitance $C_{\rm oss4}$ is discharged and S_4 is turned off under ZVS. The inductor current $i_L(t)$ charges $C_{\rm oss4}$ and discharges $C_{\rm oss3}$, respectively, energy is transferred from the inductor L to the output capacitances. Again, at the end of the commutation interval, the antiparallel body diode of S_3 takes over the current and S_3 can be turned on under ZVS/ZCS. The applied inductor voltage $v_L(t) = V_1$–V_2 either causes i_L to rise (buck operation) or fall (boost operation) during the time period $t_1 < t < t_2$ depending on the relative magnitudes of V_1 and V_2. The resulting current path in the power stage during the time period $t_1 \leq t < t_2$ is shown in Fig. 3(c).

The turn-OFF ZVS and turn-ON ZVS/ZCS principle also applies to the remaining two switching actions at $t = t_2$ (S_1 is turned off and S_2 is turned on) and at $t = t_3$ (S_3 is turned off and S_4 is turned on). However, since the direction of the current i_L is reversed at $t = t_2$ and $t = t_3$ [cf. Fig. 3(e)], during the associated commutation intervals energy is transferred from the output capacitances to the buck + boost inductor L. Therefore, the energy required for the switching actions at $t = t_0$ and $t = t_1$ is recovered during the pulse period T_p and very low overall switching losses are expected.

In the last time period $t_3 < t < T_p$, the switches S_2 and S_4 are turned on and the switches S_1 and S_3 are turned off, so that the current $i_L(t)$ circulates in the power circuit, as shown in Fig. 3(f). This is to keep the switching frequency constant and to provide the negative offset current needed for ZVS/ZCS at the beginning of the subsequent pulse period.

B. Calculation of the Switching Times

Starting with the basic inductor current waveforms as depicted in Fig. 2 for buck and boost operation, assuming constant voltages V_1 and V_2 and neglecting resistances of the inductor and the switches S_i, the differential equation

$$v_L(t) = v_1(t) - v_2(t) = L \cdot \frac{d}{dt} i_L(t) \tag{1}$$

is solved in the four time intervals and yields

$$t_1 - t_0 = L \cdot \frac{I_0 + I_1}{V_1} \tag{2}$$

$$t_2 - t_1 = L \cdot \frac{I_2 - I_1}{V_1 - V_2} \tag{3}$$

$$t_3 - t_2 = L \cdot \frac{I_0 + I_2}{V_2}. \tag{4}$$

The average power $P_{\rm tr}$ transferred from converter *side 1* to *side 2* is calculated from

$$P_{\rm tr} = \frac{1}{T_p} \cdot \int_{t_0}^{T_p} v_1(t) \cdot i_1(t) dt. \tag{5}$$

The integral (5) can be solved for the current waveform depicted in Fig. 2 and $t_0 = 0$

$$P_{\rm tr} = \frac{V_1}{T_p} \cdot \int_0^{t_2} i_L(t) dt = \frac{V_1}{2 \cdot T_p} ((I_1 + I_2) \cdot t_2 - (I_0 + I_2) \cdot t_1). \tag{6}$$

The set of equations (2)–(4) and (6) with unknowns t_1, t_2, I_1, and I_2 may be solved to calculate the switching times t_1, t_2 for the desired operating point $(V_1, V_2, P_{\rm tr})$ and a given time t_3.

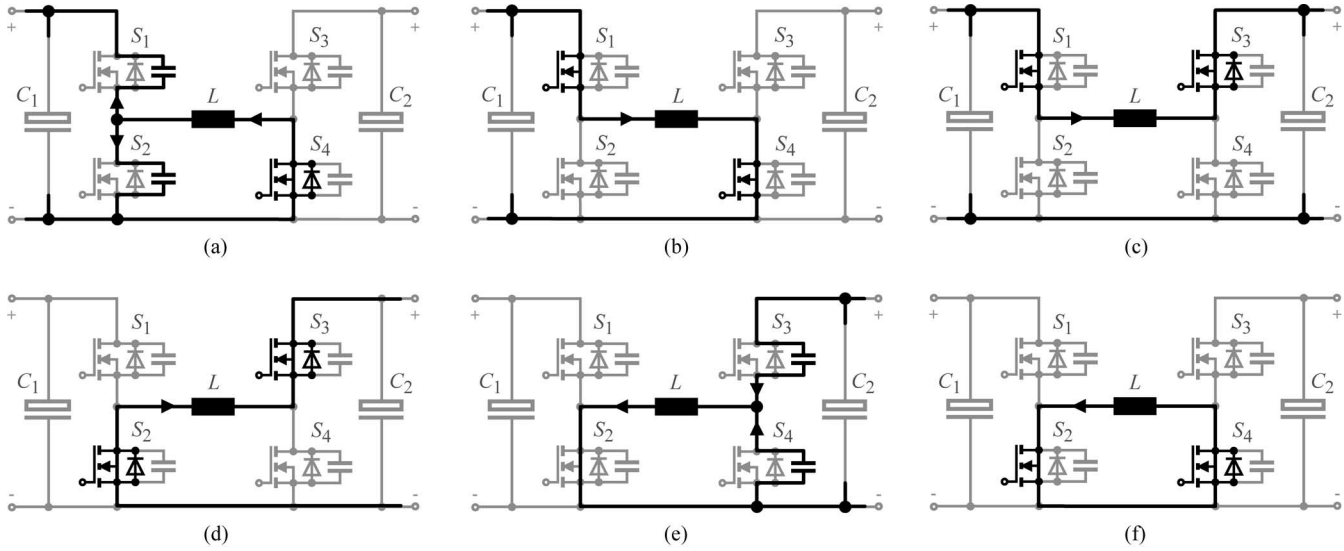

Fig. 3. Inductor current flow for time intervals (b) $t_0 < t < t_1$, (c) $t_1 < t < t_2$, (d) $t_2 < t < t_3$, and (f) $t_3 < t < T_p$, and during the resonant commutation at (a) $t = t_0$ and (e) $t = t_3$. Current direction reverses in (b) and (d), as can be seen in Fig. 2, which is not shown for the reason of simplicity.

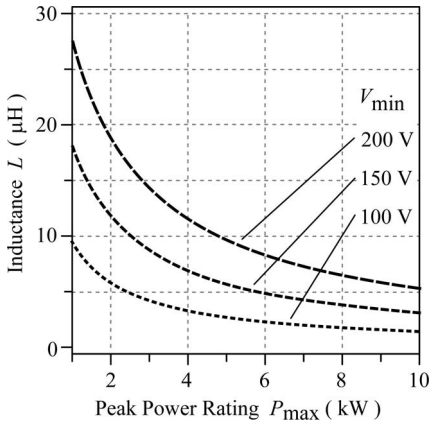

Fig. 4. Maximum inductance L, shown for $V_{1,\min} = V_{2,\min}$ $V_{\min}$, $I_0 = 10$ A, and $f_s = 100$ kHz as function of the converter peak power rating $P_{\max}$.

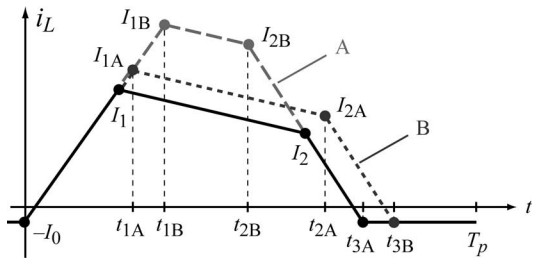

Fig. 5. Possibilities to increase transferred power $P_{\rm tr}$: keeping t_3 constant (waveform A) and shifting t_3 toward the end of the switching period T_p (waveform B).

Furthermore, as shown in the Appendix, the maximum of $P_{\rm tr}$ is calculated as

$$P_{\rm tr,max}(t_3) = \frac{V_1 V_2 \cdot (I_0^2 L^2 - 2 I_0 L \cdot (V_1 + V_2) \cdot t_3 + V_1 V_2 \cdot t_3^2)}{2 \cdot L \cdot T_p \cdot (V_1^2 + V_1 V_2 + V_2^2)}. \tag{7}$$

The inductance of the buck + boost inductor L has to be derived from (7) for a given operating voltage and power range and $t_3 = T_p$ in such a manner that $P_{\rm tr,max}$ will never be exceeded, or otherwise the constraints for soft switching will be violated. The maximum inductance L depends on the minima of V_1 and V_2 and the rated converter peak power $P_{\max} = P_{\rm tr,max}(T_p)$ as shown, exemplarily, in Fig. 4.

C. Optimized Switching Pattern

As stated before, there is the degree of freedom to choose the switching time t_3 for a given converter operating point. An example is depicted in Fig. 5. Assuming an exemplary current waveform (marked by I_0, I_1, I_2), there are two possibilities to increase $P_{\rm tr}$. First, the switching time t_3 could be kept constant and the times t_1 and t_2 adjusted (waveform B). Second, the switching time t_3 could be shifted toward the end of the switching period T_p (waveform A). This is preferred because of a lower peak and rms inductor current, and thus lower inductor losses.

Besides the consideration for a low rms current, there are reasons why a continuous variation of t_1, t_2, and t_3 (without any steps) is desired over the operating voltage and power range. First, due to the complex switching pattern, the calculation of the times is implemented by a 3-D lookup table (V_1, V_2, and $P_{\rm tr}$) and a linear interpolation. This minimizes the arithmetic effort in the DSP software, and therefore maximizes the control bandwidth. However, to achieve a low interpolation error, the partial derivatives, e.g., $\delta t_1/\delta V_1$, $\delta t_1/\delta V_2$, and $\delta t_1/\delta P_{\rm tr}$ for time t_1, must be continuous. Second, discontinuities in the partial derivatives could cause system instability. This is when minor variations of the modulator input quantities V_1, V_2, or $P_{\rm tr}$ caused by the voltage measurement or the current controller lead to wide variations in the switching times. To address these requirements, a time calculation scheme is derived for a given power $P_{\rm tr}$.

1) The minimum of t_3 is determined considering the limit of ZVS operation for the given range for V_1 and V_2 ($I_1 = +I_0$

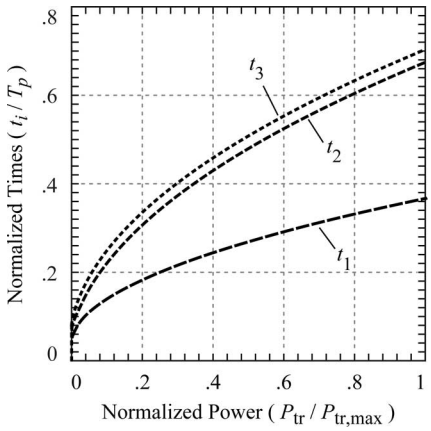

Fig. 6. Normalized output power $P/P_{\mathrm{tr,max}}$ and times t_i/T_p for $V_2 = V_{2,\mathrm{max}}$ and a voltage transfer ratio of $V_2/V_1 = 2$.

for buck operation and $I_2 = +I_0$ for boost operation) and is used as a initial value $t_{3,\mathrm{min}}$ for t_3. The initial value is normally applicable at the upper ends of the operating voltage range.

2) If the energy $E_{\mathrm{tr}} = P_{\mathrm{tr}} \cdot T_p$ could not be converted within $t_0 < t < t_{3,\mathrm{min}}$, t_3 is shifted toward the end of the pulse period at the limit of ZVS operation until the transfer of E_{tr} for any combination of V_1 and V_2 is possible (cf. Fig. 5, waveform A).
3) When $t_3 = T_p$, t_1 and t_2 are adjusted, as depicted in Fig. 5, waveform B.

The calculated, normalized values for t_1, t_2, and t_3 for a voltage transfer ratio of $V_2/V_1 = 2$ and $V_{2,\mathrm{max}} = 450$ V are shown in Fig. 6.

D. Ensuring ZVS Condition

As a first approximation, the minimum absolute value needed for I_0 depends on the resonant circuit formed by L and the MOSFET output capacitances C_{oss} of the affected half bridge as well as the converter input and output voltage levels V_1 and V_2, which excite the *LC* circuit

$$I_0 \geq \max(V_{1\mathrm{max}}, V_{2\mathrm{max}}) \cdot \sqrt{\frac{C_{\mathrm{oss}}}{L}}. \tag{8}$$

If the condition (8) is true, the energy stored in the inductor L at turn-OFF of a switch is large enough to completely transfer the charge between the both parasitic MOSFET output capacitances of the half bridge, so that the complementary switch of the half bridge can be turned on at zero voltage. The same applies to the absolute value of $i_L(t)$ at $t = t_1$ and $t = t_2$ inducing the conditions

$$I_1 \geq I_0 \qquad \text{and} \qquad I_2 \geq I_0. \tag{9}$$

It should be noted that (8) is an approximation, since C_{oss} exhibits a nonlinear, voltage-dependent characteristic and the diffusion charge Q_D stored in the body diode junction of S_3 further increases the offset current I_0.

A drift of i_L below $-I_0$ in the time period $t_3 < t < T_p$ due to component nonlinearity or inexact timing must be avoided to keep conduction losses low. An accurate high-speed zero-crossing detection could be used to exactly determine the time t_3.

Another option, which is implemented in the converter prototype, is to monitor the half bridge voltages $v_1(t)$ and $v_2(t)$ with high-speed analog comparators to detect a zero voltage level. For instance, i_L is decreasing in the time period $t_2 < t < t_3$. When i_L becomes negative, the body diode of S_4 starts conducting and $v_2(t)$ becomes zero, causing the comparator output to change. This information is then used to turn on S_4 under ZVS.

In contrast to standard ZVS modulation concepts, with the proposed novel modulation strategy ZVS is also achieved at low output power levels and even down to an output power of zero when a reactive power transfer is maintained. For instance, when the converter losses are neglected, a zero output power implies that the converter input power P_1 and output power P_2 are equal to zero

$$P_1 = \frac{1}{T_p} \cdot V_1 \int_{t_0}^{t_2} i_L(t)dt = 0 \tag{10}$$

$$P_2 = \frac{1}{T_p} \cdot V_2 \int_{t_1}^{t_3} i_L(t)dt = 0. \tag{11}$$

Detailed analytical terms of (10) and (11) are derived in the Appendix. There is a solution to calculate the switching times t_1, t_2, t_3 from (10) and (11) when either $t_1 = t_2$ or $t_2 = t_3$

$$t_1 = t_2 = \frac{2I_0L}{V_1}, \quad t_3 = \frac{2I_0L(V_1+V_2)}{V_1V_2}, \quad \text{for } t_1 = t_2$$
$$t_1 = \frac{2I_0L}{V_1}, \quad t_2 = t_3 = \frac{2V_2I_0L}{V_1(V_2-V_1)}, \quad \text{for } t_2 = t_3 \tag{12}$$

with the property that $i_L(t_1) = I_0$, and thus ZVS is achieved at the same time for each switching action. An example of the resulting triangular inductor current waveform is shown in Fig. 7 for $T_p < t < 2T_p$.

E. Direction of Power Conversion

A pulse period with a special modulation sequence must be inserted to maintain ZVS at the change of the direction of power conversion. At the beginning of the reversion sequence that is depicted in Fig. 7 for $2T_p < t < 3T_p$, the input voltage V_1 is applied to the buck + boost inductor L for a certain time $t_1 = 2I_0L/V_1$ until the current raises from $-I_0$ to $+I_0$. Then, the switches S_2 and S_4 are turned on and a positive offset current I_0 that is required for ZVS at the beginning of the subsequent pulse period circulates in the power stage.

The reverse power conversion is shown in Fig. 7 for $t > 3T_p$ whereas the control sequence for the switches S_1 to S_4 is changed in a way that the gate signals for the two half bridges are exchanged and the mode of operation has to be changed from a buck to a boost operation mode.

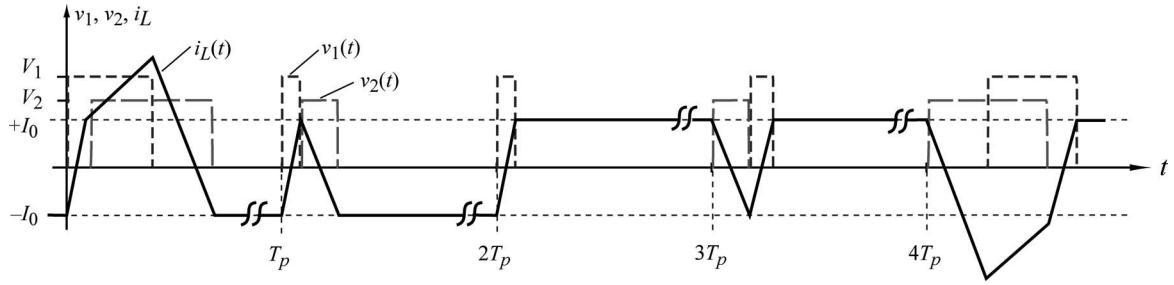

Fig. 7. Inductor current waveform and special modulation sequence ($2T_p < t < 3T_p$) for the reversal of the direction of power conversion, depicted for a voltage transfer ratio of $V_1/V_2 = 4/3$.

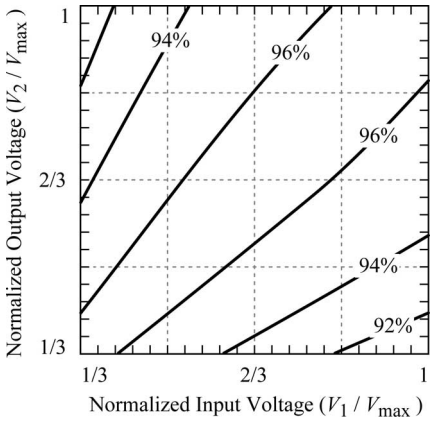

Fig. 8. Calculated semiconductor efficiency for cascaded buck + boost converter in hard-switched operation.

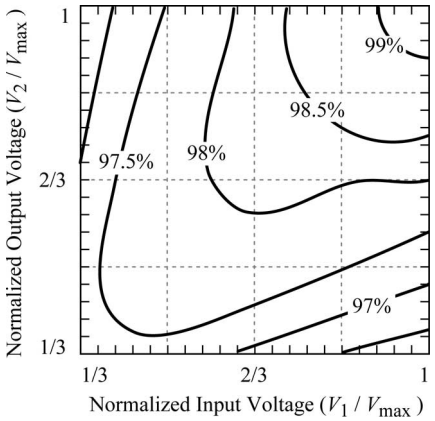

Fig. 9. Calculated semiconductor efficiency for cascaded buck + boost converter operated with the novel low-loss modulation strategy.

III. Analytical Results

A. Efficiency Comparison

For comparison of the novel modulation strategy to the hard-switched cascaded buck + boost topology operated with conventional PWM, the semiconductor conduction and switching losses are analytically calculated for both modulation methods and based on measured switching losses of two MOSFETs in a half bridge configuration and at $V_{\max} = 450$ V. Figs. 8 and 9 show an improvement in efficiency of 3% and an excellent efficiency over the full input and output voltage range at nominal power as effect of the soft switching. Furthermore, the efficiency for part load conditions (better than 93% at 10% nominal power) is a great advantage for automotive applications and could even be improved with a multiphase converter concept and by changing the number of operating phases in dependency on the required output power.

B. Calculated Power Density

A multiphase converter concept is a means to minimize the overall converter volume. To optimize power density, the individual converter components such as inductor, filter, or number of semiconductors are investigated in terms of phase count and switching frequency. The optimization is based on volume models of the passive components that are determined with the geometrical and electrical data of the capacitors and reference inductor designs.

The worst-case inductor peak current $I_{\max}$ (cf. I_1 in Fig. 2(a) for boost operation) is found at a voltage transfer ratio of $V_2/V_1 = 2$ and for the rated peak power $P_{\max}$. With the assumption that the energy $1/2LI_0^2$ is much smaller than the energy $P_{\max}T_p$ transferred within a switching period, the negative offset current $-I_0$ could be neglected and $I_{\max}$ is approximated to

$$I_{\max} \approx \sqrt{\frac{P_{\max}}{f_s L}}. \tag{13}$$

The volume of the inductor in a first step is assumed proportional to the stored energy

$$E_L = \frac{1}{2}LI_{\max}^2 = \frac{P_{\max}}{f_s} \tag{14}$$

which is calculated from (13). This is why the volume of L is constant for any number of phases N at a certain switching frequency f_s and decreases with increasing f_s.

The volume occupied by the MOSFET switches including a liquid cooler is strongly dependent on the efficiency requirement, since a parallel configuration of several discrete MOSFETs for each of the switches S_1 to S_4 is utilized in each converter phase module to reduce the conduction losses. The number of paralleled MOSFETs, i.e., the required chip area, is calculated with an iterative optimization algorithm. Starting with one MOSFET for each of the switches S_1 to S_4 of the converter phase, the number of paralleled MOSFETs for the worst-performing switch is incremented consecutively until

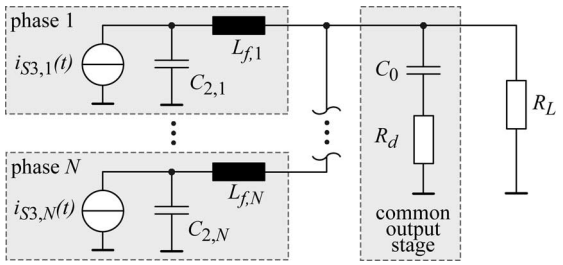

Fig. 10. Phase interconnection and input/output filter structure shown for converter side 2, switch S_3 currents $i_{S3,i}(t)$ (cf. Fig. 1).

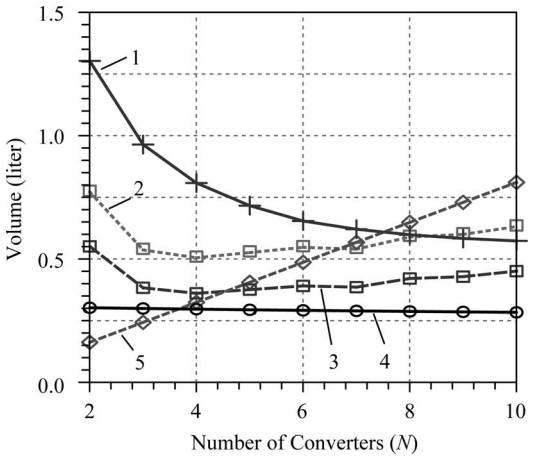

Fig. 11. Volume share of the converter sections for $f_s = 100$ kHz. (1) Input and output filter including capacitors C_1 and C_2. (2) Liquid cooler. (3) Semiconductors. (4) Inductor L. (5) Gate drive and control circuit.

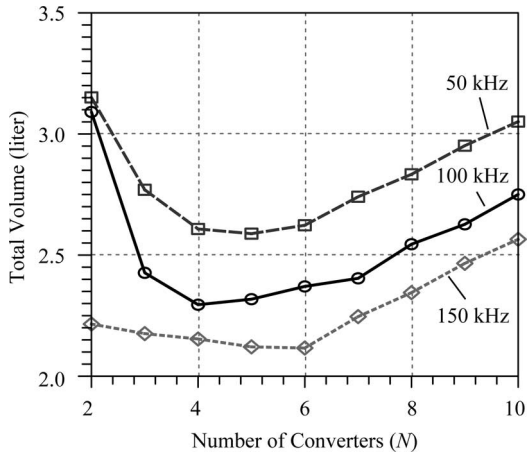

Fig. 12. Total converter volume (volume of liquid cooler not included) for switching frequencies f_s of 50, 100, and 150 kHz.

TABLE I
WORST-CASE ($V_1 = 225$ V, $V_2 = 450$ V) LOSS DISTRIBUTION AND CALCULATED CONVERTER EFFICIENCY

Total Losses	171 W	
Conduction	112 W	66 %
Switching	26 W	15 %
Winding	18 W	11 %
Core	9 W	5 %
Filter	6 W	3 %
Efficiency ≈ 96%		

the calculated semiconductor efficiency meets the minimum required value, e.g., 96%. It turns out and can also be seen from the modes shown in Fig. 3 that the rms currents are higher for the switches S_1 and S_3. Thus, a ratio for the number of switches of approximately $S_1/S_2 \approx S_3/S_4 \approx 4/3$ is determined.

Furthermore, on both sides of the converter the filter structure shown in Fig. 10 is used. For the filter design, the phases are modeled as current sources that connect to a Π-filter with a damped common capacitor C_0 and the load R_L. A split filter design is necessary because of the requirement of a low-impedance connection of the phase output capacitors $C_{2,i}$ to the half bridge. When N is increased, the ripple current calculated from the superposition of the N current sources decreases. In this case and in the case of a higher f_s, smaller reactive filter component sizes are needed, and therefore, a lower volume is achieved.

The results of the converter number (N) optimization are shown in Figs. 11 and 12 for a typical peak power rating of $P_{\max} = 70$ kW and $V_{\max} = 450$ V. The volume is calculated for IXFB82N60P MOSFETs in a TO-264 package, film capacitors and the inductor L built from planar EILP ferrite cores.

The volume share of the converter sections is shown in Fig. 11 for $f_s = 100$ kHz. The total converter volume decreases with higher f_s, whereas a minimum occurs at a phase count $4 \leq N \leq 6$ depending on f_s (Fig. 12).

A value of $N = 6$ is chosen for the reason of the greater flexibility for partial phase operation. In this case, for a liquid-cooled converter with ideally packing of the converter sections and a volume ratio of $V_{\text{cooler}}/V_{\text{semi}} = 1.4$ for the semiconductors, including mounting and the cooler, the calculated power density for $N = 6$ is 27 kW/L for $f_s = 100$ kHz and 30 kW/L for $f_s = 150$ kHz, respectively. Integrating the converter into the motor housing would allow a saving in the cooling system volume. By applying a thermal optimization strategy as presented in [19], it is possible to even reduce the inductor size in comparison to a standard design. It is estimated that with new inductor cooling techniques the power density could be increased to 40 kW/L for a switching frequency of $f_s = 100$ kHz and 42 kW/L for $f_s = 150$ kHz.

A switching frequency of 100 kHz is selected as a compromise between power density and converter efficiency. The calculated overall efficiency of a single converter module and the related loss components for the worst-case operating point (boost operation 225 V → 450 V) are listed in Table I. The high efficiency more than compensates for the drawback of a higher filtering effort caused by the increased inductor rms and peak current.

However, it must be noted that the semiconductor chip area required for the switches S_1 to S_4 is increased in comparison to a hard-switched converter or a converter topology equipped with an auxiliary circuitry to achieve soft switching. A more detailed comparison of the different topologies including cost models of each component would be required to decide on the cost-optimal topology.

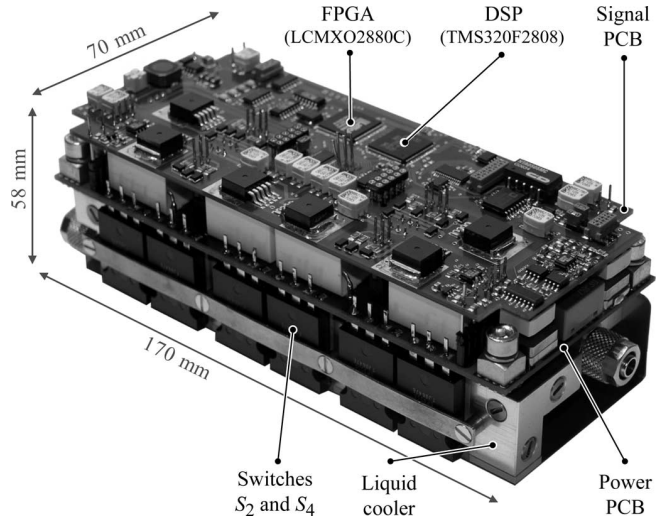

Fig. 13. Liquid-cooled 12 kW bidirectional buck + boost converter module.

IV. Experimental Verification

To demonstrate the new modulation strategy, a prototype dimensioned for $P_{\max} = 12$ kW and $V_{\max} = 450$ V has been built (Fig. 13) that has a power density of 17.4 kW/L. An inductance of $L = 5.7$ μH is calculated from (7) and built from three air-gapped EILP43 ferrite cores. The input and output capacitors C_1 and C_2 of the phase module are 12 μF film capacitors. A converter redesign using ceramic capacitors instead and an optimized construction is currently realized and the power density is expected to be above 27 kW/L.

To avoid a time-consuming calculation of the switching times t_1 to t_3 by the DSP software, and thus to improve the control bandwidth, the times are precalculated offline and tabulated for different operating points and given values of L and I_0. These are interpolated in three dimensions for V_1, V_2, and $P_{\rm tr}$ by the controller software and provided to a field-programmable gate array (FPGA)-implemented state-machine, which generates the switching pattern. An integral controller implemented in the FPGA that is fed with analog comparator signals derived from $v_1(t)$ and $v_2(t)$ controls I_0 to ensure ZVS conditions at the input-side half bridge in the buck operation mode (Section II-D). The detailed modeling of the plant and the controller is subject of current research and will be presented in a future publication.

Fig. 14 shows an experimentally measured inductor current $i_L(t)(-I_0 = -19$ A, $\hat{i}_L = 122$ A) and the half bridge voltages $v_1(t)$ and $v_2(t)$ for the case of buck operation with $V_1 = 400$ V, a voltage transfer ratio $v = V_2/V_1 = 1/2$ and an output power of $P_{\rm tr} = 7.4$ kW. The case of operation with identical input and output voltages $V_1 = V_2 = 300$ V is shown in Fig. 15 for a power of $P_{\rm tr} = 8.2$ kW. Due to the control-optimized switching pattern, the times t_2 and t_3 are not placed toward the end of the pulse period. Exemplary measurements that verify the ZVS operation of the two complementary switches S_1 and S_2 at the converter input are shown in Figs. 16 and 17. The gate signals are applied to the switches at a zero drain–source voltage and turn-OFF losses are reduced by increasing the switching speed with a lower gate resistance.

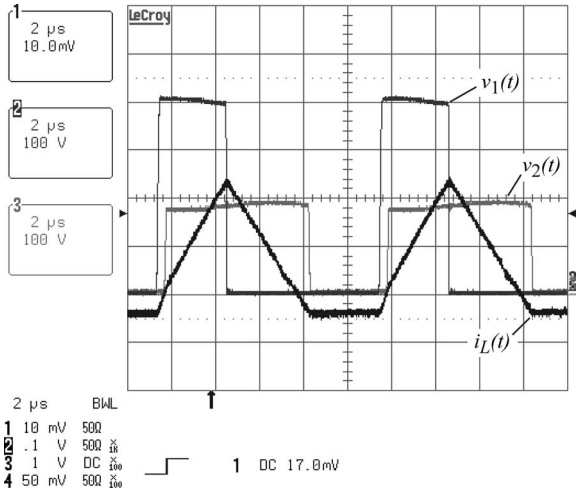

Fig. 14. Waveforms for $V_1 = 400$ V, $V_2 = 200$ V supplying a resistive load at 7.4 kW. ZVS at the converter input side (switches S_1, S_3) is ensured by an integral control of I_0 implemented in the CPLD (i_L: 50 A/div).

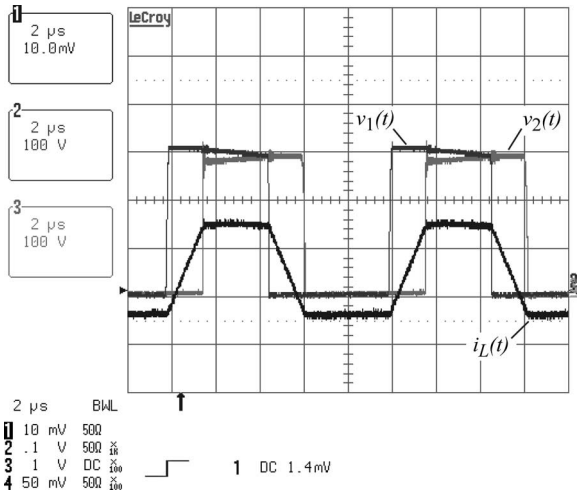

Fig. 15. Waveforms for equal input and output voltage $V_1 = V_2 = 300$ V supplying a resistive load at 8.2 kW (i_L: 50 A/div).

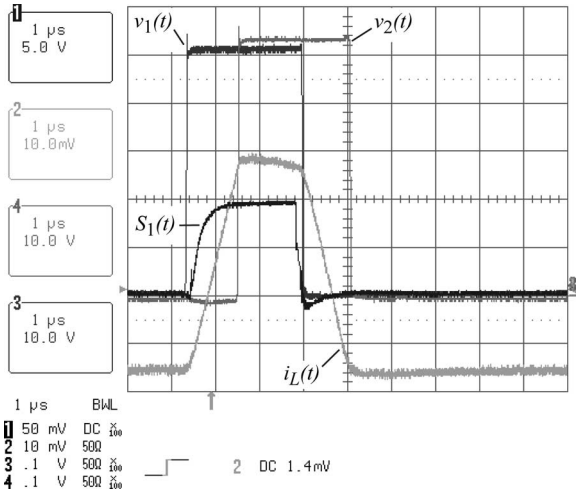

Fig. 16. ZVS of switch S_1: the gate voltage (channel 1) is applied when the drain–source voltage across S_1 is zero and a high switching speed at turn-OFF reduces losses.

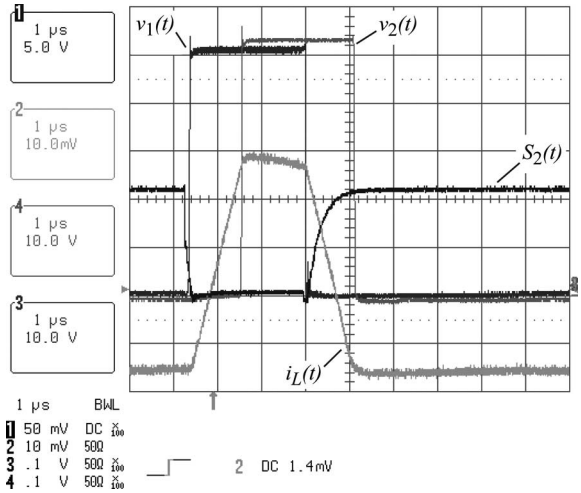

Fig. 17. ZVS of switch S_2: the gate voltage (channel 1) is applied when the drain–source voltage across S_2 is zero and a high switching speed at turn-OFF reduces losses.

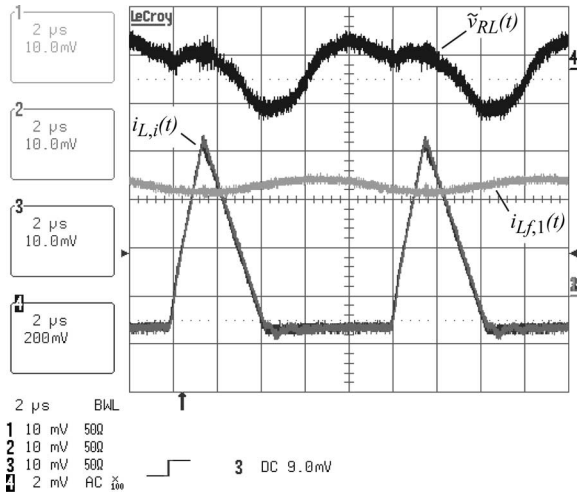

Fig. 18. Output voltage ripple for two operated phases ($V_1 = 400$ V, $V_2 = 150$ V, $P_{\rm tr} = 3.4$ kW) and a phase shift angle of 0° (channel 1: filter inductor L_f current 5 A/div, channel 2/3: inductor currents $i_{L,i}$, 20 A/div, and channel 4: output voltage ripple).

The results of the multiphase operation of two converter phases with identical timing t_1 to t_3 and the reduction in the converter output voltage ripple, associated with an ideal phase shift angle of 180°, are shown in Figs. 18 and 19. As with the non-CCM modulation, the sensitivity of the current share to tolerances in the duty cycles and the inductance L is relatively small [5], there is no individual closed-loop current control of the phases. However, a control concept that further minimizes the output ripple and the frequency content of the phase switching frequency f_s in the output spectrum is currently investigated.

The overall efficiency for a single converter phase module is measured with a Norma D 6133 S power analyzer for different voltage transfer ratios in dependence on the output power and is shown in Fig. 20. The converter shows an excellent efficiency over a wide output power range. For equal input and output voltages of 300 V, a maximum efficiency of 98.3% is achieved.

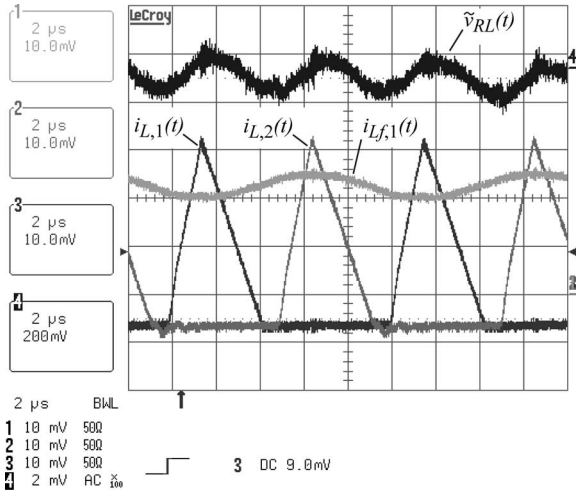

Fig. 19. Output voltage ripple for two operated phases ($V_1 = 400$ V, $V_2 = 150$ V, $P_{\rm tr} = 3.4$ kW) and a phase shift angle of 180° (channel 1: filter inductor L_f current 5 A/div, channel 2/3: inductor currents $i_{L,i}$, 20 A/div, channel 4: output voltage ripple).

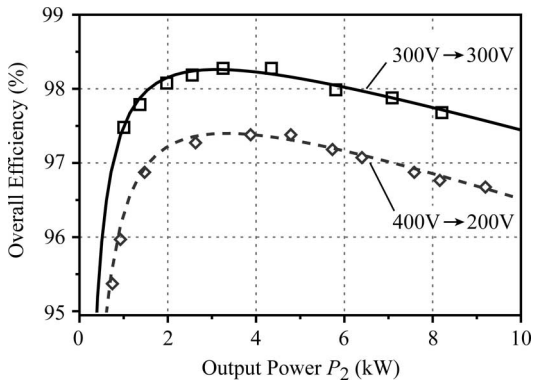

Fig. 20. Measured overall efficiency for the single converter phase module shown in Fig. 12.

V. Conclusion

In this paper, different converter topologies and soft-switching circuitry for a bidirectional buck + boost dc/dc converter, which could be used in a HEV or FCV, have been discussed. Major disadvantages of state-of-the-art converters are low efficiency, expensive technology, or complex power circuitry.

To deal with those drawbacks, a novel constant-frequency, soft-switching modulation strategy for a bidirectional buck + boost converter has been presented, along with a detailed description of the operating principle. The proposed modulation strategy provides a negative offset current at the beginning of each pulse period that, in conjunction with just the parasitic MOSFET output capacitances but no additional components, allows ZVS with the full voltage and load range.

The proposed new modulation strategy not only provides an excellent overall efficiency at nominal power but also features a higher efficiency for partial load operation. In addition, it results in a simple power circuitry and a high power density, which is proved by analytical calculations considering a multiphase converter design.

Furthermore, the novel modulation strategy is successfully implemented in a 12 kW prototype that has a power density of 17.4 kW/L, and measurements verify the control concept for the buck, boost, and multiphase operation. A measured efficiency of at least 96% at rated power and a maximum efficiency of 98.3% at equal input and output voltages of 300 V make the concept very promising for automotive applications.

APPENDIX

MAXIMUM TRANSFERABLE POWER

Equations (2)–(4) can be used to calculate the time function of inductor current

$$i_L(t) = \begin{cases} -I_0 + \dfrac{V_1}{L}t, & \text{for } 0 \le t < t_1 \\ -I_0 + \dfrac{V_2}{L}t_1 + \dfrac{V_1 - V_2}{L}t, & \text{for } t_1 \le t < t_2 \\ -I_0 + \dfrac{V_2}{L}t_1 + \dfrac{V_1}{L}t_2 - \dfrac{V_2}{L}t, & \text{for } t_2 \le t < t_3 \\ -I_0, & \text{for } t_3 \le t < T_p. \end{cases} \tag{A1}$$

With (A1), the converter input and output power is calculated by integration of the inductor current

$$\begin{aligned} P_1 &= \frac{1}{T_p}\cdot V_1 \int_{t_0}^{t_2} i_L(t)dt \\ &= \frac{V_1}{2T_pL}\left((V_1 - V_2)t_2^2 - V_2 t_1^2 + 2V_2 t_1 t_2\right) - \frac{V_1 I_0}{T_p}t_2 \end{aligned} \tag{A2}$$

$$\begin{aligned} P_2 &= \frac{1}{T_p}\cdot V_2 \int_{t_1}^{t_3} i_L(t)dt = -\frac{V_2 I_0}{T_p}(t_3 - t_1) + \frac{V_2}{2T_pL} \\ &\quad \times \left(-V_2 t_3^2 - V_1 t_2^2 - (V_1 + V_2)t_1^2 + V_2 t_1 t_3 + 2V_1 t_2 t_3\right). \end{aligned} \tag{A3}$$

As can be seen from (A3), the output power depends on the switching times t_1, t_2, and t_3. There are constraints that limit the degrees of freedom in selecting these switching times. First, when the converter losses are neglected, input and output power must match and correspond to a transferred power P_{tr}

$$P_1 = P_2 = P_{\mathrm{tr}}. \tag{A4}$$

Second, due to the desired principal current waveform (cf. Fig. 2), at $t = t_3$ the inductor current must be equal to the negative offset current $-I_0$

$$i_L(t_3) = -I_0 + \frac{V_2}{L}t_1 + \frac{V_1}{L}t_2 - \frac{V_2}{L}t_3 \stackrel{!}{=} -I_0. \tag{A5}$$

The following fundamental correlation between t_1 and t_2 is calculated from (A5):

$$t_2 = \frac{V_2}{V_1}(t_3 - t_1). \tag{A6}$$

Since t_3 must not exceed T_p, there is an upper limit $P_{\mathrm{tr,max}}$ of the converter output power for a given converter design (T_p, L) and a given operating point (V_1, V_2). To determine $P_{\mathrm{tr,max}}$, (A3) is evaluated at (A6) and differentiated with respect to t_1. The times $t_{1,\max}$ and $t_{2,\max}$ for maximum transferred power ($P_{\mathrm{tr}}(t_1)$ is a quadratic function in t_1, $(d/dt_1)P_{\mathrm{tr}}(t_1) = 0$) are calculated to

$$\begin{aligned} t_{1,\max} &= \frac{V_2^2 t_3 + V_1 I_0 L}{V_1^2 + V_1 V_2 + V_2^2} \\ t_{2,\max} &= \frac{(V_2^2 + V_1 V_2)t_3 - V_2 I_0 L}{V_1^2 + V_1 V_2 + V_2^2}. \end{aligned} \tag{A7}$$

Equation (A3) is evaluated at $t_1 = t_{1,\max}$ and $t_2 = t_{2,\max}$ and yields (7).

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Dr. Kolar is a Member of the Institute of Electrical Engineers of Japan (IEEJ) and Technical Program Committees of numerous international conferences (e.g., the Director of the Power Quality branch of the International Conference on Power Conversion and Intelligent Motion). From 1997 to 2000, he served as an Associate Editor of the IEEE Transactions on Industrial Electronics, and since 2001, as an Associate Editor of the IEEE Transactions on Power Electronics.