Output Ripple Reduction of an Automotive Multi-Phase Bi-Directional DC-DC Converter

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***Abstract*—Bi-directional dc-dc converters for automotive applications typically are limited to generate only a small voltage ripple, especially when a ultra-capacitor with a limited ripple current capability is interfaced by the converter. Thus, to minimize the ripple quantities and the converter volume at the same time, interleaved multi-phase dc-dc converters are utilized. However, tolerances of the buck+boost inductors of the interleaved phases generate sub-harmonics in the ripple spectrum that are counterproductive to the advantage of ripple reduction. A method to cancel the fundamental frequency of the voltage ripple is proposed that is applicable to a converter consisting of three or more phases. It is shown that even for a low phase count the overall ripple amplitude is greatly reduced, only by adjustment of the phase shift angles. Experimental results carried out with a three-phase interleaved bi-directional dc-dc converter proof the concept functionality.**

***Index Terms*—DC-DC Converter, Multi-Phase, Interleaving, Voltage Ripple**

I. Introduction

Both Hybrid Electrical Vehicles (HEVs) and Fuel Cell Vehicles (FCVs) require energy storage elements such as batteries or ultra-capacitors that are connected to the high voltage (HV) inverter dc-link by bi-directional dc-dc converters and are utilized to provide power to the electric drive system during acceleration and for regenerative braking. The dc-link voltage is typically higher than the battery or ultra-capacitor voltage, but could, depending on the design of the propulsion system, also overlap with the dc-link voltage. A nominal dc-link voltage in the range of 400 V is considered to be a trade-off between the converter current load and costs for drive trains up to 100 kW [1]. On the other hand, Nickel Metal Hydride or Lithium Ion HV batteries that are used in HEV or FCV today have an operating voltage in the range of 150 V to 270 V, depending on the number of cells and the state of charge. An applicable highly-efficient bi-directional buck+boost converter topology is shown in Fig. 1. This covers a voltage range of 150 V to 450 V at both sides of the converter and operates at a constant switching frequency of $f_{\mathrm{sw}} = 1/T_{\mathrm{p}}$ = 100 kHz and a Zero Voltage Switching (ZVS) modulation of the MOSFET switches S_1 to S_4 without an additional soft switching circuit [2].

Requirements for dc-dc converters in this application are a high efficiency, an highly compact and low cost design as well as a low voltage ripple at the fuel cell and dc-link side of the converter. To minimize the overall converter volume multi-phase converters are proposed [2][3][4] that result in a volume reduction for the passive components due to the higher effective switching frequency achieved by interleaved operation of the phases.

However, in a practical multi-phase converter design non-idealities like tolerances in the inductance values or semiconductor switching times are unavoidable and these lead to an unbalance in the average phase currents and/or sub-harmonics of the effective switching frequency in the output voltage ripple spectrum. While unbalanced currents mainly lead to efficiency drawbacks [5], sub-harmonics, on the other hand, increase the ripple amplitudes since the filter attenuation at low frequencies is not sufficient.

Therefore, the paper gives a model for the analytical calculation of the output voltage ripple of the converter as a function of the buck+boost inductor and the filter component values (section II) and an overview on techniques for ripple reduction. Furthermore, a new method to cancel the voltage ripple caused by the fundamental of the switching frequency is proposed (section III) and experimental results that verify the method of operation are given in section V.

II. Calculation of the Output Voltage Ripple

A clear understanding of the sources that affect the converter output voltage ripple is required in advance to the ripple reduction methods. Thus, in the following an equivalent circuit of

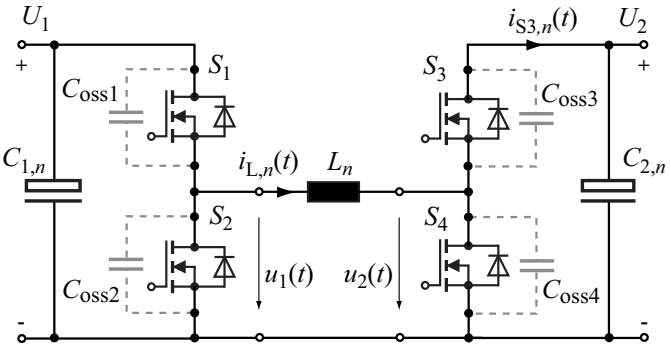

Fig. 1. Cascaded bi-directional buck+boost converter, shown with parasitic MOSFET output capacitances $C_{\mathrm{oss},i}$.

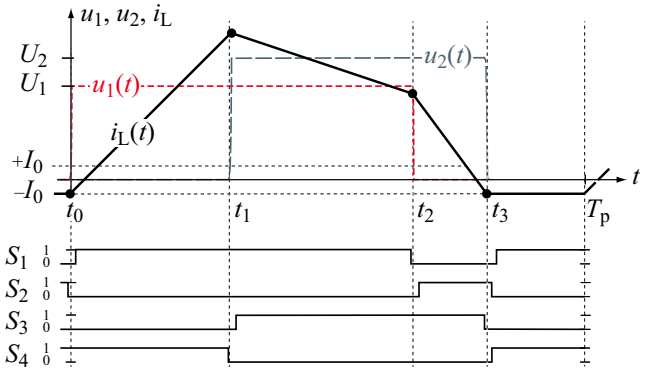

Fig. 2. Basic timing diagram for the switch S_1 to S_4 control signals the and inductor current i_L for boost operation ($U_2 > U_1$). Zero Voltage Switching of the four switches is achieved by a negative offset current at the beginning of the switching period T_p.

the multi-phase converter including the output filter structure is given analytically and verified in hardware. With the model as a basis, the influence of component tolerances is discussed in a next step.

A. Equivalent Circuit of the Multi-Phase Converter

The investigated converter system is built of N_Σ identical phases that are connected in parallel. Each phase is a bi-directional dc-dc converter with the topology depicted in Fig. 1 and consists of two half-bridges with MOSFET switches S_i, the buck+boost inductor L_n and the capacitors $C_{1,n}$ and $C_{2,n}$.

During the constant switching period T_p, the inductor current $i_{L,n}(t)$ is shaped by switching the MOSFETs at the switching times $t = t_i$ (cf. Fig. 2). The current waveform shows a negative offset current $-I_0$ at the beginning of the period that allows ZVS of all four switches because the anti-parallel body diode is conducting at turn-on of a switch and the parasitic output capacitance C_{oss} assists the turn-off process [2]. However, there is a degree of freedom in selecting the switching times t_i and algorithms for an optimized control behavior and optimized efficiency are proposed in [2] and [6].

The output voltage ripple is caused by the buck+boost inductor current that is reason to a charge $Q_{2,n}$ delivered to the output capacitor $C_{2,n}$ during the switching period. The charge $Q_{2,n}$ is a function of L_n, the operating point (U_1, U_2 and the transferred power P_2) and the switching times t_1 to t_3 of the four MOSFET switches S_i. The switching times are assumed to be known and constant for the following calculations. Then, the switch S_3 current is given by

$$i_{\mathrm{S3},n}(t) = \begin{cases} -I_0 + \dfrac{U_2}{L_n}t_1 + \dfrac{U_1 - U_2}{L}t & t_1 < t < t_2 \\ -I_0 + \dfrac{U_1}{L_n}t_2 + \dfrac{U_2}{L_n}(t_1 - t) & \text{for} \quad t_2 < t < t_3 \\ 0 & \text{otherwise} \end{cases} \tag{1}$$

and results in the charge

$$\begin{aligned} Q_{2,n} &= \int_0^{T_\mathrm{p}} i_{\mathrm{S3},n}(t)\mathrm{d}t = \int_{t_1}^{t_3} i_{\mathrm{L},n}(t)\mathrm{d}t = \\ &= c_\mathrm{L} \cdot \frac{1}{L_n} - c_\mathrm{I} I_0 \end{aligned} \tag{2}$$

that is delivered to $C_{2,n}$ during the switching period T_p with the constants

$$\begin{aligned} c_\mathrm{L} &= \frac{1}{2}(2t_2t_3 - t_1^2 - t_2^2)U_1 + \frac{1}{2}(2t_1t_3 - t_1^2 - t_3^2)U_2 \\ c_\mathrm{I} &= t_3 - t_1 \end{aligned} \tag{3}$$

that reflect the operation point. For a single converter phase $Q_{2,n}$ would cause an ac voltage ripple across $C_{2,n}$ with an amplitude of approximately

$$\Delta u_{\mathrm{C2},n} \approx \frac{1}{2C_{2,n}} \cdot Q_{2,n}. \tag{4}$$

However, the converter consists of N_Σ interleaved converter phases and these are connected by a Π-filter that is shown in Fig. 3 where the dc current I_2 and the switch S_3 currents of each converter phase are modeled by current sources. The phase capacitors $C_{2,n}$ that support the switched inductor current $i_{\mathrm{S3},n}(t)$ are connected by filter inductors $L_{\mathrm{f2},n}$ to limit current oscillations between these capacitors. The value of $L_{\mathrm{f2},n}$ thereby is selected as a trade-off of the filter inductor current amplitude, the filter losses and the filter volume. At the same time the higher filter order helps to reduce the overall filter volume for a given output voltage ripple requirement. An equivalent circuit of the filter is found by superposition

$$i_{\mathrm{S3},\Sigma}(t) = \sum_{n=1}^{N} i_{\mathrm{S3},n}(t) \tag{5}$$

of the current sources and is shown in Fig. 4.

In order to calculate the time function of the voltage across the common capacitor $C_{2,0}$ the Fourier coefficients of $i_{\mathrm{S3},\Sigma}(t)$ are multiplied with the filter transfer function $G_\mathrm{U}(s) := U_{\mathrm{C2},0}(s)/I_{\mathrm{S3},\Sigma}(s)$ evaluated at multiples of the

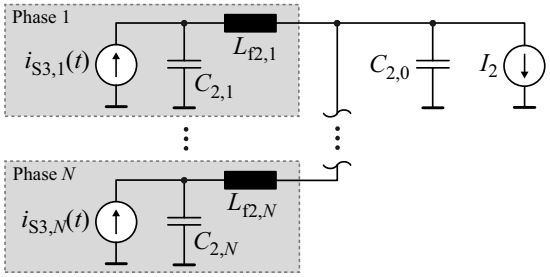

Fig. 3. Filter structure at side 2 of the multi-phase converter shown with the switch S_3 currents $i_{\mathrm{S3},n}(t)$ modeled as current sources, a common capacitor $C_{2,0}$ and the load current I_2; damping elements and the inductor resistance are neglected in the figure.

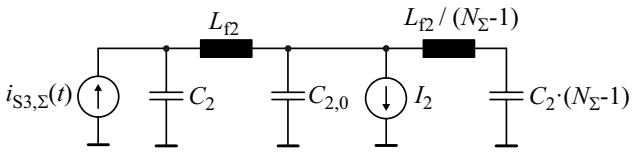

Fig. 4. Filter equivalent circuit for N_Σ converter phases resulting from the superposition of the switch S_3 currents shown in Fig. 3.

fundamental frequency f_{sw}.

$$u_{\mathrm{C2,0}}(t) = \sum_{\nu} \mathrm{e}^{\mathrm{j}\nu\omega t} \cdot \hat{I}_{\mathrm{S3},\Sigma,\nu} \mathrm{e}^{\mathrm{j}\varphi_{\Sigma,\nu}} \cdot G_{\mathrm{U}}\left(\mathrm{j}\nu\omega\right) \qquad (6)$$

In (6) $\hat{I}_{\mathrm{S3},\Sigma,\nu}$ is the amplitude of the ν-th harmonic, $\varphi_{\Sigma,\nu}$ is the associated phase angle and $\omega = 2\pi f_{\mathrm{sw}}$.

The influence of tolerances of the filter components on the output voltage is neglected and the same values $L_{\mathrm{f2},n} = L_{\mathrm{f2}}$, $C_{2,n} = C_2$ are assumed for each phase. Then, based on the the filter equivalent circuit, the transfer function G_{U} including the ac resistance R_{f2} of the filter inductors is calculated by

$$G_{\mathrm{U}}(s) = \frac{1}{\left(C_2 L_{\mathrm{f2}} C_{2,0} \cdot s^2 + C_2 R_{\mathrm{f2}} C_{2,0} \cdot s + \ldots \right.} \quad . \qquad (7)$$
$$\left. \ldots\, C_2 N_\Sigma + C_{2,0}\right) s$$

It is advantageous to operate only a certain number N out of N_Σ converter phases of a multi-phase converter at the same time to improve efficiency in part load conditions [6]. Typically, for the N operated phases equally distributed phase shift angles $\varphi_n = 2\pi\frac{n-1}{N}$ are introduced. The resulting current $i_{\mathrm{S3},\Sigma}(t)$ then shows an effective switching frequency that is N times higher than the phase switching frequency f_{sw}, reducing the voltage ripple $\Delta u_{2,0}$ because of the better filter attenuation at a higher frequency.

B. Verification of the Filter Transfer Function

The filter and output voltage ripple model is verified in hardware with a setup of N_Σ = 3 converter phases and a single phase operated. The electrical specification of the phases is given in table I and the filter component values listed in table II. The measured and calculated capacitor $C_{2,0}$ currents for a single phase operated at U_1 = 400 V, U_2 = 200 V and I_2 = 30 A are shown in Fig. 5. For reasons of accuracy a measurement of the capacitor current instead of the capacitor voltage is chosen because $u_{\mathrm{C2,0}}(t)$ shows an overlaid dc voltage U_2 and is exposed to noise due to the small ac amplitude. As can be seen from the figure, the calculated ripple current that is determined by the product of $\hat{I}_{\mathrm{S3},n}$ and the

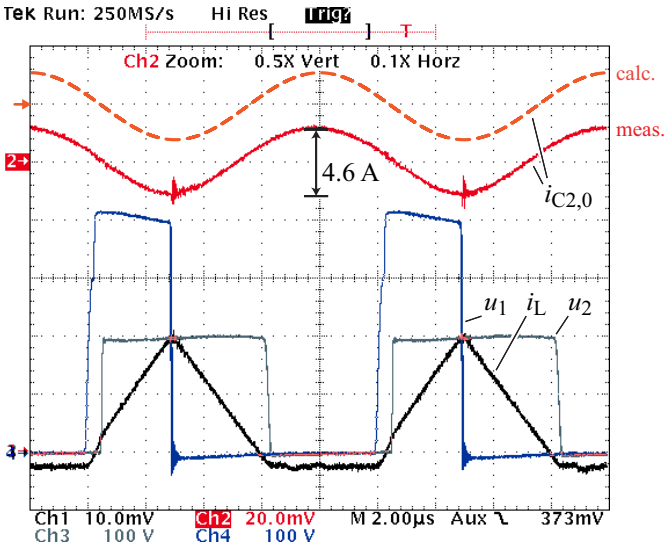

Fig. 5. Verification of the filter transfer function. The model of the common output capacitor $C_{2,0}$ ripple current is in good accordance to the measurement.

transfer function

$$G_{\mathrm{I}}(s) = \frac{C_{2,0}}{C_2 L_{\mathrm{f2}} C_{2,0} \cdot s^2 + C_2 R_{\mathrm{f2}} C_{2,0} \cdot s + \ldots} \qquad (8)$$
$$\ldots C_2 N_\Sigma + C_{2,0}$$

is in very good accordance with the measurement. The actual capacitor voltage can be found by integration of the capacitor current ($u_{\mathrm{C2,0}}(t) = 1/C_{2,0} \cdot \int i_{\mathrm{C2,0}}(t)\mathrm{d}t + U_2$) and the ripple amplitude by multiplication with the capacitor impedance ($\Delta u_{\mathrm{C2,0}} = (2\pi f_{\mathrm{sw}} C_{2,0})^{-1} \cdot \Delta i_{\mathrm{C2,0}}$). The fundamental $\hat{I}_{\mathrm{S3},n}$ is calculated by a Fourier expansion of (1) with the parameters such as the switching times t_i, and the current magnitude extracted from the measurement of $i_L(t)$.

C. Influence of Inductance Tolerances

In a practical realization the buck+boost inductors L_n are subject to production tolerances and thus lead to an asymmetrical average and peak current distribution among the phases as can be seen from (1). This unbalance is reason for subharmonics of the effective switching frequency in the ripple spectrum. To analyze the influence of the tolerances on the voltage ripple, the fundamentals of the switch S_3 currents of each phase are expressed as ripple phasors

$$\vec{i}_{\mathrm{S3},n} = \hat{I}_{\mathrm{S3},n} \cdot e^{\mathrm{j}\varphi_n} \qquad (9)$$

TABLE I
ELECTRICAL SPECIFICATION OF A PHASE MODULE

Name	Parameter	Value
Side 1 voltage range	U_1	150 V .. 450 V
Side 2 voltage range	U_2	150 V .. 450 V
Peak power	$P_{2,n}$	12 kW
Switching frequency	f_{sw}	100 kHz

TABLE II
FILTER COMPONENTS

Name	Value	Condition
C_2	13 µF	U_2 = 200 V
$C_{2,0}$	28 µF	
L_{f2}	4.2 µH	I_2 = 30 A
R_{f2}	50 mΩ	f = 100 kHz

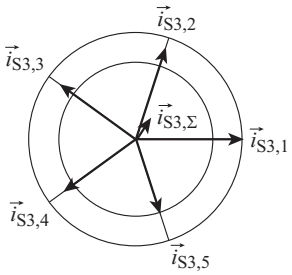

Fig. 6. Ripple phasors for symmetrical interleaving with unsorted phases. The non-zero fundamental of the effective switch S_3 current $\vec{i}_{\mathrm{S3},\Sigma}$ is reason to a sub-harmonic content in the output ripple spectrum.

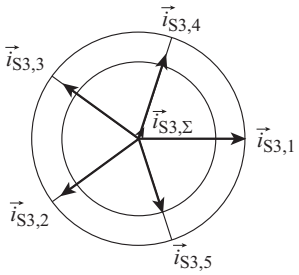

Fig. 7. Ripple phasors for symmetrical interleaving with sorted phases. The fundamental of the effective switch S_3 current $\vec{i}_{\mathrm{S3},\Sigma}$ is reduced by sorting of the ripple phasors.

in the following, where $\hat{I}_{S3,n}$ is the amplitude of the fundamental wave of the associated Fourier expansion ($f = f_{\mathrm{sw}}$) and φ_n is the phase shift angle. This model is of sufficient accuracy in most cases, as it is convenient to design the filter to show a cut-off frequency well below the switching frequency in order to achieve an adequate differential mode attenuation and the higher frequency content of $i_{\mathrm{S3},n}(t)$ is therefore suppressed by the filter.

For a phase count of $N > 1$ the effective ripple phasor is found by the sum

$$\vec{i}_{\mathrm{S3},\Sigma} = \sum_{n=1}^{N} \vec{i}_{\mathrm{S3},n} = \sum_{n=1}^{N} \hat{I}_{\mathrm{S3},n} \cdot e^{\mathrm{j}\varphi_n}, \tag{10}$$

where φ_n directly corresponds to the phase shift angles of the converter phases. As depicted in Fig. 6, (10) can also be graphically visualized as a vector sum. It can be exemplarily seen in the figure for 5 operated phases with phase shift angles that are a multiple of 72° and randomly assigned to the phases, that the vector sum $\vec{i}_{\mathrm{S3},\Sigma}$ is non-zero due to the tolerances. A $\vec{i}_{\mathrm{S3},\Sigma} \neq 0$ implies a sub-harmonic portion in the ripple spectrum at $f = f_{\mathrm{sw}}$ that might increase the voltage ripple amplitude $\Delta u_{2,n}$ and therefore should be kept at a minimum.

III. Proposed Method for Ripple Cancellation

Besides introducing equally distributed phase shift angles $\varphi_n = 2\pi\frac{n-1}{N}$ for the N activated converter phases, there are more sophisticated methods to minimize the output voltage ripple. One method to further reduce the amplitude of $\vec{i}_{\mathrm{S3},\Sigma}$ and therefore also $\Delta u_{2,0}$ is not to randomly assign the angles φ_n to the individual phases, but sorted by the amplitudes $\hat{I}_{\mathrm{S3},n}$ of the ripple phasors [3]. For an even number of phases, two phases with similar $\hat{I}_{\mathrm{S3},n}$ are phase shifted by 180°, respectively. The sorting algorithm is also applicable for an odd number of phases, as shown in Fig. 7. Here, the phasors are ordered by decreasing amplitude and $\vec{i}_{\mathrm{S3},2}$, $\vec{i}_{\mathrm{S3},3}$ are placed opposite to $\vec{i}_{\mathrm{S3},1}$ to reduce the resulting ripple $\vec{i}_{\mathrm{S3},\Sigma}$ in comparison to an unsorted distribution.

With the sorting algorithm good results are obtained for a large number of phases but however, this method does not provide a complete ripple cancellation and additionally is not applicable for a phase count of three. Therefore, for $N = 3$, an adjustment of the phase shift angles is proposed to cancel the ripple phasor $\vec{i}_{\mathrm{S3},\Sigma}$.

The ripple phasors with different amplitudes due to inductor L_n tolerances that are ideally interleaved ($\varphi_n = 0, \frac{2\pi}{3}, \frac{4\pi}{3}$) and sum to an overall ripple phasor of $\vec{i}_{\mathrm{S3},\Sigma}$ are depicted in Fig. 8. As indicated in Fig. 9, there exists a solution for the phase shift angles φ_n, where the sum of the three phasors is zero and thus the fundamental output voltage ripple $\Delta u_{2,0}$ is canceled. In general, there always is an explicit solution

$$\begin{aligned} \varphi_2 &= \pi - 2 \cdot \arctan \frac{r}{s - \hat{I}_{\mathrm{S3},3}} \\ \varphi_3 &= \pi + 2 \cdot \arctan \frac{r}{s - \hat{I}_{\mathrm{S3},2}} \end{aligned} \tag{11}$$

where

$$\begin{aligned} r &= \sqrt{\frac{(s - \hat{I}_{\mathrm{S3},1})(s - \hat{I}_{\mathrm{S3},2})(s - \hat{I}_{\mathrm{S3},3})}{s}} \\ s &= \frac{\hat{I}_{\mathrm{S3},1} + \hat{I}_{\mathrm{S3},2} + \hat{I}_{\mathrm{S3},3}}{2} \end{aligned} \tag{12}$$

when $\forall |L_n/L| \leq \frac{1}{3}$ that is found by the trigonometric calculations.

The proposed ripple cancellation method can further improve the phase sorting method for $N > 3$ activated phases as indicated in Fig. 10. That is when the $N - 2$ phases of the largest ripple amplitude are sorted with ideal phase shift angles, summarized to form a ripple phasor $\vec{i}'_{\mathrm{S3}}$ and (11) is solved with $\vec{i}'_{\mathrm{S3}}$ and the remaining two ripple phasors.

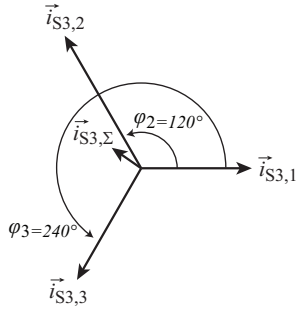

Fig. 8. Ripple phasors and resulting non-zero fundamental $\vec{i}_{\mathrm{S3},\Sigma}$ for equally distributed phase shift angles.

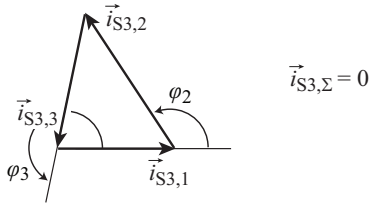

Fig. 9. Ripple phasors for optimized phase shift angles. For a phase count of three, there exists an solution for the phase shift angles that cancel the fundamental $\vec{i}_{S3,\Sigma}$.

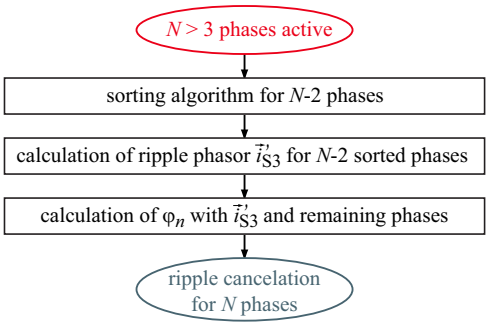

Fig. 10. Combination of sorting and cancellation algorithms for ripple reduction with $N > 3$ phases activated.

IV. Inductor Tolerance Determination

As stated in section III the amplitudes $\hat{I}_{S3,n}$ of the ripple phasors must be known to calculate the phase shift angles φ_n for ripple cancellation or to apply a sorting algorithm. Since these are related to the inductance L_n of phase n and the inductor tolerance ΔL_n respectively, where $L_n = L + \Delta L_n$, either L_n or ΔL_n has to be determined in advance. On the other hand, it might be advantageous to identify these parameters during converter operation. Then, also aging effects or a temperature dependence of L_n can be taken into account. A method to identify the relative inductances in respect to a reference phase is proposed in the following for the converter operated with the ZVS modulation and a passive, i.e. uncontrolled, current balancing. The method however, is also applicable for a discontinuous conduction mode (DCM) in general.

In case of the ZVS operation, a passive current balancing among the phases means that there is no individual current control of each phase and the switches of the N phases are gated with identical timing values t_i, which is preferred because of the reduced amount of required current sensors and overall control effort. The average phase output current $I_{2,n}$ for the converter operated with passive current balancing is calculated from (2) and is given by

$$I_{2,n} = \frac{P_{2,n}}{U_2} = \frac{U_2 Q_{2,n}}{T_\mathrm{p}} \cdot \frac{1}{U_2} \overset{eq.(2)}{=} c'_\mathrm{L} \cdot \frac{1}{L_n} - c'_\mathrm{I} I_0, \qquad (13)$$

where $c'_\mathrm{L} = c_\mathrm{L}/T_\mathrm{p}$ and $c'_\mathrm{I} = c_\mathrm{I}/T_\mathrm{p}$ and $Q_{2,n}$ is the charge delivered to the phase capacitor $C_{2,n}$ during a switching period. Equation (13) is solved and yields an inductor value of

$$L_n = \frac{c'_\mathrm{L}}{I_{2,n} + c'_\mathrm{I} I_0} \qquad (14)$$

and thus for small tolerances ΔL_n the proportionality

$$L_n \sim 1/I_{2,n} \qquad (15)$$

is given. It should be noted that (14), (15) introduce an unbalance of the phase currents

$$I_{2,n} = \frac{I_2}{N} \cdot \frac{1}{1 + \Delta L_n / L} \qquad (16)$$

that has to be considered during the dimensioning of the converter. Furthermore, it can be seen from (1) that for known timing values and voltages, the ac component of $i_{S3,n}(t)$ is scaled by $1/L_n$. That is also why all Fourier coefficients are scaled by the same factor, resulting in the proportionality

$$\hat{I}_{S3,n} \sim 1/L_n \qquad (17)$$

and in conjunction with (15) in

$$\hat{I}_{S3,n} \sim I_{2,n}. \qquad (18)$$

Therefore, when all N phase currents $I_{2,n}$ are measured during the operation of the converter, a triangle similar to Fig. 9 can be constructed with the ratio $I_{2,n}/I_{2,m}$ where m is the index of a reference phase, $n \in [1..N] \setminus m$ and the phase shift angles are determined by (11). When there is no separate current sensor for each of the phases, as can be seen from the system and control block diagram depicted in Fig. 11, a calibration measurement must be carried out where each phase is operated individually at the same voltages U_1, U_2 and timing parameters t_1, t_2, t_3 and the currents $I_2 = I_{2,n}$ are tabularized. However, this method is not practical during nominal converter operation because cycling through the converter phases with constant t_i would cause a load current step.

When a digital control is utilized, as depicted in Fig. 11, there is an alternative. The voltages U_1, U_2 as well as the load current I_2 are measured and controlled by the cascaded controllers $G_{\mathrm{c,U}}$ and $G_{\mathrm{c,I}}$. The current controller output $I_{2,\mathrm{mod}}$ is interpreted as a reference current and is used together with the filtered voltages $U_{1,\mathrm{f}}$, $U_{2,\mathrm{f}}$, a lookup table (LUT) and a linear interpolation of the LUT values to calculate the switching times t_i. As the times t_i or the LUT values respectively are calculated for a nominal inductance L, there will be a mismatch of $I_{2,\mathrm{mod}}$ and $I_{2,\mathrm{n}}$ when $L_n \neq L$ that is related to the inductor tolerance.

This relation is derived, in correspondence with the measurement depicted in Fig. 5, by simplification of (13) under the assumption of $U_2 = \frac{1}{2}U_1$, $t_1 = 0$, $t_3 = 2t_2$ and I_0 = 0 A, as indicated in Fig. 12, and results in the current

$$I_2 = \frac{U_1 t_2^2}{2 L_n T_p}. \qquad (19)$$

Equation (19) is solved for t_2, whereas for a controlled and therefore constant current I_2, the value of t_2 varies for different

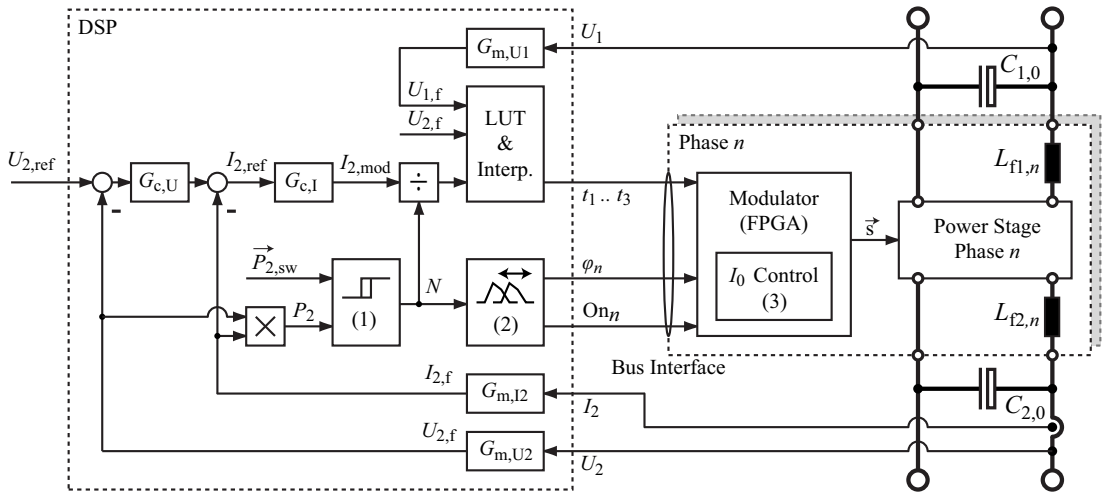

Fig. 11. Interconnection of the N_Σ phase modules by filter inductors $L_{f1,n}$, $L_{f2,n}$ to common input and output capacitors $C_{1,0}$, $C_{2,0}$, controller block diagram of the digital control that implements the proposed ripple reduction method and communication interface between the converter phases.

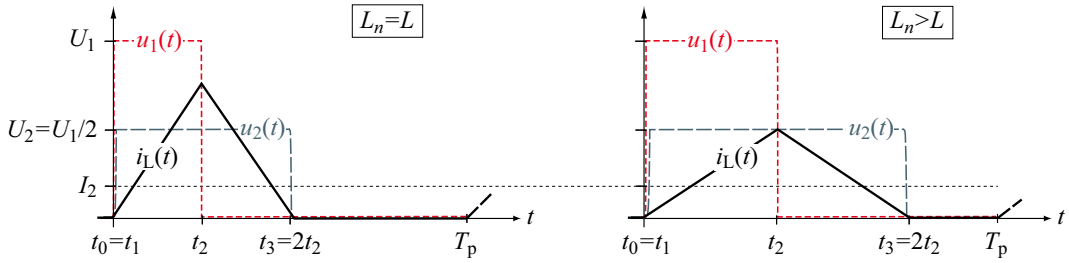

Fig. 12. Simplified inductor current waveforms for the same operation point U_1, U_2, I_2 with an inductance L_n matching the nominal inductance L and an inductance $L_n > L$. The timing t_i, and therefore $I_{2,\mathrm{mod}}$, has to be varied to compensate the inductance mismatch.

inductance values L_n. Under assumption of $L_n \neq L$, e.g. as depicted in Fig. 12 for $L_n > L$, the time t_2 found by the analytical solution with the actual inductance L_n is identical with the time value calculated and set by the controller under assumption of the nominal inductance L:

$$t_2 = \sqrt{\frac{2L_nT_pI_2}{U_1}} \stackrel{!}{=} \sqrt{\frac{2LT_pI_{2,\mathrm{mod}}}{U_1}} \tag{20}$$

Solving (20) for the current controller output $I_{2,\mathrm{mod}}$ yields the proportionality

$$I_{2,\mathrm{mod}} = L_n \cdot \frac{I_2}{L} \sim L_n \tag{21}$$

and

$$\hat{I}_{S3,n} \sim 1/L_n \sim \frac{1}{I_{2,\mathrm{mod}}}. \tag{22}$$

Again, the phase shift angles φ_n are calculated by construction of a triangle similar to Fig. 9 with the ratio $I_{2,\mathrm{mod},m}/I_{2,\mathrm{mod},n}$. With this approach and the fact that the phases can be instantly turned on and off [6], the tolerance measurements can now be carried out during nominal operation at the same operating point U_1, U_2, I_2. Thereto, the current I_2 is controlled and delivered by only a single phase activated at the same time. By cycling through the N phases and storing the controller output variables $I_{2,\mathrm{mod},n}$, a tolerance lookup table is generated.

The results of a calibration of three different converter phases at U_1 = 400 V, U_2 = 200 V and I_2 = 30 A including the calculated phase shift angles φ_n are listed in table III and are utilized as a basis for the experimental verification presented in section V. It should be noted that the inductance values L_n of the phases 2 and 3, that have been originally tuned to show a low tolerance ΔL_n, are intentionally increased to proof the proposed ripple reduction concept.

TABLE III
CALCULATED PHASE SHIFT ANGLES FOR RIPPLE CANCELLATION

Phase	$I_{2,\mathrm{mod}}$	Ratio	φ_n
1	29.8 A	1.00	0.0°
2	40.5 A	0.74	133.2°
3	40.5 A	0.74	226.8°

V. EXPERIMENTAL RESULTS

The proposed ripple cancellation method is verified in hardware with a converter consisting of three identical phases, each with the specifications given in table I, that are connected in parallel to the input and output filter as depicted in Fig. 11. A digital control implemented in a Digital Signal Processor (DSP) generates the timing information t_i and the phase shift angles φ_n, which are calculated by the phase shift controller

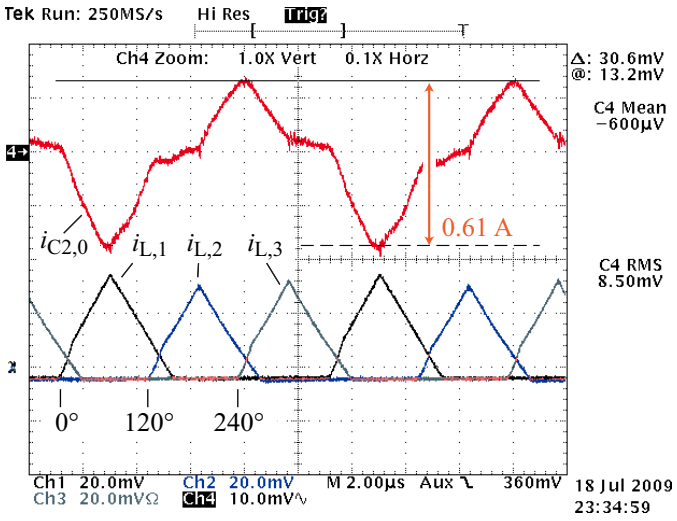

Fig. 13. Measurement of the capacitor $C_{2,0}$ ripple current $i_{\mathrm{C},0}(t)$ (200 mA / 10 mV) and the three inductor currents $i_{\mathrm{L},n}$ (20 A / 10 mV) with equally distributed phase shift angles.

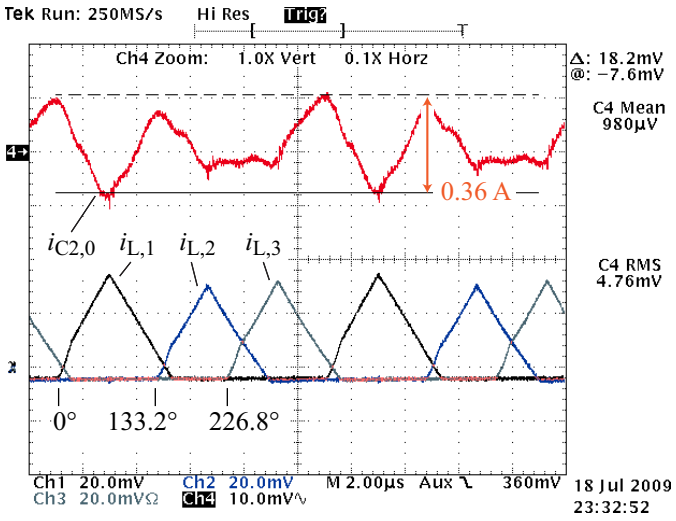

Fig. 14. Measurement of the capacitor $C_{2,0}$ ripple current $i_{\mathrm{C},0}(t)$ (200 mA / 10 mV) and the three inductor currents $i_{\mathrm{L},n}$ (20 A / 10 mV) with the calculated optimum phase shift angles applied.

(2), and forwards these values to the N_Σ phases via a serial communication interface. Details on the additional controllers that decide on the number of activated phases N (1) and implement an offset current control (3) can be found in [6].

The resulting capacitor current ripple for three interleaved phases with equally distributed φ_n is shown in Fig. 13 for U_1 = 400 V, U_2 = 200 V and I_2 = 36 A. The inductor current $i_{L,1}$ of the first phase with the maximum amplitude can clearly be identified as the source of the sub-harmonic content of the ripple current at f = 100 kHz.

With the calculated optimum phase shift angles φ_n listed in table III applied, the current ripple amplitude $\Delta i_{\mathrm{C2,0}}$ is reduced by the factor of 0.61 A / 0.36 A = 1.7 and thus also $\Delta u_{\mathrm{C2,0}}$. Figure 15 illustrates the spectrum of the measured ripple current $i_{\mathrm{C},0}(t)$. Due to the adjustment of the phase shift angles the sub-harmonic content in the spectrum is shifted toward higher frequencies as intended.

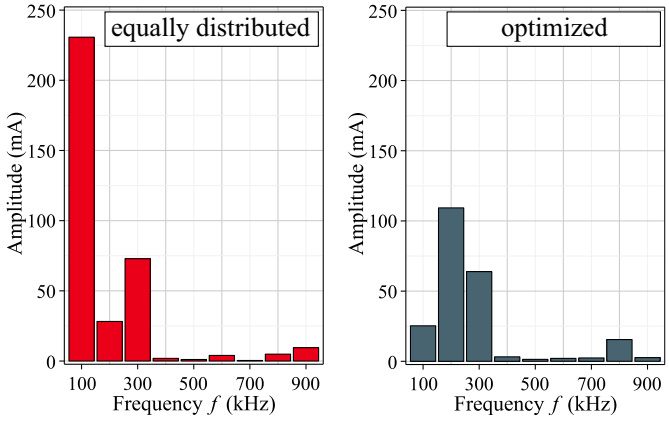

Fig. 15. Current ripple $\Delta\vec{i}_{\mathrm{C2,0}}$ spectrum without and with optimum phase shift angles φ_n.

VI. Conclusion

In this paper a detailed analytical model for calculation of the output voltage ripple of a bi-directional multi-phase automotive dc-dc converter is given under consideration of the output filter and the influence of tolerances in the buck+boost inductors. Furthermore, basic methods to reduce the ripple quantities are discussed, including the introduction of an interleaved operation and sorting of the phase shift angles.

A novel method to minimize the content of the fundamental frequency in the output voltage ripple spectrum and a strategy to measure the tolerances during operation of the converter are proposed. The models and the operational concept are verified by measurements with a converter consisting of three interleaved phases and a reduction of the voltage ripple amplitude of approximately 40% is achieved.

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