Comparative Evaluation of Soft-Switching Concepts for Bi-directional Buck+Boost Dc-Dc Converters

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***Abstract*—Soft-switching techniques are an enabling technology to further reduce the losses and the volume of automotive dc-dc converters, utilized to interconnect the high voltage battery or ultra-capacitor to the dc-link of a Hybrid Electrical Vehicle (HEV) or a Fuel Cell Vehicle (FCV). However, as the performance indices of a power electronics converter, such as efficiency and power density, are competing and moreover dependent on the underlying specifications and technology node, a comparison of different converter topologies naturally demands detailed analytical models. Therefore, to investigate the performance of the ARCP, CF-ZVS-M, SAZZ and ZCT-QZVT soft-switching converters, the paper discusses in detail the advantages and drawbacks of each concept, and the impact of the utilized semiconductor technology and silicon area on the converter efficiency. The proposed analytical models that correlate semiconductor, capacitor and inductor losses with the component volume furthermore allow for a comparison of power density and to find the η-ρ-Pareto-Front of the CF-ZVS-M converter.**

***Index Terms*—Automotive, dc-dc converter, soft-switching**

I. Introduction

Hybrid Electrical Vehicles (HEV) and Fuel Cell Vehicles (FCV) utilize bi-directional dc-dc converters to interface an energy storage device such as a high voltage battery or a supercapacitor to a high voltage dc-link. This secondary power source delivers peak power during the acceleration phase of the vehicle and is also beneficial to improve the overall drive train efficiency. This is because either recuperated braking or excess energy that is available when the primary power source is operated at maximum efficiency can be recovered. The dc-dc converter must therefore allow bi-directional operation and should show a high efficiency both at peak power (acceleration phase and recuperation) and in the part load operation (battery State Of Charge (SOC) energy management during non-acceleration phases). When the application requires a buck and a boost operation in both directions of power flow, converters based on the cascaded buck-boost structure depicted in Fig. 1 consisting of four switches S_1 to S_4 are commonly utilized.

However, in a hard-switched operation, switching losses at a high switching frequency become significant and reduce efficiency. On the other hand, as the volume of the passive components decreases with frequency, compact converters are only feasible at a reasonably high switching frequency. Thus, disregarding cost aspects, in the design phase of a converter a compromise between efficiency η and power density ρ must be found, where the limiting curve between these two contrary quantities is the η-ρ-Pareto-Front [1].

Soft-switched dc-dc converters are beneficial to reduce switching losses and thus to achieve a high efficiency over a wide operating voltage and power range. There are two major categories that classify this type of converters. Firstly, resonant converters that achieve a soft-switching by proper gating of the main switches S_1 to S_4, e.g. the cascaded buck+boost converter operated with the Constant-Frequency Zero Voltage Switching Quasi-Square-Wave (CF-ZVS-QSC) method [2][3] or the Constant-Frequency Zero Voltage Switching Modulation (CF-ZVS-M) [4]. Secondly, PWM converters extended by auxiliary circuitry such as the Auxiliary Resonant Commutated Pole (ARCP) converter (cf. Fig. 2) [5][6], the Zero Current Transition Quasi Zero Voltage Transition (ZCT-QZVT) converter (cf. Fig. 4) [7][8] or the Snubber Assisted Zero Voltage and Zero Current Transition (SAZZ) converter (cf. Fig. 3) [9][10].

There are realizations of these soft-switching converters that show an outstanding power density ($\approx$ 40kW/l [10]) and/or efficiency ($\approx 99\%$ [10][11]), but a comprehensive comparison of the concepts has not yet been published. Moreover, results are published for converters that differ in the specifications such as the operating voltage range or output voltage ripple requirements and make a direct comparison difficult or even completely impossible. Therefore, the paper focuses on a comparison of the ARCP, CF-ZVS-M, SAZZ and ZCT-QZVT converters based on common specifications, technology standards and analytical loss and volume models that are verified with experimental results.

The paper presents the converter models including the dimensioning criteria of the components, and their current and voltage ratings (Section II) and loss and volume models of the active and passive components (Section III). A comparison of the different concepts is given in Section IV.

II. Analytical Modeling of the Concepts

As a direct comparison of the four concepts considered based on published results is not feasible due to different specifications, the dimensioning criteria for each of the components given in the following are under consideration of the a voltage range $U_1 = U_2 = U_{\min}..U_{\max} =$ 150V .. 450V and a peak power rating of $P_{\max} =$ 12kW per converter module. The comparison is carried out for a single converter module only with maximum ripple amplitudes across the capacitors C_1 and C_2 of $\hat{\tilde{u}}_{\mathrm{C}} =$ 5V. All equations will be given in dependence of the voltage transfer ratio $v = U_2/U_1$ and the normalized inductor impedances $Z = L/T_{\mathrm{p}}$ and $Z_{\mathrm{x}} = \sqrt{L_{\mathrm{x}}/C_{\mathrm{x}}}$, where $T_{\mathrm{p}} = 1/f_{\mathrm{sw}}$ is the switching period.

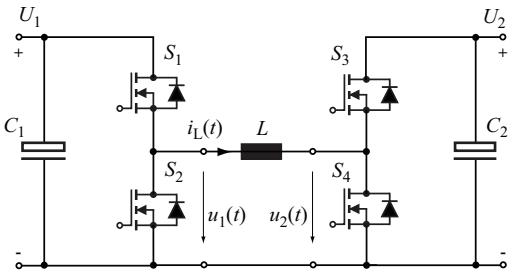

Fig. 1. Cascaded buck-boost converter applicable for PWM modulation or Constant-Frequency ZVS Modulation (CF-ZVS-M).

A. PWM Converter Concepts

For the ARCP, SAZZ and ZCT converters, depending on the mode of operation (buck or boost) and direction of power flow, either the main switches S_1, S_2 or S_3, S_4 are operated with Pulse Width Modulated (PWM) gating signals, e.g. S_1, S_2 for buck operation and energy transfer from side 1 to side 2. The switch S_3 is turned on continuously in that case.

In the bi-directional buck-boost configuration MOSFET switches are advantageous, as their unipolar structure permits a reduction of diode conduction losses by synchronous rectification. As there are no current tailing effects present that would affect the design of the auxiliary circuits shown later, a higher switching frequency and thus a higher power density is achieved. When synchronous rectification is utilized and the inductor current is permitted to show negative values [10], the converter does not enter the Discontinuous Conduction Mode (DCM) and the duty cycle $D_1 = t_1/T_\mathrm{p}$ is a function of solely the voltage transfer ratio, e.g. $D_1 = v$ for the buck operation. Then, for a given worst-case relative ripple current amplitude $r_\mathrm{L} = \hat{\tilde{i}}_\mathrm{L}/I_\mathrm{max}$, that is observed for $v = 1/2$ or $v = 2$, the required main inductance is given by

$$L = \frac{U_\mathrm{max} T_\mathrm{p}}{8 r_\mathrm{L} I_\mathrm{max}} \tag{1}$$

where $r_\mathrm{L} \approx 50\%$ is considered as a reasonable trade-off between high-frequency losses due to the ripple current and power density [10]. The values of the capacitors C_1 and C_2 are identical for symmetrical voltage ranges that include $v = 1/2$ or $v = 2$ and calculated by

$$C_1 = C_2 = \frac{I_\mathrm{max} T_\mathrm{p}}{8 \hat{\tilde{u}}_\mathrm{C}}. \tag{2}$$

The most important quantities required to select the semiconductors and to design the main inductor L are the inductor and the switch S_i RMS currents, which are given by

$$I_\mathrm{L,rms} = \sqrt{\frac{\kappa_v}{12}\left(\frac{U_1}{Z}\right)^2 + \frac{1}{v^2}\left(\frac{P}{U_1}\right)^2} \tag{3}$$

$$\begin{aligned} I_\mathrm{S1,rms} &= \sqrt{\frac{v\kappa_v}{12}\left(\frac{U_1}{Z}\right)^2 + \frac{1}{v}\left(\frac{P}{U_1}\right)^2} \\ I_\mathrm{S2,rms} &= \sqrt{\frac{(1-v)\kappa_v}{12}\left(\frac{U_1}{Z}\right)^2 + \frac{1-v}{v^2}\left(\frac{P}{U_1}\right)^2} \end{aligned} \tag{4}$$

and $I_\mathrm{S3,rms} = I_\mathrm{L,rms}$, $I_\mathrm{S4,rms} = 0$ in the buck operation mode, where $\kappa_v = v^4 - 2v^3 + v^2$, and under consideration of the inductor ripple current but for constant voltages U_1, U_2.

B. ARCP Converter

Two auxiliary switches plus series diodes for the ARCP converter to achieve a bi-directional blocking capability, one auxiliary inductor L_x and two capacitors C_x across the main switches are added per half-bridge as shown in Fig. 2. When the auxiliary switch is turned on, the resonant capacitor C_x is discharged and the main switch can be turned on under Zero Voltage Switching (ZVS) conditions. The snubber is connected to an auxiliary voltage source, which is half the voltage U_1 or U_2, respectively.

The switches are gated as shown in Fig. 2 for the buck operation. At $t = t_0$ the auxiliary switch S_x1 is turned on under Zero Current Switching (ZCS). However, switching losses occur due to the fact that the energy

$$E_\mathrm{Sx,turn-on} = \frac{2}{3} C_\mathrm{oss} \sqrt{U_\mathrm{ds,ref}} U_1^{3/2} \tag{5}$$

stored in the output capacitance C_oss of the auxiliary switch during the blocking state is wasted. Equation (5) is found under the assumption that, according to [12], the nonlinear characteristic of the MOSFET output capacitance is approximated by

$$C_\mathrm{oss}(u_\mathrm{ds}) \approx C_\mathrm{oss,ref} \sqrt{\frac{U_\mathrm{ds,ref}}{u_\mathrm{ds}}}. \tag{6}$$

During the time interval $t_0 < t < t_1$ the resonant inductor current i_x rises linearly ($U_\mathrm{Lx1} = U_1/2$) and the main inductor current I_L is taken over by the resonant circuit. When i_x reaches I_L at $t = t_1$, the diode of switch S_2 is turned off and the resonant current charges C_x2 and discharges C_x1 in the subsequent time interval $t_1 < t < t_2$. At $t = t_2$ the voltage u_S1 across the main switch S_1 has reached zero and S_1 can be turned on under ZVS. The resonant current reaches zero at $t = t_3$ ($U_\mathrm{Lx1} = -U_1/2$ for $t_2 < t < t_3$) and reverse recovery of the diode D_1 occurs. Therefore, fast recovery diodes should be selected for D_1 to D_4. The auxiliary switch can be turned off under ZCS afterwards. Based on the timing, the average and RMS values of the resonant current for the buck operating

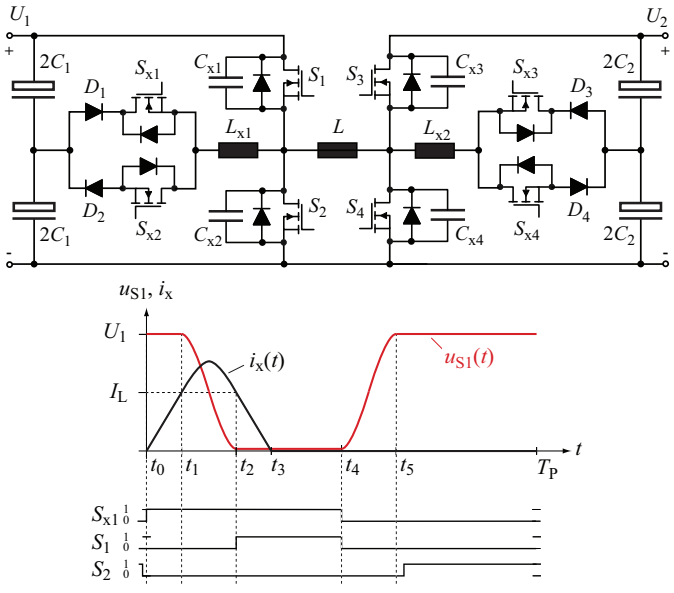

Fig. 2. ARCP converter and waveforms for the buck operation mode.

mode are calculated by

$$I_{\mathrm{Sx1,avg}} = \frac{L_\mathrm{x}\left(2P^2Z_\mathrm{x}^2 + U_1^4v^2 + PU_1^2vZ_\mathrm{x}\pi\right)}{T_\mathrm{p}U_1^3v^2Z_\mathrm{x}^2}$$
$$I_{\mathrm{Sx1,rms}} = \sqrt{\frac{L_\mathrm{x}}{T_\mathrm{p}}\left(\frac{4P^3}{3U_1^4v^3} + \frac{P^2\pi}{U_1^2v^2Z_\mathrm{x}} + \frac{2P}{vZ_\mathrm{x}^2} + \frac{U_1^2\pi}{8Z_\mathrm{x}^3}\right)}. \quad (7)$$

C. SAZZ Converter

The SAZZ converter (cf. Fig. 3) auxiliary circuit topology is very similar to the ARCP concept. However, in the SAZZ converter one auxiliary inductor per auxiliary switch provides a greater flexibility in the connection of the snubbers to the auxiliary voltage source, which allows to optimize the auxiliary losses to a certain extent. In addition, the diodes D_2, D_4, D_6, D_8 are introduced in series to the resonant capacitors which is why, contrary to the ARCP converter, only the capacitor $C_{\mathrm{x}1}$ is discharged during the time interval $t_1 < t < t_2$ (cf. Fig. 2). The average and RMS values of the current in the additional diode D_2 are given by

$$I_{\mathrm{D2,avg}} = \frac{L_\mathrm{x}P\left(2PZ_\mathrm{x} + U_1^2v\pi\right)}{T_\mathrm{p}U_1^3v^2Z_\mathrm{x}}$$
$$I_{\mathrm{D2,rms}} = \sqrt{\frac{4L_\mathrm{x}P^3}{3T_\mathrm{p}U_1^4v^3} + \frac{L_\mathrm{x}P^2\pi}{T_\mathrm{p}U_1^2v^2Z_\mathrm{x}}}. \quad (8)$$

When IGBTs are used for S_1 to S_4, a design criteria for the resonant capacitors are the tail current losses that introduce a lower limit for the half period $T_\mathrm{x} = t_2 - t_1$ of the auxiliary circuit resonant tank [13]. In the case of MOSFET switches L_x and C_x should be optimized for lowest total auxiliary losses, whereas the semiconductor conduction losses, high frequency losses and core losses of the resonant inductor (cf. Section III) and the reverse recovery of the main switch diodes should be taken into account.

At a higher switching frequency L_x typically is in the range of $L_\mathrm{x} \lesssim 1\mu\mathrm{H}$ and $C_\mathrm{x} = 3{\times}6.8\mathrm{nF}$ for the 50kHz SAZZ converter proposed in [10]. One drawback arises from a low auxiliary inductance. When an auxiliary switch of the ARCP or SAZZ converter is turned off, the switch output capacitance C_oss must be charged to the blocking voltage by the auxiliary inductor current. The resulting ringing in the current and the switch voltage results in additional losses. One method to reduce these losses is the application of saturable auxiliary inductors that show a high inductance at a low current to suppress the ringing and the nominal value L_x when saturated.

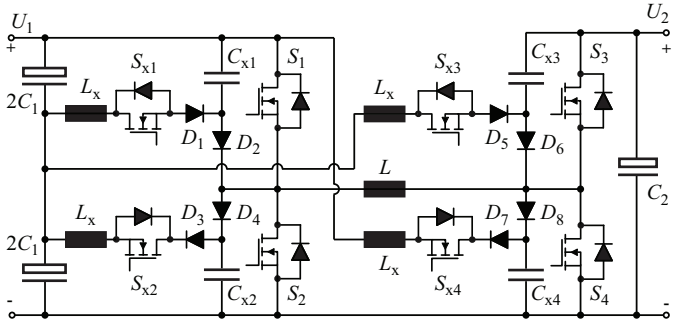

Fig. 3. Bi-directional SAZZ converter with optimized auxiliary circuit [10].

D. ZCT-QZVT Converter

The ZCT-QZVT converter is depicted in Fig. 4 where two auxiliary switches and a resonant tank consisting of one capacitor and an inductor are added per bridge-leg to achieve a Zero Current Switching of the main switches S_i. As can be seen from the waveform given in Fig. 4, in the buck operation mode, the auxiliary switch $S_{\mathrm{x}2}$ is turned on under ZCS at $t = t_0$ and a resonant transition is initiated. At $t = t_3$ the main inductor current is solely sourced by the resonant tank and S_1 can be turned on under ZCS. Turn-on losses are generated, however, as the voltage across S_1 is low but not zero (Quasi Zero Voltage Transition, QZVT). At $t = t_5$ the auxiliary switch $S_{\mathrm{x}1}$ is turned on and during the resonant transition S_1 is turned off under ZVS at $t = t_7$ because the anti-parallel diode is conducting. Both auxiliary switches are turned off under ZVS at t_3 and t_{11}, respectively.

The design rules

$$C_\mathrm{x} = \frac{I_\mathrm{max}}{2U_\mathrm{min}} \cdot \frac{(2+k_\mathrm{off})T_\mathrm{off}}{\arccos\frac{1}{k_\mathrm{off}}}$$
$$L_\mathrm{x} = \frac{U_\mathrm{min}}{2I_\mathrm{max}} \cdot \frac{T_\mathrm{off}}{(2+k_\mathrm{off})\arccos\frac{1}{k_\mathrm{off}}} \quad (9)$$

for the resonant capacitor and inductor are given in [8] and values of $C_\mathrm{x} = 153\mathrm{nF}$ and $L_\mathrm{x} = 0.19\mu\mathrm{H}$ are calculated for the given converter operating range. One major drawback of the ZCT-QZVT converter is that C_x and L_x need to be determined for the minimum dc-link voltage U_min such that at $t = t_7$ the peak resonant current is well above the maximum main inductor current I_max with $k_\mathrm{off} \approx 1.3$ being a safety factor. As a consequence, high resonant peak currents result near the upper limit of the dc-link voltage range and reduce the ZCT-QZVT converter efficiency as will be shown in Section IV.

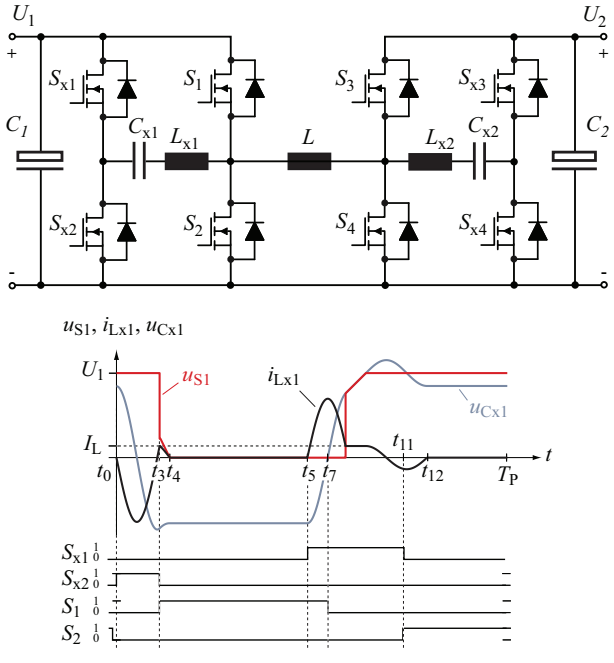

Fig. 4. ZCT-QZVT converter topology and typical waveforms for the buck operation mode.

E. CF-ZVS-M Converter

Contrary to the ARCP, SAZZ and ZCT-QZVT converters, the CF-ZVS-M method of soft-switching of the switches S_1 to S_4 of the cascaded buck-boost converter (cf. Fig. 1) is achieved without an additional auxiliary circuit. This is due to the fact that with the help of the current of inductor L the total charge $Q_{\mathrm{oss},\Sigma}$ stored in one of the output capacitances of the two MOSFET switches in a half-bridge is transferred to the other after turn-off of the first switch. When the resonant transition completes, the second switch is turned on under ZVS [4]. The inductor current i_{L} thereto must be shaped by gating the switches S_i as depicted in Fig. 5 and shows a negative offset current $-I_0$. The minimum required magnitude of I_0 to achieve ZVS depends on the charge stored in the MOSFET output capacitances

$$Q_{\mathrm{oss}}(u_{\mathrm{ds}}) = \int_0^{u_{\mathrm{ds}}} C_{\mathrm{oss}}(u')\mathrm{d}u' = 2C_{\mathrm{oss,ref}}\sqrt{u_{\mathrm{ds}}U_{\mathrm{ds,ref}}} \quad (10)$$

that is calculated by integration of (6). However, $Q_{\mathrm{oss},\Sigma}$ depends on the Silicon area utilized by the both switches in the half-bridge and therefore is calculated from

$$Q_{\mathrm{oss},\Sigma} = 2C^*_{\mathrm{oss}}(A_{\mathrm{Si},1} + A_{\mathrm{Si},2})\sqrt{u_{\mathrm{ds}} \cdot U_{\mathrm{ds,ref}}} \quad (11)$$

where C^*_{oss} is the specific output capacitance at $U_{\mathrm{ds,ref}}$. For example when the voltage U_1 is applied to the inductor L (resonant transition at the side 1 half-bridge at $t = 0$ in buck mode), a minimum current I_0 is required to complete the resonant transition which can be calculated from the energy balance

$$U_1(Q_{\mathrm{oss},\Sigma}(U_1) + Q_{\mathrm{rr}}) \approx \frac{1}{2}LI_0^2. \quad (12)$$

In (12), Q_{rr} is the reverse recovery charge stored in the anti-parallel body diode at the start of the resonant transition that has to be removed from the diode. A detailed model will be given in the transaction version of the paper. Solving (12) for I_0 and neglecting the reverse recovery charge results in

$$I_0 = 2U_1^{3/4}U_{\mathrm{ds,ref}}^{1/4}\sqrt{\frac{C^*_{\mathrm{oss}}(A_{\mathrm{Si},1} + A_{\mathrm{Si},2})}{L}}. \quad (13)$$

By use of (13), the RMS values of the switch and inductor currents can be approximated, e.g.

$$I_{\mathrm{L,rms}} \leq \sqrt{\frac{2\sqrt{2}}{3} \cdot \frac{v^4 + v^3 + v^2 + v + 1}{v(v^2 + v + 1)^{3/2}}\sqrt{\frac{P^3}{ZU_1^2}} + I_0^2} \quad (14)$$

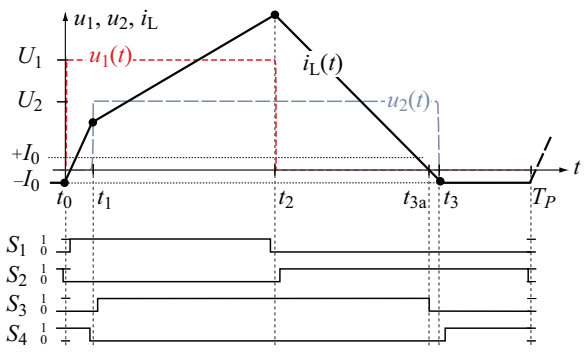

Fig. 5. CF-ZVS-M waveform for the buck operation mode.

Equation (14) is considered as an upper limit of the RMS current, which in a practical implementation of the CF-ZVS modulation and especially in the part load operation and for $v \approx 1$ could be reduced further by optimization of the switching times t_i [14].

There exists an upper limit for the inductance L dependent on the specified peak power P_{max} and the specified operating voltage range. A method to select L is given in [4]. For equal voltage ranges U_1 and U_2 the capacitance required to limit the peak voltage ripple to $\hat{\tilde{u}}_{\mathrm{C}}$ are calculated from

$$C_1 = C_2 = \frac{T_{\mathrm{p}}}{\hat{\tilde{u}}_{\mathrm{C}}}\left(\frac{P_{\mathrm{max}}}{U_{\mathrm{max}}} + \frac{2ZP^2_{\mathrm{max}}}{U^3_{\mathrm{max}}} - \frac{6\sqrt{14ZP^3_{\mathrm{max}}}}{7U^2_{\mathrm{max}}}\right). \quad (15)$$

III. Loss and Volume Models

As switching losses are low for the soft-switching converter topologies presented in Section II, the most important loss contributions are the semiconductor conduction losses, the MOSFET gate losses and the losses of main and auxiliary inductors. As component losses and volume are mutually coupled, e.g. a large-sized inductor has lower losses, accurate models that correlate these two quantities are required to analytically calculate the performance indices of a converter, such as efficiency and power density.

A. Semiconductor Losses

The conduction losses of a MOSFET switch are proportional to the on-resistance $R_{\mathrm{DS(on)}}$. However, in order to directly compare different devices and device technologies, it is more convenient to consider specific device characteristics that are referred to the utilized silicon area. The conduction losses of a power MOSFET are then given by

$$P_{\mathrm{S,cond}} = \frac{R^*_{\mathrm{DS(on)}}}{A_{\mathrm{Si}}}I^2_{\mathrm{S,rms}} \quad (16)$$

where $R^*_{\mathrm{DS(on)}}$ is the specific on-resistance and A_{Si} the chip size. The on-resistance if a function of the junction temperature T_{j} and the drain current density J_{D}.

$$R^*_{\mathrm{DS(on)}} = R^*_{\mathrm{DS(on)}}\Big|_{T_{\mathrm{j}}=T_{\mathrm{j,ref}},J_{\mathrm{D}}=J_{\mathrm{D,ref}}} \cdot (1 + \alpha_1\Delta T_{\mathrm{j}} + \alpha_2\Delta T_{\mathrm{j}}^2) \cdot (1 + \beta_1\Delta J_{\mathrm{D}} + \beta_2\Delta J_{\mathrm{D}}^2) \quad (17)$$

In (17) ΔT_{j} and ΔJ_{D} are the deviations from the reference junction temperature $T_{\mathrm{j,ref}}$ and reference drain current density $J_{\mathrm{D,ref}}$.

The specific on-resistance of different 600V MOSFET switches in dependence of J_{D} is compared in Fig. 6. It can be seen clearly from the figure that the Super Junction devices show a significantly reduced $R^*_{\mathrm{DS(on)}}$ due to their pillar-like charge compensation structures.

In spite of the soft-switching principle there are semiconductor losses dependent on the converter switching frequency f_{sw}, which are calculated from the loss energy $E_{\mathrm{S,i}}$

$$P_{\mathrm{S,sw}} = f_{\mathrm{sw}}\sum_i E_{\mathrm{S,i}}. \quad (18)$$

The switching losses may include the MOSFET turn-on losses $E_{\mathrm{S,turn-on}}$ (5) under ZCS and the reverse recovery losses E_{rr}

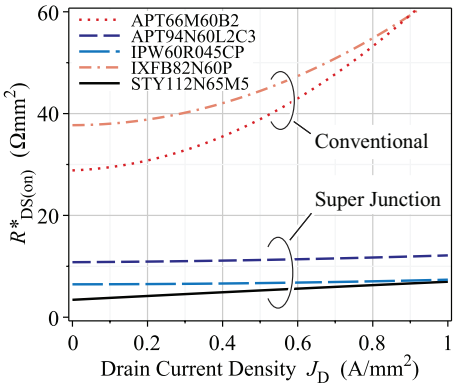

Fig. 6. Specific MOSFET on-state resistance as function of drain current density J_D at T_j = 150°C. The Super Junction devices (APT94N60L2C3, IPW60R045CP, STY112N65M5) offer a significantly better performance in comparison to the conventional device families.

of the internal body diode. Another important contribution are the gate losses

$$E_{\mathrm{S,gate}} = \frac{Q^*_\mathrm{G} A_\mathrm{Si}}{U_{\mathrm{gs,ref}}} U^2_\mathrm{gs} \tag{19}$$

which are equal to 4.8W for the 100kHz CF-ZVS-M converter described in [4] where U_gs = 12V and 9.5W for the 50kHz SAZZ converter [10] where $U_\mathrm{gs} = \pm$12V.

Based on the above explanations, a MOSFET utilized in a soft-switching converter can be characterized by the Figure of Merit $\mathrm{FOM_S} = (R^*_{\mathrm{DS(on)}} Q^*_\mathrm{G} C^*_\mathrm{oss})^{-1}$.

The MOSFET junction temperature T_j depends on the thermal resistance between die and the coolant (coolant temperature T_f) and the total MOSFET losses $P_\mathrm{S} = P_{\mathrm{S,cond}} + P_{\mathrm{S,sw}}$ and is calculated by

$$T_\mathrm{j} = P_\mathrm{S} R_{\mathrm{th,j-f}} + T_\mathrm{f}. \tag{20}$$

As can be seen from (16) and (20) power losses and junction temperature are interlinked, however, the equations can be solved for the thermal equilibrium values and yield

$$P_{\mathrm{S,eq}} = \frac{1-\sqrt{\kappa_1}}{2\alpha_2 \kappa_2 R^2_{\mathrm{th,j-f}} I^2_{\mathrm{S,rms}}} - \frac{\frac{\alpha_1}{2\alpha_2} + T_\mathrm{f} - T_\mathrm{ref}}{R_{\mathrm{th,j-f}}} \tag{21}$$

with

$$\kappa_1 = 1 - \big(4\alpha_2(T_\mathrm{f} - T_\mathrm{ref}) + 2\alpha_1\big)\kappa_2 R_{\mathrm{th,j-l}} I^2_{\mathrm{S,rms}} + \\ + \big((\alpha_1^2 - 4\alpha_2)\kappa_2 I^2_{\mathrm{S,rms}} - 4\alpha_2 P_{\mathrm{S,sw}}\big)\,\kappa_2 R^2_{\mathrm{th,j-f}} I^2_{\mathrm{S,rms}} \tag{22}$$

and

$$\kappa_2 = \frac{R^*_{\mathrm{DS(on)}}}{A_\mathrm{Si}} \left(1 + \beta_1 \frac{I_{\mathrm{S,rms}}}{A_\mathrm{Si}} + \beta_2 \frac{I^2_{\mathrm{S,rms}}}{A^2_\mathrm{Si}}\right). \tag{23}$$

Finally, the conduction losses in the auxiliary circuit diodes are given by

$$P_{\mathrm{D,cond}} = U_{\mathrm{F,D}} I_{\mathrm{D,avg}} + \frac{r^*_\mathrm{D}}{A_\mathrm{Si}} I^2_{D,rms} \tag{24}$$

where the temperature and current dependence of the forward voltage $U_{\mathrm{F,D}}$ and the specific resistance r^*_D is neglected as the diode losses have a rather low impact on the total conduction losses.

The specific parameters of the MOSFETs and diodes required for the loss calculations are given in Table I. $U_{\mathrm{ds,ref}}$ should be chosen in a way that the error due to the approximation of the MOSFET output capacitance (6) remains low. It should also be noted that the effective carrier lifetime for the APT94N60L2C3 body diode was determined from measurements with the SPW47N60C3 MOSFET that has the same specific parameters at half the chip size.

B. Semiconductor Volume

The semiconductor losses can easily be related to the occupied volume under the following assumptions. Firstly, liquid cooling of the semiconductors with a cold plate that has a thickness of h_CP = 4mm is assumed, where the surface area of the cold plate is calculated from the silicon area

$$A_\mathrm{CP} = f_\mathrm{pkg} A_\mathrm{Si}, \tag{25}$$

where the factor f_pkg = 5 (determined for the ST STY112N65M5 MOSFET) area is introduced to consider the overhead caused by packaging of the Silicon chips and the connecting pins. Secondly, with a thickness h_pkg = 8mm of the package including mounting with a screw, clamp or plate as depicted in Fig. 8 the semiconductor volume is given by

$$V_\mathrm{S} = A_\mathrm{CP} h_\mathrm{pkg} = f_\mathrm{pkg} A_\mathrm{Si} h_\mathrm{pkg}. \tag{26}$$

TABLE I
SEMICONDUCTOR DEVICE PARAMETERS

MOSFET Parameters					
Device	U_DSS V	A_Si mm^2	$R^*_{\mathrm{DS(on)}}$ Ωmm^2	C^*_oss pF/mm^2	Q^*_G nC/mm^2
APT94N60L2C3	600	139	4.08	32	3.63
IPW60R045CP	600	69	2.50	11.6[1)]	2.17
IXFB82N60P	600	193	14.0	7.7	1.24
STY112N65M5	650	123	1.52	4.3	2.90

Diode Parameters					
Device	U_RRM V	A_Si mm^2	r^*_D Ωmm^2	$U_{\mathrm{F,D}}$ V	$\tau_{\mathrm{c,eff}}$ ns
APT94N60L2C3	600	139	0.52	0.73	480[3)]
IXFB82N60P	600	193	0.48	0.70	129
STY112N65M5	650	123	0.69	0.74	380
DSEE29-12CC	600	19[2)]	0.40	1.80	

$R^*_{\mathrm{DS(on)}}$ at J_D = 0.5A/mm^2
[1)] at $U_{\mathrm{ds,ref}}$ = 50V, otherwise at $U_{\mathrm{ds,ref}}$ = 25V
[2)] per diode, package contains two chips
[3)] measured value for SPW47N60C3

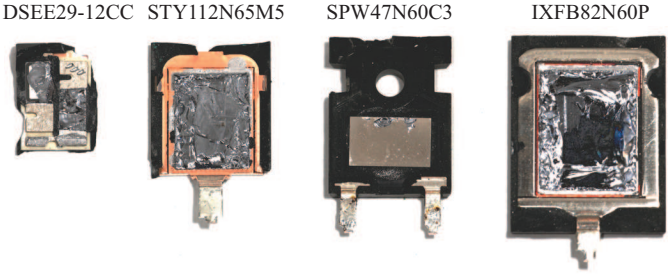

Fig. 7. Package interior showing the chip sizes for several of the semiconductor devices listed in Table I.

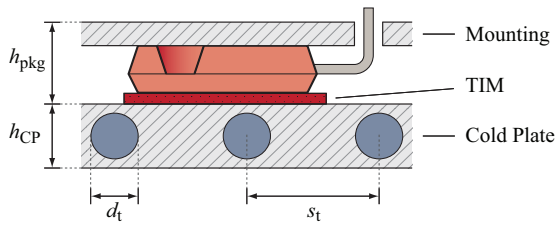

Fig. 8. Semiconductor - cold plate assembly, h_{pkg} is the height required for mounting the semiconductor package onto an aluminium cold plate with tubes of diameter d_t and a tube spacing of s_t.

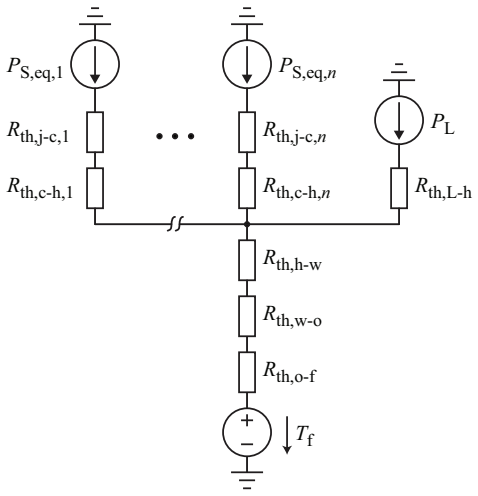

Fig. 9. Simplified thermal model of n semiconductors and an inductor mounted on a cold plate.

A simplified thermal model of the semiconductor cold plate assembly for a steady state operation is shown in Fig. 9. The total R_{th} is a function of the thermal resistance between junction and case $R_{th,j-c}$ approximated as proposed in [15], the thermal resistance of the thermal interface (TIM)

$$R_{th,c-h} = \frac{d_{TIM}}{\lambda_{TIM} f_{pkg} A_{Si}} \tag{27}$$

and the thermal resistance of the cold plate $R_{th,h-f}$. However, $R_{th,h-f}$ is a function of the flow rate m^*_{H2O} and the cold plate dimensions as given in Fig. 8. Under the assumption that the total power losses $P_{loss,\Sigma}$ are equally distributed on the cold plate surface A_{CP} the cold plate thermal resistance

$$R_{th,h-f} = \frac{T_{h-w} + T_{w-o} + T_{o-f}}{P_{loss,\Sigma}} \tag{28}$$

is calculated from the temperature rise of the coolant T_{o-f} (inlet to outlet), the temperature rise T_{w-o} across the liquid coolant convection film from the walls of the tube to the coolant and the temperature rise T_{h-w} through the cold plate as proposed in [16].

The thermal resistance of the cold plate as a function of the cold plate surface A_{CP} and the flow rate is depicted in Fig. 10 for $w_{CP} = l_{CP}$, $h_{CP} = 4$mm, $d_t = 2$mm, $s_t = 10$mm. As can be seen from the figure, for a typical [17] flow rate of 300l/h, the temperature rise $P_{loss,\Sigma} R_{th,h-f}$ due to power losses in the range of $P_{loss,\Sigma} = (1/\eta - 1)\, P_{max} \approx 250$W is low, all of the heat can be removed by the cold plate and the assumptions made for the cold plate dimensions in (26) are valid.

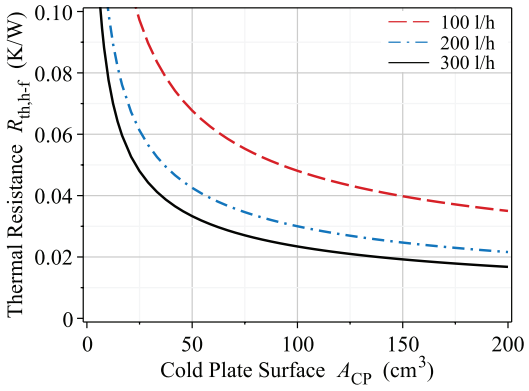

Fig. 10. Thermal resistance $R_{th,h-f}$ of the cold plate as a function of the cold plate surface and the flow rate.

C. Inductor L

Losses of an inductor depend on the core shape, the core material and the winding type, such as a foil or Litz wire winding. As it is not the intention of this paper to optimize each of the possible combinations, certain assumptions have to be made. Firstly, the utilized core material is EPCOS N87 ferrite and the inductance L is controlled with the air gap length l_g. Secondly, the shape of the inductor is based on the reference inductor design depicted in Fig. 11, consisting of four E65/32/27-cores and that is well balanced regarding core volume, window area and average winding length.

In order to calculate the losses for an arbitrary inductor volume, all important geometrical quantities such as the window dimensions, core cross section A_c or core volume V_c have to be related to the inductor volume V_L by scaling factors, e.g.

$$s_{Ac} = \frac{A_{c,ref}}{V_{L,ref}^{2/3}} = \frac{2 c_{ref} f_{ref}}{V_{L,ref}^{2/3}} = 0.310 \tag{29}$$

that are determined for the reference inductor design.

The key equations for the inductor design with the reluctance R_m of a gapped inductor that is calculated as proposed in [18] with fringing factors to model the influence of the air gap on the magnetic circuit, are given by

$$L = \frac{N^2}{R_m}, \quad B_{pk} = \frac{L I_{L,pk}}{N A_c}. \tag{30}$$

The number of turns N is a degree of freedom in the design process for a given inductor volume, required inductance L

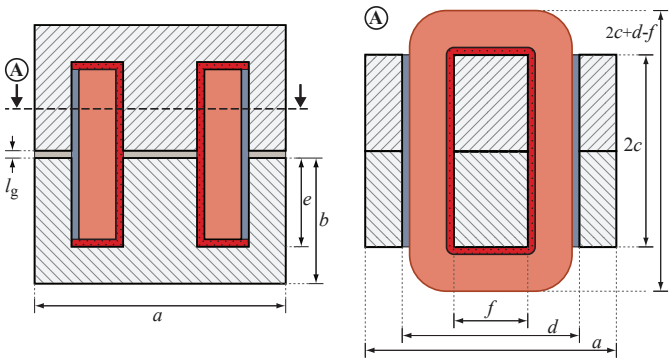

Fig. 11. Dimensions of an inductor made of four E-cores.

and worst-case inductor peak current $I_{\mathrm{L,pk}}$. However, as the peak induction B_{pk} and air gap length must not exceed a maximum value, an upper and lower limit is introduced for N

$$\frac{LI_{\mathrm{L,pk}}}{B_{\mathrm{pk,max}}A_{\mathrm{c}}} < N < \sqrt{LR_{\mathrm{m}}(l_{\mathrm{g}} = l_{\mathrm{g,max}})}. \tag{31}$$

Fitting the N turns of the Litz wire into the window area A_{w} with a filling factor k_{w} leads to an outer Litz diameter of

$$d_{\mathrm{litz}} = \sqrt{\frac{4k_{\mathrm{w}}A_{\mathrm{w}}}{N\pi}}. \tag{32}$$

According to IEC 60317-11, the number of strands in a Litz is calculated from $N_{\mathrm{s}} = d_{\mathrm{litz}}^2/p^2d_{\mathrm{s}}^2$, where $p = 1.28$ is the packing factor. The copper filling factor $k_{\mathrm{w}} = \pi/4p^2$ for a square packing of the N turns can also be determined with p.

The dc and skin losses in the winding and the losses due to the internal and external proximity effect in the Litz bundle are calculated from

$$\begin{aligned}
P_{\mathrm{L,dc}} &= \frac{R_{\mathrm{DC,E}}Nl_{\mathrm{wdg}}}{N_{\mathrm{s}}}I_{\mathrm{L,avg}}^2 \\
P_{\mathrm{L,skin}} &= \frac{R_{\mathrm{DC,E}}Nl_{\mathrm{wdg}}}{N_{\mathrm{s}}}\sum_{\nu}F_{\mathrm{R,E}}I_{\mathrm{L,pk},\nu}^2 \\
P_{\mathrm{L,pi}} &= \frac{R_{\mathrm{DC,E}}Nl_{\mathrm{wdg}}N_{\mathrm{s}}}{2\pi^2d_{\mathrm{litz}}^2}\sum_{\nu}G_{\mathrm{R,E}}I_{\mathrm{L,pk},\nu}^2 \\
P_{\mathrm{L,pe}} &= R_{\mathrm{DC,E}}N^2l_{\mathrm{wdg}}N_{\mathrm{s}}F_{\mathrm{g}}^2\sum_{\nu}G_{\mathrm{R,E}}I_{\mathrm{L,pk},\nu}^2
\end{aligned} \tag{33}$$

In (33) l_{wdg} is the average winding length, $I_{\mathrm{L,pk},\nu}$ are the Fourier amplitude coefficients of the current time function $i_{\mathrm{L}}(t)$, $R_{\mathrm{DC,E}} = 4/\sigma_{\mathrm{Cu}}\pi d_{\mathrm{s}}^2$ the dc resistance of a single strand of the Litz and $F_{\mathrm{R,E}}$ and $G_{\mathrm{R,E}}$ are factors that model the frequency dependence of the losses and are given in [19]. F_{g} is the geometry factor of the air gap field that is calculated by analytical models and validated by FEM simulations.

As a final loss contribution, the core losses are calculated with the Steinmetz Parameters k, α, β and the model

$$P_{\mathrm{L,core}} = \mathrm{DPF}\cdot k_{\mathrm{c}}f_{\mathrm{sw}}(\Delta B)^{\beta-\alpha}\sum_{j}\left|\frac{U_{\mathrm{L},j}}{NA_{\mathrm{c}}}\right|^{\alpha}(\Delta t_j) \tag{34}$$

given in [20] extended by the displacement factor DPF to consider the increase of the losses under dc bias. Measurements of the DPF for the EPCOS N87 material are given in [21].

As the winding losses increase with the number of turns N and the core losses decrease, there is an optimal number of turns for a given inductor volume V_{L} resulting in minimum total losses P_{L}. The relation between V_{L} and P_{L} under consideration of the optimum number of turns is depicted in Fig. 12 for the CF-ZVS-M inductor.

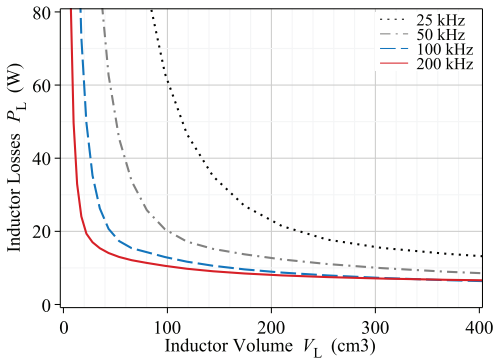

Fig. 12. CF-ZVS-M inductor losses in the worst-case operation point (U_1 = 450V, U_2 = 225V, $I_2 = I_{2,\mathrm{max}}$) as a function of the inductor volume.

IV. Topology Comparison

A. Converter Complexity

An obvious differentiating factor of the converter principles is the number of components required for realization of the power circuit including the auxiliary components and the gate drivers. Naturally, a simple structure is preferable as a large amount of heterogeneous components raises the manufacturing costs and shortens the Mean Time Between Failure (MTBF).

The CF-ZVS-M converter achieves the lowest component count but however, there is a move of complexity and know-how towards modulation strategy and software implementation. In contrast to the ACRP, SAZZ and ZCT-QZVT converter, which use the established PWM concept extended by control signals of the auxiliary switches relatively aligned to the PWM signals, time consuming calculations need to be carried out to find the switching times t_i of the CF-ZVS-M.

B. Efficiency

Under consideration of the loss models proposed in Section III the converter efficiency is calculated from

$$\eta = \frac{P_2}{P_1} = \frac{P_2}{P_2 + P_{\mathrm{S,cond}} + P_{\mathrm{S,sw}} + P_{\mathrm{L}} + P_{\mathrm{Lx}}}. \tag{35}$$

As has been shown, the semiconductor losses depend strongly on the specific device parameters and the chip area per switch and, due to the varying number of semiconductors, can only be compared among the converter concepts for the same silicon area $A_{\mathrm{Si},\Sigma}$ utilized in total. Thereto weight factors γ_i where $\sum\gamma_i = 1$ are introduced for each semiconductor device that indicate the percentage of $A_{\mathrm{Si},\Sigma}$. The weight factors given in Table II are based on converter prototypes of the CF-ZVS-M and the SAZZ converter and are calculated in relation to the sum of all RMS currents ($\gamma_i = I_{\mathrm{rms,i}}^2/\sum I_{\mathrm{rms,i}}^2$) for the ARCP and ZCT-QZVT converters but may also be found by the optimization principle proposed in [11]. As an example, the total losses of the CF-ZVS-M converter are calculated from

$$\begin{aligned}
P_{\mathrm{CF-ZVS-M}} = \frac{R_{\mathrm{DS(on)}}^*}{A_{\mathrm{Si},\Sigma}}\Bigg(&\frac{1}{\gamma_{\mathrm{S1}}}I_{\mathrm{S1,rms}}^2 + \frac{1}{\gamma_{\mathrm{S2}}}I_{\mathrm{S2,rms}}^2 + \\
&+ \frac{1}{\gamma_{\mathrm{S3}}}I_{\mathrm{S3,rms}}^2 + \frac{1}{\gamma_{\mathrm{S4}}}I_{\mathrm{S4,rms}}^2\Bigg) + \\
&+ A_{\mathrm{Si},\Sigma}Q_{\mathrm{G}}^*\frac{U_{\mathrm{gs}}^2}{U_{\mathrm{gs,ref}}} + R_{\mathrm{L,eff}}I_{\mathrm{L,rms}}^2,
\end{aligned} \tag{36}$$

where the effective inductor resistance $R_{\mathrm{L,eff}}$ is a function of the operating point (U_1,U_2,P) and the inductor volume V_{L}.

TABLE II
Silicon Area Share

Topology	$\gamma_{\mathrm{S1}}, \gamma_{\mathrm{S3}}$	$\gamma_{\mathrm{S2}}, \gamma_{\mathrm{S4}}$	$\gamma_{\mathrm{Sx,i}}$	$\gamma_{\mathrm{Dx,i}}$
ARCP	20.6%	20.6%	2.4%	0.1%
CF-ZVS-M	28.6%	21.4%	-	-
SAZZ	20.2%	20.2%	3.3%	0.8%
ZCT-QZVT	13.3%	13.3%	11.7%	-

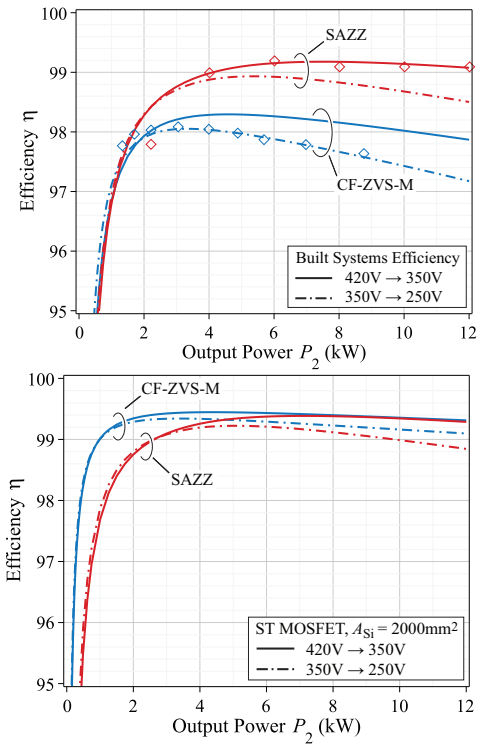

Fig. 13. Calculated efficiency of the CF-ZVS-M and SAZZ converters in the buck operation mode. The rectangles denote the measured efficiency of the CF-ZVS-M and SAZZ converter with the SAZZ efficiency as given in [10].

In case of the auxiliary circuit converters not all of the main switches cause gate and conduction losses but the additional losses of the auxiliary circuit need to be considered.

The efficiency of the CF-ZVS-M and the SAZZ converter calculated based on the device parameters listed in Table I and the switch configurations given in the publications [4][10] is depicted in Fig. 13 along with the measured results. Due to the superior characteristics of the Microsemi APT94N60L2C3 in comparison to the IXYS IXFB82N60P MOSFET, the SAZZ converter prototype outperforms the CF-ZVS-M converter.

However, the calculations based on the parameters of the ST STY112N65M5 MOSFET, which has the best FOM of the devices listed in Table I, and the same overall silicon area $A_{\mathrm{Si},\Sigma}$ applied show a comparable performance of both concepts. As can be seen from the figure, due to the constant losses in the auxiliary circuit and the reverse recovery losses, the SAZZ converter generally shows a worse part load efficiency but has a slight advantage at high output power because of the lower RMS currents in the main switches and the inductor L.

The SAZZ converter offers the highest efficiency among the auxiliary circuit converters (cf. Fig. 14) that even can be improved when the specification allows a bi-directional buck-only converter (dashed line) where the switches S_3, S_4 and the associated auxiliary circuit can be omitted. Mainly due to the higher resonant tank currents the efficiency of the ZCT-QZCT converter is significantly lower, especially at light load.

It should be noted that the results given in Fig. 13 and Fig. 14 also include the auxiliary inductor losses and reverse recovery losses of the main switch diodes. The loss models could not be presented in the paper due to length restrictions but, however, will be given in the transaction version of the paper, including measurements of the auxiliary inductor core

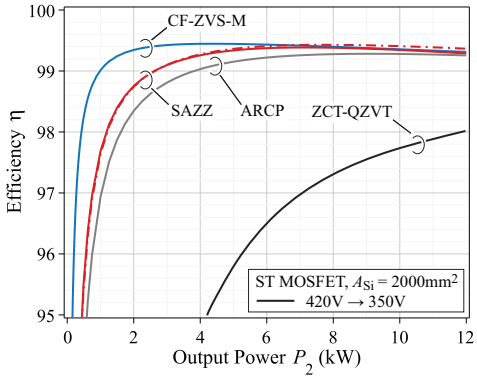

Fig. 14. Calculated efficiency of the ARCP, CF-ZVS-M, SAZZ and ZCT-QZVT converters in the buck operation mode. The dashed line indicates the efficiency of the bidirectional SAZZ buck-converter.

losses and the effective carrier life time $\tau_{\mathrm{c,eff}}$ (cf. Table I) required for recovery loss calculation with the Level-2 diode model [22]. Reverse recovery losses are negligible for the CF-ZVS-M converter but are problematic for PWM converters in spite of the auxiliary circuit.

C. Power Density

Weight and volume limitations cause the power density to be an important performance index of dc-dc converters for an automotive application and can be calculated from

$$\rho = \frac{P_{2,\max}}{(1+f_{\mathrm{pack}})(V_{\mathrm{L}}+V_{\mathrm{C}}+V_{\mathrm{S}}+V_{\mathrm{CP}}+V_{\mathrm{GD}}+V_{\mathrm{x}})} \tag{37}$$

where V_{GD} is the volume of the gate drivers, V_{x} the volume of the auxiliary circuit and a factor of $f_{\mathrm{pack}} = 30\%$ considers the increase in volume due to non-ideal packing and interconnection of the components. The volume V_{C} of the film capacitors C_1, C_2 and C_{x} is thereby estimated by the formula given in [11]. It should be noted that (37) is merely an estimation as in reality the volume occupied by current sensors, connectors and the EMI filter would further decrease the power density.

Due to the conflicting correlation of converter losses and volume, a comparison of ρ is only meaningful in consideration of the same efficiency. Therefore, the same main inductor losses $P_L = 20\mathrm{W}$, which is a good trade-off to V_{L} (cf. Fig. 12), are assumed and the total silicon area $A_{\mathrm{Si},\Sigma}$ is determined to obtain an efficiency of $\eta = 99\%$ at $U_1 = 420\mathrm{V}$, $U_2 = 350\mathrm{V}$, $P = 12\mathrm{kW}$ and a coolant temperature of $95°\mathrm{C}$.

The converter volumes for different switching frequencies are given in Fig. 15, calculated with the required $A_{\mathrm{Si},\Sigma}$ and the values of the passive components listed in Table III. Losses in the auxiliary circuit are the reason that the efficiency requirement is not reached with the ZCT-QZVT converter and is no longer met for the ARCP and SAZZ converters for a switching frequency of 100kHz and above. The calculations predict the possibility of a very compact realization of the CF-ZVS-M converter and a high switching frequency operation. The auxiliary circuit converters on the other hand are more suited for a moderate f_{sw}. If the application allows a bi-directional buck-only converter, the auxiliary circuit converters take advantage of requiring only two main switches and a smaller capacitor C_2 (in Fig. 15 and Table III exemplary denoted as SAZZ-BIBU for the SAZZ converter).

TABLE III
PASSIVE COMPONENT VALUES AND SILICON AREA

Topology	L µH	C_1,C_2 µF	L_x µH	C_x nF	$A_{Si,\Sigma}$ mm^2
25 kHz					
ARCP	100	90	43 (<0.5)	20.4	666
CF-ZVS-M	22.8	102	-	-	996
SAZZ	100	90	85 (<1.0)	20.4	632
SAZZ-BIBU	100	90, 21	85 (<1.0)	20.4	207
50 kHz					
ARCP	50	45	43 (<0.5)	20.4	1082
CF-ZVS-M	11.4	51	-	-	1003
SAZZ	50	45	85 (<1.0)	20.4	933
SAZZ-BIBU	50	45, 11	85 (<1.0)	20.4	320
100 kHz					
CF-ZVS-M	5.7	25.4	-	-	1024

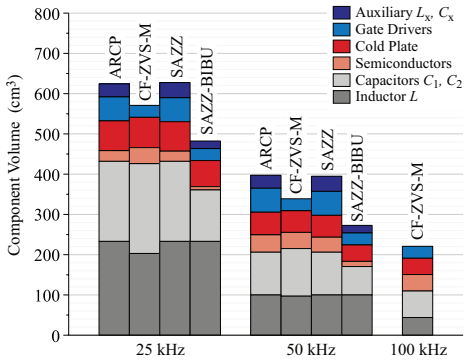

Fig. 15. Calculated converter volumes for diffent f_{sw}. For $f_{sw} \geq$ 100kHz, the assumed efficiency requirement is no longer met by the ARCP and SAZZ converters because of the increasing losses in the auxiliary circuit.

D. Multi-phase Operation

In a multi-phase converter design, an equal power balance between the N phases is of great importance, as an asymmetrical distribution could lead to an power overload of a single phase and reduced efficiency. There are two main reasons for a power imbalance in converters operated in the continuous conduction mode such as the ARCP, SAZZ and ZCT-QZVT converters, presented. Tolerances in the effective phase resistance $R_{\mathrm{ph},n}$ between the input and the output terminal that e.g. includes the $R_{DS(on)}$ of the MOSFETs and the inductor L resistance and tolerances in the duty cycle.

Figure 16 shows a simple equivalent circuit for the steady-state operation of a buck converter with an output voltage of U_2. By switching the input side half-bridge an average

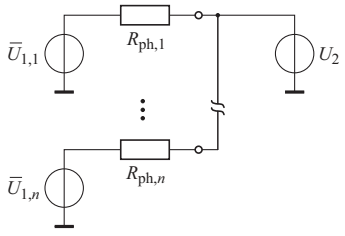

Fig. 16. Equivalent circuit for the steady-state operation of a multi-phase buck converter.

voltage $\bar{U}_{1,n} = U_1 \cdot t_{1,n}/T_\mathrm{p}$ is generated. The current of the n-th phase depends on the voltage difference between the average voltage $\bar{U}_{1,n}$ and the converter output voltage, and the effective phase resistance $R_{\mathrm{ph},n}$. Based on the model, the relative phase current error caused by a mismatch $\Delta t_{1,n}$ in the on-time $t_{1,n}$ and a tolerance $t_{\mathrm{R},n} = R_{\mathrm{ph},n}/\bar{R}_\mathrm{ph} - 1$ in the effective resistance is calculated from

$$f_{\mathrm{I,CCM}} = \frac{\eta}{vT_\mathrm{p}(1-\eta)}\Delta t_{1,n} - t_{\mathrm{R},n}, \tag{38}$$

where η is the required converter efficiency.

With simplified equations for the switching times t_i and the phase current given in [23], the relative phase current error of the the CF-ZVS-M converter is calculated from

$$f_{\mathrm{I,CF\text{-}ZVS\text{-}M}} = \frac{U_1(v\Delta t_1 + \Delta t_2)}{T_\mathrm{p}\sqrt{v^2+v+1}}\sqrt{\frac{2}{PZ}} - t_{\mathrm{L},n}. \tag{39}$$

As an example, the two error functions (38) and (39) are evaluated with $\eta = 98\%$, $T_\mathrm{p} = 100$kHz, $Z = L/T_\mathrm{p} = 0.57\Omega$ and the operating point $U_1 = 450$V, $v = 1/2$, $P = 10$kW.

$$\begin{aligned} f_{\mathrm{I,CF\text{-}ZVS\text{-}M}} &= 3.19\cdot 10^5 \Delta t_{1,n} + 6.37\cdot 10^5 \Delta t_{2,n} - t_{\mathrm{L},n} \\ f_{\mathrm{I,CCM}} &= 9.80\cdot 10^6 \Delta t_{1,n} - t_{\mathrm{R},n} \end{aligned} \tag{40}$$

As can be seen from (40), the relative error due to tolerances in the switching times is one magnitude lower for the CF-ZVS-M converter. Under the assumption of $\Delta t_i = 50$ns, the current imbalance for the CCM converters is already 49% and for the CF-ZVS-M on the contrary only 4.8%. The impact of the duty-cycle tolerances can also be seen from the measurements presented for the SAZZ converter in [10]. Current sensors for each phase and individual current controllers are required to balance the phases.

On the other hand, the power balance of a CF-ZVS-M multi-phase converter directly depends on the inductor tolerance t_L, which for a gapped inductor design mainly is due to the tolerance in the air gap length. As a large air gap length that can be manufactured to tight tolerances is required for an inductor of high peak current rating and low inductance, which is the case for the CF-ZVS-M converter, the influence of the inductor L on the power balance is relatively low. This is the reason why the CF-ZVS-M converter has the major advantage that no individual current controllers and sensors are required.

E. Further Issues of a Practical Realization

In addition to the circuit complexity, efficiency, power density and suitability for a multi-phase operation, there may be additional aspects that influence the decision process of selecting one of the converter topologies.

Firstly, the auxiliary circuit introduces a limitation in the duty cycle of the main switches and high inductor peak currents result for the CF-ZVS-M converter when a wide operating voltage range should be covered. The CF-ZVS-M converter, furthermore, typically requires a special startup modulation to rise the load voltage into the nominal operating voltage range $U_\mathrm{min}..U_\mathrm{max}$ under soft-switching. Secondly, for equal voltages $U_1 = U_2$ all main switches S_i of the PWM converters need to be switched to compensate the voltage drop between the input and output voltage terminal of the converter and efficiency will drop. Lastly, the auxiliary circuit of the ARCP and SAZZ converter is connected to a split capacitor C_1

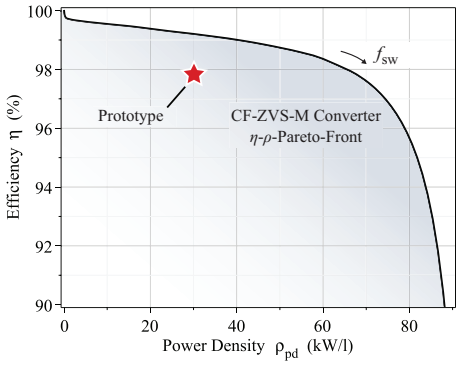

Fig. 17. η-ρ-Pareto-Front showing the performance limit of the of the CF-ZVS-M converter.

and/or C_2 and it should be accurately analyzed how symmetry of the two capacitor voltages is guaranteed.

V. η-ρ-Pareto-Front of the CF-ZVS-M Converter

The relation of multiple competing performance indices, which here are the converter efficiency η and power density ρ, can be illustrated graphically in the Performance Space [1] and the curve that defines the performance limit is the η-ρ-Pareto-Front. The η-ρ-Pareto-Front of the CF-ZVS-M converter calculated with the proposed component models for $U_1 = U_{\max}$, $v = 1/2$ and $I_2 = I_{2,\max}$ with the switching frequency as a parameter is depicted in Fig. 17. The performance of the experimental CF-ZVS-M converter is also shown in the figure. It is important to point out that for forced air cooling and at a high switching frequency the power density would rapidly drop to zero because of the increasing high-frequency losses in the inductor and the MOSFET gate losses demand for a larger cooler. On the other hand for a liquid-cooled converter higher losses correlate with a more powerful pump and/or lager heat exchanger, which however, are not considered in the calculations.

VI. Conclusion

The presented calculations and measurements affirm a comparable efficiency of the CF-ZVS-M and the SAZZ converter, which is identified as the most attractive concept of the investigated auxiliary circuit PWM converters and for the same total Silicon area an efficiency better than 99% is achieved with both of the concepts. The CF-ZVS-M converter is found to be the most promising concept to achieve high efficiency also in the part load operation and a high power density greater than 40kW/l at an efficiency of 99% due to the better suitability to operate at a high switching frequency.

The auxiliary circuit converters have conceptional advantages when the application allows a bi-directional buck converter. Then the component effort is greatly reduced and for a moderate switching frequency a higher power density is achieved in comparison to the CF-ZVS-M converter. However, bi-directional buck converters without auxiliary circuitry have been proposed as well [2][3]. Similar to the CF-ZVS-M converter, this concepts make use of the advanced semiconductor parameters by means of a soft-switching modulation only, and are also candidates for a high-performance bi-directional dc-dc converter.

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