Efficiency Optimization of an Automotive Multi-Phase Bi-directional DC-DC Converter

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***Abstract*—The paper proposes methods to improve the efficiency of a bi-directional, multi-phase buck+boost DC-DC converter for application in Hybrid Electrical Vehicles (HEV) or Fuel Cell Vehicles (FCV). Thereto, the modulation strategy for a highly-compact, 30kW/Liter, constant-frequency soft-switching converter is optimized based on a converter loss model that includes the losses in the power semiconductors and the buck+boost inductor. An algorithm for numerical calculation of the optimum switching times is given, whereas the values for the loss-optimized operation of the converter are stored in a lookup-table that is accessed by the digital controller. In addition, a novel method and control concept to ensure a Zero Voltage Switching (ZVS) of all semiconductor switches by determination of a zero voltage across the MOSFET switches with analog comparators is proposed that results in the lowest inductor RMS currents for ZVS operation at the same time. Furthermore, at low output power an absolute efficiency gain of over 2.8% is achieved by partial operation of the six interleaved converter phases. A detailed description on the control concept that determines the optimum number of activated phases for the current operating point of the converter is given and verified by experimental results. The measurements prove the capability to instantaneously switch the number of active phases during operation without a overshoot or drop in the converter output voltage.**

***Index Terms*—DC-DC Converter, Efficiency Optimization, Interleaving, Multi-Phase**

I. Introduction

Hybrid Electrical Vehicles (HEVs) or Fuel Cell Vehicles (FCVs) have improved fuel economy and reduced emissions compared to conventional drive drains with a single combustion engine [1]. Both HEVs and FCVs require energy storage elements such as batteries or ultra-capacitors that provide power to the electric drive system during acceleration and are used for regenerative braking. The energy storage elements and the high voltage (HV) inverter DC-link are connected by bi-directional DC-DC converters [2].

Requirements for DC-DC converters in this application are a high efficiency, an highly compact and low cost design as well as low EMI emissions. Therefore, to minimize the overall converter volume multi-phase converters are proposed [3][4][5] that result in a volume reduction for the passive components. Typical methods to improve the efficiency include soft switching techniques [3] or the application of Silicon Carbide (SiC) semiconductors [5].

An applicable bi-directional buck+boost converter topology to interconnect the HV battery of a HEV or FCV to the DC-link is shown in Fig. 1. A constant-frequency soft-switching modulation of the MOSFET switches S_1 to S_4 that is characterized by a negative offset current I_0 at the start of the pulse period T_p, as depicted in Fig. 2 for the boost operation mode, ensures a Zero Voltage Switching (ZVS) of the four switches without an additional circuit effort [3]. An excellent efficiency over a wide output power range (cf. Fig. 9) and also for a wide voltage transfer ratio U_2/U_1 is achieved. A picture of one out of six converter phases that has a power density of 30 kW/Liter at a maximum output power of $P_{2,max}$ = 12kW, an input voltage range of U_1 = 150..450V and an output voltage range of U_2 = 150..450V is shown in Fig. 3.

For further efficiency improvement of the converter phases, an algorithm based on the converter loss model that identifies the loss-optimized modulation strategy for the MOSFET switches is presented in section II and section III. Additionally, the efficiency of the multi-phase converter could be improved at light output power P_2 by partial phase operation [5], but no comprehensive theoretical results and measurements of the transient behavior when the number of active phases is changed have been published so far. Therefore, the analytical

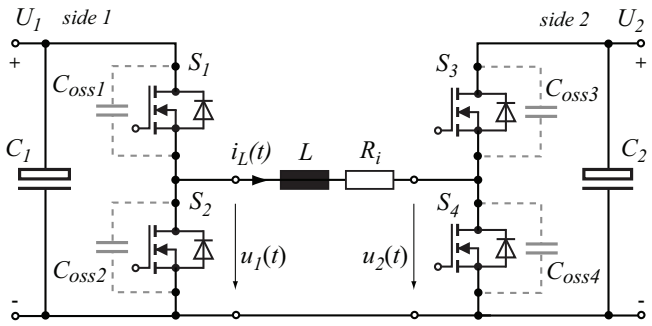


Fig. 1. Cascaded buck+boost converter for bi-directional power-flow, shown with parasitic MOSFET output capacitances $C_{oss,i}$ and the effective loss resistance R_i.

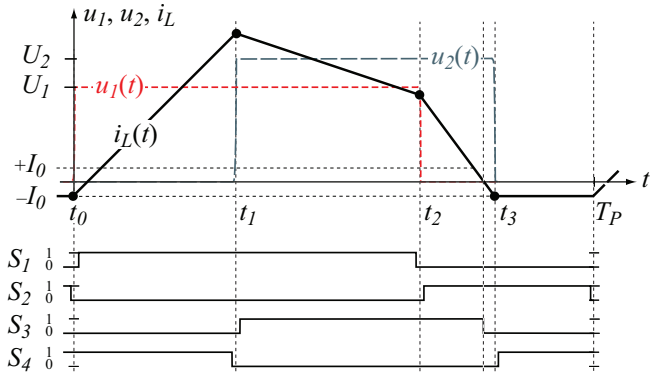


Fig. 2. Basic timing diagram for the switch S_1 to S_4 control signals, the half-bridge voltages $u_1(t)$, $u_2(t)$ and the inductor current $i_L(t)$ for boost operation ($U_2 > U_1$).

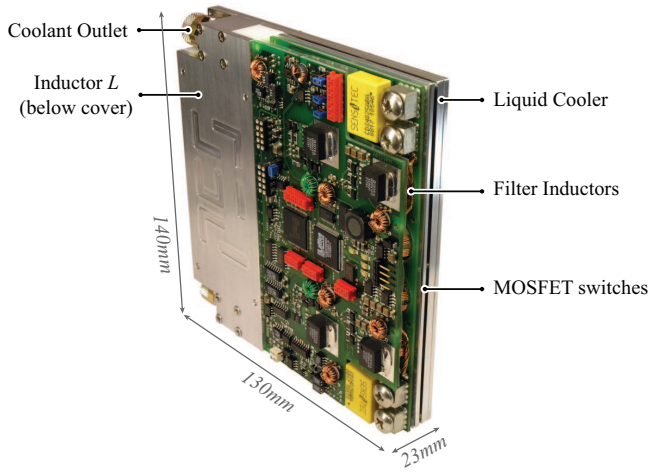


Fig. 3. Photo of a converter phase module with a power density of 30 kW/Liter at a maximum output power of 12kW.

calculation of the optimum number of phases to operate at partial load is given in section IV and detailed experimental results are provided in section V.

II. Loss-optimized Modulation Strategy

Efficiency optimization of the modulation method depicted in Fig. 2 could be done analytically based on a converter loss model. Major loss mechanism are conduction losses in the switches S_1 to S_4 and the inductor L that are modeled by a single effective loss resistance R_i connected in series to the inductor L (cf. Fig. 1). The numeric value of R_i depends on the $R_{ds,on}$ of the four MOSFET switches and on the inductor AC resistance for a given operating point and is varying for the four time intervals $T_i = [t_{i-1}..t_i]$. The switching losses and filter losses are neglected in the optimization, since these are low for the given ZVS converter but could also be modeled as part of the effective loss resistance R_i.

In order to maximize the efficiency

$$\eta(P_{2,n}) = \frac{P_{2,n}}{P_{2,n} + P_{loss}} \tag{1}$$

of a converter phase module n, the exact time function of inductor current $i_L(t)$ must be known, since the losses are approximately proportional to the square of the inductor RMS current ($P_{loss} \propto I^2_{L,rms}$). Thus, the differential equation of the inductor current including the loss resistor R_i is solved for each of the time intervals T_i, under the assumption of constant capacitor voltages U_1 and U_2 and is given by

$$i_{L,i}(t) = (I_{L,i-1} - \frac{U_{L,i}}{R_i}) \cdot e^{-\frac{R_i}{L}(t-t_{i-1})} + \frac{U_{L,i}}{R_i}. \tag{2}$$

In (2), $I_{L,i-1}$ is the value of the inductor current at the switching time t_{i-1} and $U_{L,i}$ the applied inductor voltage that is given by $+U_1$, $U_1 - U_2$, $-U_2$ and 0V in the four different time intervals T_i. As can be seen from Fig. 4, there are different combinations of the switching times t_1 to t_3 that result in the same converter output power

$$P_2 = U_2 \cdot \int_{t_1}^{t_3} i_L(t)dt \tag{3}$$

whereas the best efficiency is achieved for the switching time combination that results in the lowest inductor RMS current $I_{L,rms}$ since $P_{loss} \propto I^2_{L,rms}$. However, two constraints must be met to form the inductor current i_L. Firstly, $i_L(t = T_p)$ must match the negative offset current $-I_0$ at the beginning of the subsequent pulse period

$$-I_0 = i_{L,4}(T_P) \tag{4}$$

and a minimum magnitude of $I_0 \geq max(U_1, U_2) \cdot \sqrt{\frac{N_{sw} C_{oss}}{L}}$ that depends on the parasitic output capacitances $C_{oss,i}$ of the MOSFET switches is required to provide soft-switching conditions for the switches S_i. Secondly, also at $t = t_1$ and $t = t_2$ the inductor current must be above I_0 to achieve ZVS. These constraints induce a minimum switching time $t_{1,min}$ and a minimum length $T_{3,min}$ of the time interval T_3.

Since a transcendental equation is obtained when (1) is evaluated with (3) and (2) that cannot be maximized analytically, the times t_1 to t_3 for optimum efficiency are calculated numerically for a given operating point (U_1, U_2, $P^*_{2,n}$). For instance, for the buck operation mode (cf. Fig. 4 b)) the following algorithm is deployed:

1) Shifting t_3 toward the end of the pulse period and a maximum length of the time interval $T_2 = [t_1..t_2]$ results in the lowest RMS current. Therefore, initial values of $t_1 = t_{1,min}$ and $t_3 = T_p - T_{4,min}$ are chosen with $T_{4,min}$ as a small spare time to compensate for inductor and switching tolerances.
2) With (2), known values of I_0, R_i and the voltages U_1 and U_2, the value of t_2 is calculated analytically.
3) Equation (3) is evaluated with the results of steps 1) and 2) and compared to the desired output power $P^*_{2,n}$. In case of $P_{2,n} < P^*_{2,n}$, t_1 is increased by the modulation FPGA time step Δt = 10ns, otherwise t_3 is decreased by Δt.
4) Steps 2) to 3) are repeated until $P_{2,n}$ matches $P^*_{2,n}$.

A similar algorithm is utilized for the boost operating mode. However, an initial value for t_2 is chosen to fulfill the

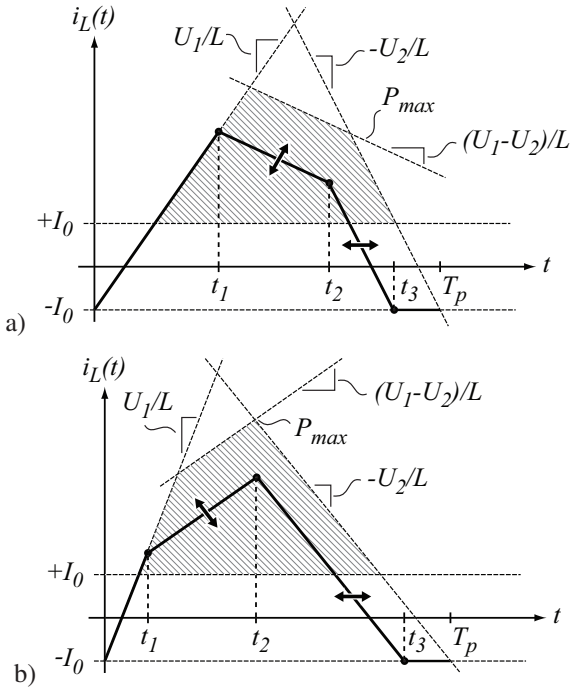


Fig. 4. Degrees of freedom in selection of the switching time t_2 and t_3 for the Boost operation (a) and t_1 and t_2 for the Buck operation mode (b).

constraint $T_3 \geq T_{3,min}$, t_1 is calculated analog to step 2). t_2 and t_3 are adjusted (cf. Fig. 4 a)) until the desired output power is matched.

A more detailed system model is advantageous in order to describe the influence of parasitic effects on the transferred power and on the efficiency. Therefore, two additional factors are considered in extension to the simplified model. Firstly, the output power P_2 strongly depends on the initial value of $i_L(0)$ at the beginning of the pulse period, i.e. the offset current I_0, especially for $P_2 \approx 0$. A uncertainty of ΔI_0 in the value of I_0 leads to an error

$$\Delta P_{2,I0} = \frac{U_1}{T_p} \cdot \Delta Q_2 = \frac{U_1}{T_p}(t_3 - t_1)\Delta I_0 \tag{5}$$

in the output power. Therefore, a detailed model of I_0 is required that can be derived from the differential equations

$$\begin{aligned} u_L(t) &= u_1(t) = L\frac{d}{dt}i_L(t) \\ i_L(t) &= -i_{Coss}(t) = -N_{sw} \cdot C_{oss}\left(u_1(t)\right)\frac{d}{dt}u_1(t) \end{aligned} \tag{6}$$

where $C_{oss}(u_1(t))$ is the nonlinear output capacitance of a single MOSFET and N_{sw} is the total number of MOSFETs applied for each half-bridge. The system of differential equations (6) can only be solved numerically due to the nonlinear characteristics of $C_{oss}(u_1(t))$ but is utilized to calculate I_0 (initial conditions $i_L(0) = I_0$, $u_1 = 0$) as well as the time duration of the resonant process initiated at a given value of i_L. The calculations are in good correspondence with the offset current

$$I_{0,min} \approx \frac{1}{25.5V} \cdot max(U_1, U_2) + 1.09A. \tag{7}$$

measured for the converter depicted in Fig. 3.

Secondly, the voltages U_1 and U_2 are not constant but show a superposed voltage ripple $\tilde{u}_1$ and $\tilde{u}_2$ respectively. Thus, also the voltage applied to L varies over time, resulting in an error $\Delta P_{2,U}$, whereas the influence of $\Delta P_{2,U}$ is most significant for equal voltages $U_1 = U_2$. The detailed model that is not shown in this paper also includes the differential equations for the capacitors C_1 and C_2 to avoid that error.

Due to the high computation effort in the calculation of the switching times with the detailed model, the times are not analytically calculated by the Digital Signal Processor (DSP) but determined off-line by a computer algebra program and stored in the DSP memory in the form of three lookup-tables (LUT) in dependence on U_1, U_2 (LUT dimensions j, k) and I_2 (LUT dimension l). Assuming that U_1, U_2 are measured and I_2 is equal to a control variable $I_{2,mod}$. Then e.g. t_1 is calculated by consecutive interpolation

$$\left.\begin{array}{l} t_{1,jkl} \\ t_{1,j+1kl} \end{array}\right\} t_{1,\bar{j}kl} \quad \left.\begin{array}{l} t_{1,jk+1l} \\ t_{1,j+1k+1l} \end{array}\right\} t_{1,\bar{j}k+1l} \quad \left.\begin{array}{l} t_{1,jkl+1} \\ t_{1,j+1kl+1} \end{array}\right\} t_{1,\bar{j}kl+1} \quad \left.\begin{array}{l} t_{1,jk+1l+1} \\ t_{1,j+1k+1l+1} \end{array}\right\} t_{1,\bar{j}k+1l+1}$$

$$\left.\begin{array}{l} t_{1,\bar{j}kl} \\ t_{1,\bar{j}k+1l} \end{array}\right\} t_{1,\bar{j}\bar{k}l} \quad \left.\begin{array}{l} t_{1,\bar{j}kl+1} \\ t_{1,\bar{j}k+1l+1} \end{array}\right\} t_{1,\bar{j}\bar{k}l+1}$$

$$\left.\begin{array}{l} t_{1,\bar{j}\bar{k}l} \\ t_{1,\bar{j}\bar{k}l+1} \end{array}\right\} t_{1,\bar{j}\bar{k}\bar{l}} \tag{8}$$

in the three LUT dimensions j, k, l to determine the necessary timing for a given operation point. In (8), e.g. $t_{1,jkl}$ and $t_{1,j+1kl}$ with the indices j and $j+1$ in the dimension j are the two LUT elements adjacent to the input quantity U_1 and $t_{1,\bar{j}kl}$ is the linear interpolation of these two values in consideration of the fractional part of U_1 in respect to the two values.

III. Offset Current Control

Besides the fact that the value I_0 must be known to calculate the times t_1 to t_3 with a sufficiently low error $\Delta P_{2,I0}$, a higher magnitude of I_0 also increases the conduction losses. The additional losses caused by an offset current of $I_0 = I_{0,min} + \Delta I_0$ approximately depends on the effective loss resistance R_4 during the time interval T_4

$$\Delta P_{loss,I0} \approx R_4\left(2I_{0,min}\Delta I_0 + \Delta I_0^2\right)\left(1 - \frac{t_3}{T_p}\right) \tag{9}$$

and become most significant for a low output power P_2 since t_3 is small in this case. Therefore, a closed loop control is implemented in the modulation FPGA that minimizes I_0 to equal $I_{0,min}$. Two control concepts that utilize digital signals generated by fast analog comparators, which monitor the half-bridge voltages $u_1(t)$ and $u_2(t)$, are applied depending on the operating mode of the converter.

In the buck operation mode I_0 must be large enough to achieve ZVS at the input side of the converter, especially at $t = t_0$. An applicable controller is shown in Fig. 5 and the

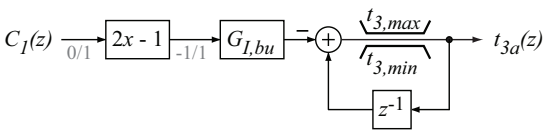


Fig. 5. I_0 controller for buck operation, sampling time T_p, sampling point t_{0b}.

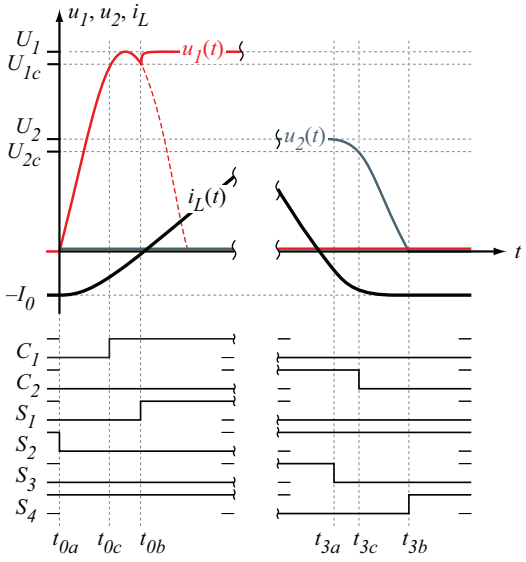


Fig. 6. Detailed timing diagram of the switch $S_1(t)$ to $S_4(t)$ gate signals and the comparator signals $C_1(t)$, $C_2(t)$ for the buck operation mode and $t = t_0$ and $t = t_3$. The comparator signal $C_1(t)$ is evaluated by an integral controller that adjusts the time t_{3a} (S_3 is turned off) in order to minimize I_0.

corresponding waveforms in Fig. 6. At $t_{0b} = t_{0a} + T_{IL,1}$, where $T_{IL,1}$ is the interlocking delay time for the half-bridge at the converter input side, the analog comparator signal

$$C_1(t) = \begin{cases} 1 \\ 0 \end{cases} \text{for} \begin{matrix} U_1 \geq U_{1c} \\ U_1 < U_{1c} \end{matrix}, \; U_{1c} = 90\% \cdot U_1 \qquad (10)$$

is sampled and scaled to $-1/+1$. An integral controller with gain $G_{I,bu} < 1$ sets the switching time t_{3a} (turn-off of S_3). Thus, in the steady state a negative voltage $u_L(t) = -U_2$ is applied to L during the time interval T_3, exactly long enough to obtain the required value of $I_{0,min}$. The requirements for ZVS of the output side half-bridge are fulfilled at the same time since $U_2 < U_1$.

However, for the boost operation mode the concept described above is not applicable since with a magnitude of $I_0 = I_{0,min}$ ZVS conditions for the input side half-bridge are always fulfilled (cf. equation (7)) and thus the comparator signal $C_1(t)$ cannot be utilized to control the switching time of S_3. On the other hand, with the ZVS modulation strategy as proposed in [3] and described in section II it is essential to have a feedback on the influence of the switching time t_3. Otherwise, when the calculated timing does not correspond to the actual situation in hardware, the average inductor current might drift toward zero as well as the transferred power.

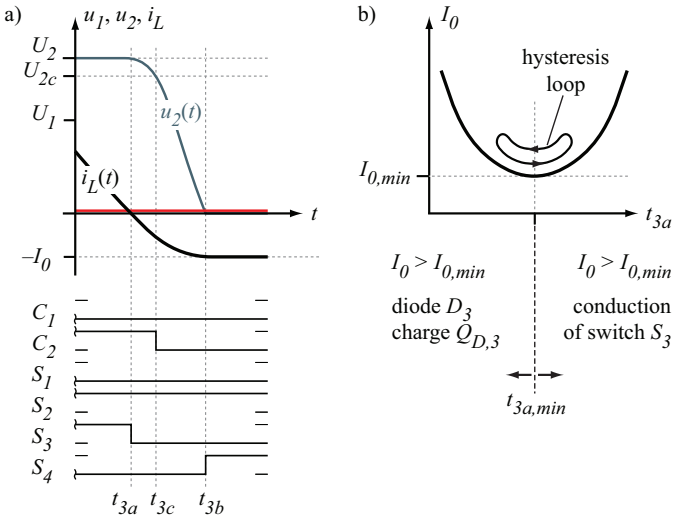


Fig. 7. Detailed timing diagram of the switch $S_1(t)$ to $S_4(t)$ gate signals and the comparator signals $C_1(t)$, $C_2(t)$ for the boost operation mode and $t = t_3$. The comparator signal $C_2(t)$ is evaluated by an hysteresis controller that adjusts the time t_{3a} (S_3 is turned off) in order to minimize I_0.

A first solution to prevent this problem is to turn S_3 off at $t_{3a} = t_2$ or at least when $i_L(t_{3a}) > 0$. Then, in interval T_3, the anti-parallel body diode D_3 conducts $i_L(t)$ for $i_L(t) > 0$. At $i_L(t) = 0$, D_3 blocks and during the subsequent resonant process i_L charges $C_{oss,3}$ and discharges $C_{oss,4}$. But in addition to the charge $Q_{oss} = N_{sw} \cdot C_{oss}(U_2) \cdot U_2$ stored in the MOSFET output capacitances, the diode diffusion charge Q_{D3} (reverse recovery charge) that has been accumulated during the diode conduction time [6] now has to be considered and increases the offset current.

Diode recovery and late turn-off of S_3 lead to a nonlinear dependence of I_0 on t_{3a} that is depicted qualitatively in Fig. 7 (b). Assuming constant values for t_1, t_2, U_1, U_2, a measurement of $t_{3b} = t_{3c} + T_{IL,2}$ (cf. Fig. 7 (a)), where $T_{IL,2}$ is the interlocking delay time for the half-bridge at the converter output side, indicates the end of the resonant process (ZVS turn-on of S_4 is allowed) and a lower t_{3b} corresponds to a lower magnitude of I_0. The time instant t_{3b} is determined with the help of the comparator signal

$$C_2(t) = \begin{cases} 1 \\ 0 \end{cases} \text{for} \begin{matrix} U_2 \geq U_{2c} \\ U_2 < U_{2c} \end{matrix}, \; U_{2c} = 90\% \cdot U_2 \qquad (11)$$

that changes at $t = t_{3c}$ and is interpreted by the hysteresis controller shown in Fig. 8.

Due to the nonlinear behavior, the implemented controller is a search algorithm that continuously adjusts t_{3a} by ΔT_3 and recognizes an improvement or worsening of I_0. In the steady state $I_{0,min}$ is maintained with a hysteresis loop as depicted in Fig. 7 (b).

Both offset current control concepts are advantageous as no accurate high-speed DC current measurement of $i_L(t)$ is required.

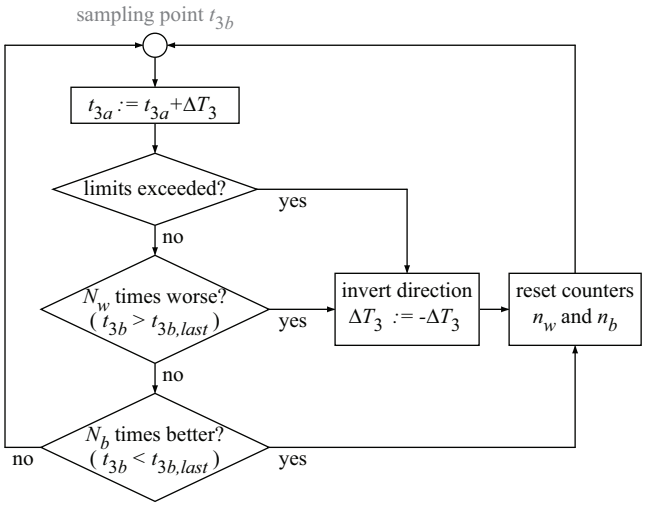


Fig. 8. Flow chart of the I_0 controller for boost operation, sampling time T_p, sampling point t_{3b}.

IV. Partial Phase Operation

In addition to the loss reduction achieved by the utilization of the low-loss modulation strategy and the optimization of the switching timing, with a multi-phase converter further improvements in efficiency could be achieved in part-load conditions.

For a multi-phase converter the overall converter output power is the sum of the output power of the N out of N_Σ active phases:

$$P_2 = \sum_{n=1}^{N} P_{2,n}. \tag{12}$$

At a low output power, for instance $P_2 = 5\% \cdot P_{2,max}$ and assuming that all available phases operated simultaneously ($N = N_\Sigma$) and with the same power $P_{2,n}$, also the phase utilization is 5%. Typically the efficiency drops dramatically in this region due to the switching losses or constant loss contributions such as gate driver losses.

Therefore, to improve efficiency, it is reasonable to turn off a certain number of phases at light load conditions of the converter system. In order to determine the number N out of N_Σ phases that should be operated at a certain output power P_2, the measured efficiency $\eta(P_{2,n})$ of a single converter phase is approximated by a fit with an analytical function. The fit function

$$\eta(P_{2,n}) = a - b \cdot \frac{1}{P_{2,n}} - c \cdot P_{2,n} \tag{13}$$

includes an inversely proportional term that primarily models the characteristic below the efficiency maximum and a linear term to characterize the efficiency drop for a high output power.

As depicted in Fig. 9 by a set of curves of the total efficiency $\eta_\Sigma(P_2) = \eta(P_2/N)$ in dependence on N, the efficiency is improved by partial phase operation for light loads, whereas the output power $P_{2,sw}(N)$ that distinguishes between N and

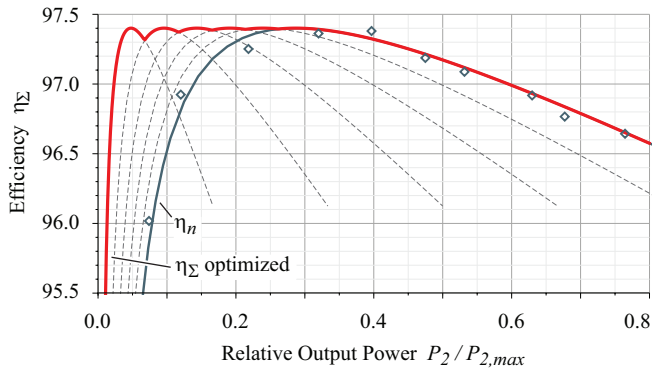


Fig. 9. Measured efficiency and curve fit (blue), improved efficiency at low relative output power $P_2/P_{2,max}$ by partial phase operation (red).

$N+1$ operated phases is calculated by the intersection of two adjacent efficiency curves:

$$\begin{aligned} \eta\left(P_{2,n} = \frac{P_2}{N}\right) &= \eta\left(P_{2,n} = \frac{P_2}{N+1}\right) \\ a - b \cdot \frac{N}{P_2} - c \cdot \frac{P_2}{N} &= a - b \cdot \frac{N+1}{P_2} - c \cdot \frac{P_2}{N+1} \end{aligned} \tag{14}$$

Solving (14) in respect to P_2 yields

$$P_{2,sw}(N) = \sqrt{\frac{b}{c} N(N+1)} \overset{N \geq 1}{\approx} \sqrt{\frac{b}{c}} \left(\sqrt{2} + N - 1\right). \tag{15}$$

that is approximately a linear function in N.

For the measured efficiency shown in Fig. 9 for U_1 = 400V, U_2 = 200V, the coefficients of the efficiency fit (13) are given by

$$\begin{aligned} a &= 98.84 \\ b &= 2476 \text{ W} \\ c &= 2.091 \cdot 10^{-4} \text{ W}^{-1} \end{aligned} \tag{16}$$

and the vector of power levels $\vec{P}_{2,sw}$ for changing the number of active phases N is listed in table I. The expected efficiency gain by partial phase operation with the efficiency characteristic depicted in Fig. 9 is approximately 2.8% at $P_2 = 5\% \cdot P_{2,max}$ and 8.3% at $P_2 = 2\% \cdot P_{2,max}$.

TABLE I
Power Levels to Change Number of Active Modules

Active Phases N	Power $P_{2,sw}$	Power per Phase
$1 \leftrightarrow 2$	4.87 kW	4.87 kW $\leftrightarrow$ 2.44 kW
$2 \leftrightarrow 3$	8.43 kW	4.21 kW $\leftrightarrow$ 2.81 kW
$3 \leftrightarrow 4$	11.9 kW	3.97 kW $\leftrightarrow$ 2.98 kW
$4 \leftrightarrow 5$	15.4 kW	3.85 kW $\leftrightarrow$ 3.08 kW
$5 \leftrightarrow 6$	18.9 kW	3.78 kW $\leftrightarrow$ 3.15 kW

V. Experimental Results

A block diagram that illustrates the connection of the phase modules and the implementation of the control concept to determine the number N of activated phases is shown in Fig. 10. The phases, as depicted in Fig. 3, are individually

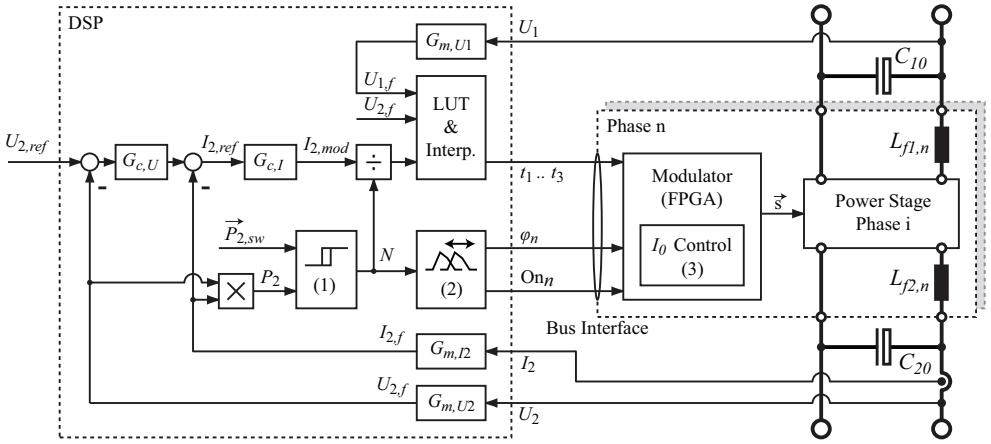


Fig. 10. Interconnection of the N_Σ phase modules by filter inductors $L_{f1,n}$, $L_{f1,n}$ to common input and output capacitors C_{10}, C_{20}, controller block diagram and communication interface between the converter phases.

connected by filter inductors $L_{f1,n}$ and $L_{f1,n}$ to the common input and output capacitors C_{10} and C_{20}.

The voltages U_1 and U_2 as well as the output current I_2 are measured, filtered (filter transfer functions $G_{m,U1}$, $G_{m,U2}$, $G_{m,I2}$) and provided to a cascaded controller with reference voltage input $U_{2,ref}$. A comparator with hysteresis (1) that is supplied with the list of power values $\vec{P}_{2,sw}$ (cf. table I) and the measured output power P_2 decides on the number N of active phases. The current controller output $I_{2,mod}$ is divided by N to calculate the reference for the phase output currents. This reference and the filtered voltages $U_{1,f}$ and $U_{2,f}$ are utilized to calculate the switching times t_1 to t_3 with the help of the lookup-table (LUT) and interpolation (cf. section II).

Furthermore, the number N of active phases is applied to a controller (2) that determines the phases to activate and calculates the phase-shift angles φ_n for a minimal output voltage ripple in interleaved operation of the phases. Thereby, the phase shift angles are not necessarily equal to an ideal value of $\varphi_n = 360°/N$ but are controlled to compensate the influence of tolerances in the inductors L that cause subharmonics of the effective switching frequency $f_{sw,eff} = N/T_p$.

The switching times, the phase shift angles φ_n and the phase activation state On$_n$ are passed to the phases together with a synchronization signal by a serial bus interface. Each phase is equipped with a FPGA that generates the gate signals $\vec{s}$ for the switches S_i and implements the offset current controllers proposed in section III.

The turn-on of the second phase at U_1 = 250V, U_2 = 160V and P_2 = 4.6kW, which is the worst case in respect to the power difference per phase (cf. table I), is shown in Fig. 11. After a short period of time the phase-shift controller sets the optimum phase shift angles φ_n and the voltage ripple $\tilde{u}_2$ measured across the common output capacitor C_{20} reduces. Further details are depicted in Fig. 12 before (a), at (b) and after (c) the turn-on of the second phase. Due to the quasi-non-continuous conduction mode that is utilized to achieve ZVS, only a low amount of energy is stored in the inductor L and the filter inductors L_f. Therefore, an instantaneous turn-on or turn-off of a phase does not result in an overshoot or drop of the output voltage U_2, as can be seen from the output ripple voltage $\tilde{u}_2$ measurement. Fig. 12 (b) also illustrates the functionality of the offset current control: Initially, the inductor current $i_{L,2}$ of the second phase is zero and the therefore invalid timing is reason to an increased I_0 at $t = t_3$. However, after a few switching periods the offset current controller compensates that error.

The measurements for the turn-on of the third phase at U_1 = 250V, U_2 = 222V, P_2 = 2kW is depicted in Fig. 13 and the turn-off of a second phase at U_1 = 250V, U_2 = 213V, P_2 = 1.8kW in Fig. 14. In each case a smooth transition of the power flow between the modules is observed. After a turn-off, the inductor current $i_L(t)$ decays with an damped oscillation between L and the output capacitances of the MOSFET switches.

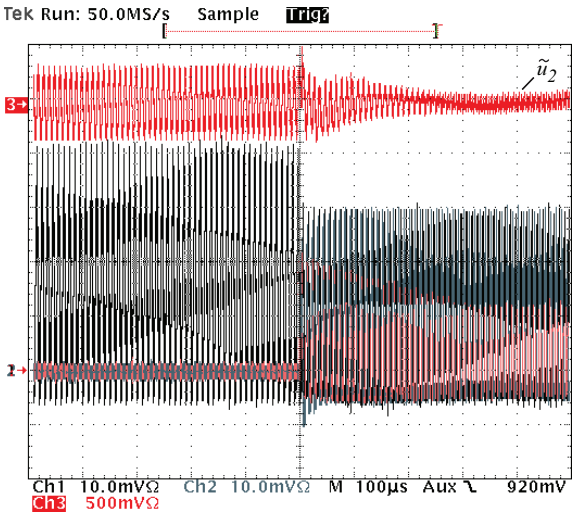
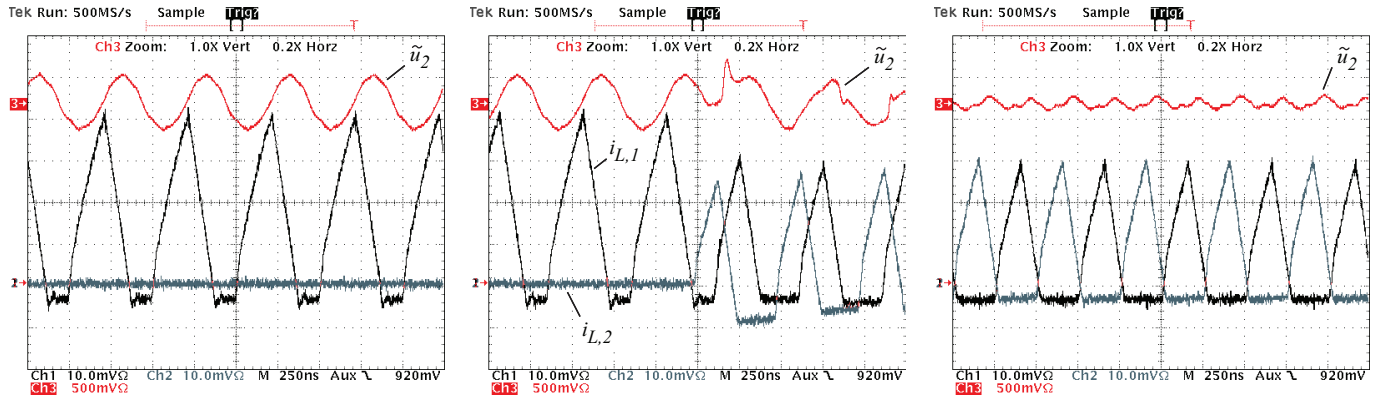


Fig. 11. Overview on the turn-on process depicted in Fig. 12: The voltage ripple $\tilde{u}_2$ across C_{20} reduces after the optimum phase shift angles φ_n are set by the phase-shift controller.



(a) (b) (c)

Fig. 12. Turn-on of the second phase at U_1 = 250V, U_2 = 160V, P_2 = 4.6kW. Few switching periods after the turn-on instance the offset current I_0 is controlled to a minimum and the phase shift is adjusted to 180°. Inductor currents $i_{L,i}$, 10A/10mV, output voltage ripple $\tilde{u}_2$, 1V/100mV.

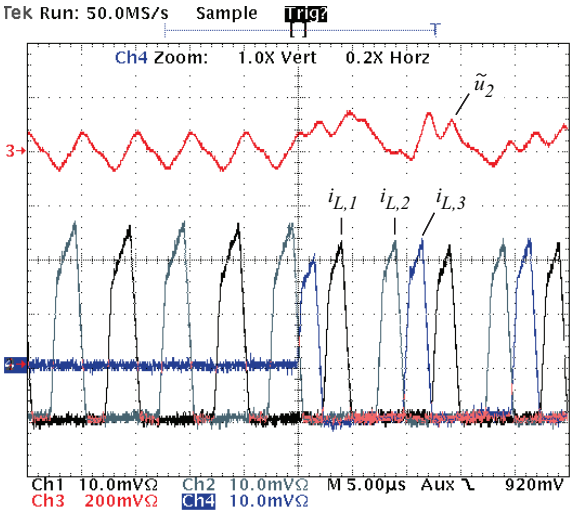


Fig. 13. Turn-on of the third phase at, U_1 = 250V, U_2 = 222V, P_2 = 2kW. Inductor currents $i_{L,i}$, 10A/10mV, output voltage ripple $\tilde{u}_2$, 1V/100mV

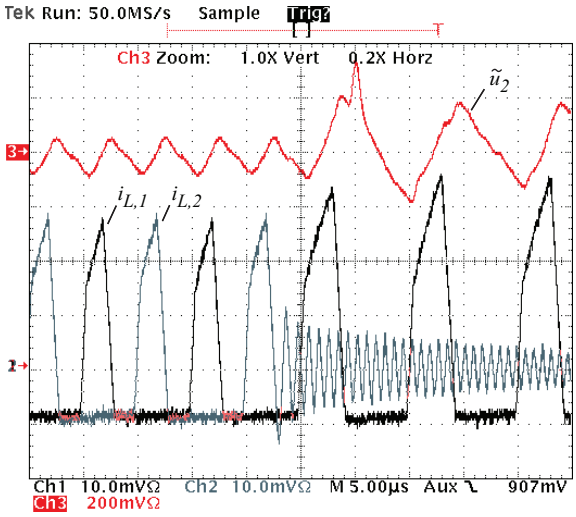


Fig. 14. Turn-off of the second phase at U_1 = 250V, U_2 = 213V, P_2 = 1.8kW. Inductor currents i_L, 10A/10mV, output voltage ripple $\tilde{u}_2$, 1V/100mV

VI. Conclusion

In this paper different methods to optimize the efficiency of a bi-directional multi-phase DC-DC converter are proposed. The overall converter efficiency benefits from the lower losses achieved with the analytical optimization of the ZVS modulation strategy and the proposed control concepts for the offset current that reduces the inductor RMS current. The novel concept ensures a Zero Voltage Switching (ZVS) of all semiconductor switches by determination of a zero voltage across the MOSFET switches with analog comparators instead of the application of a high speed DC current sensor.

Furthermore, a concept for further improvement of the efficiency of the multi-phase converter at low output power by partial phase operation is proposed and verified by experimental results. An absolute efficiency improvement of 2.8% is calculated at 5% of the maximum output power. It is shown that a stable output voltage is maintained when switching the phase count during operation.

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